

NP50P06SDG

-60V – -50A – P-channel Power MOS FET

R07DS1511EJ0100

Rev.1.00

Application : Automotive

Jun. 03, 2022

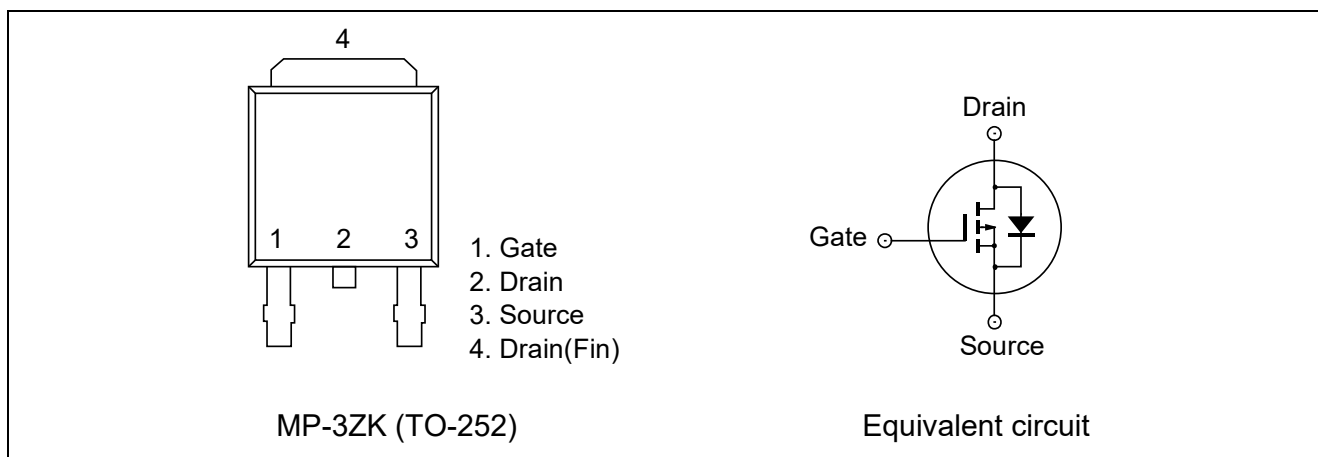
Description

This product is P-channel MOS Field Effect Transistor designed for high current switching applications.

Features

- Super low on-state resistance : $R_{DS(on)} = 16.5 \text{ m}\Omega \text{ Max. (} V_{GS} = -10 \text{ V, } I_D = -25 \text{ A)}$
 $R_{DS(on)} = 23.0 \text{ m}\Omega \text{ Max. (} V_{GS} = -4.5 \text{ V, } I_D = -25 \text{ A)}$
- Low input capacitance : $C_{iss} = 5000 \text{ pF Typ.}$
- Designed for automotive application and AEC-Q101 qualified.
- Pb-free (This product does not contain Pb in the external electrode)

Outline



Absolute Maximum Ratings

($T_a = 25^\circ\text{C}$)

Item	Symbol	Ratings	Unit
Drain to Source Voltage ($V_{GS} = 0 \text{ V}$)	V_{DSS}	-60	V
Gate to Source Voltage ($V_{DS} = 0 \text{ V}$)	V_{GSS}	± 20	V
Drain Current (DC) ($T_c = 25^\circ\text{C}$)	$I_{D(DC)}$	± 50	A
Drain Current (pulse)	$I_{D(pulse)}$ Notes1	± 150	A
Total Power Dissipation ($T_c = 25^\circ\text{C}$)	P_{T1}	84	W
Total Power Dissipation ($T_a = 25^\circ\text{C}$)	P_{T2}	1.2	W
Channel Temperature	T_{ch}	175	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to 175	$^\circ\text{C}$
Single Avalanche Current	I_{AS} Notes2	32	A
Single Avalanche Energy	E_{AS} Notes2	102	mJ

Notes 1. $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1\%$

2. Starting $T_{ch} = 25^\circ\text{C}$, $V_{DD} = -30\text{V}$, $R_G = 25 \Omega$, $V_{GS} = -20 \rightarrow 0\text{V}$, $L = 100\mu\text{H}$

Thermal Resistance

Channel to Case Thermal Resistance	$R_{th(ch-c)}$ ^{Notes3}	1.78	°C/W
Channel to Ambient Thermal Resistance	$R_{th(ch-a)}$ ^{Notes3}	125	°C/W

Electrical Characteristics

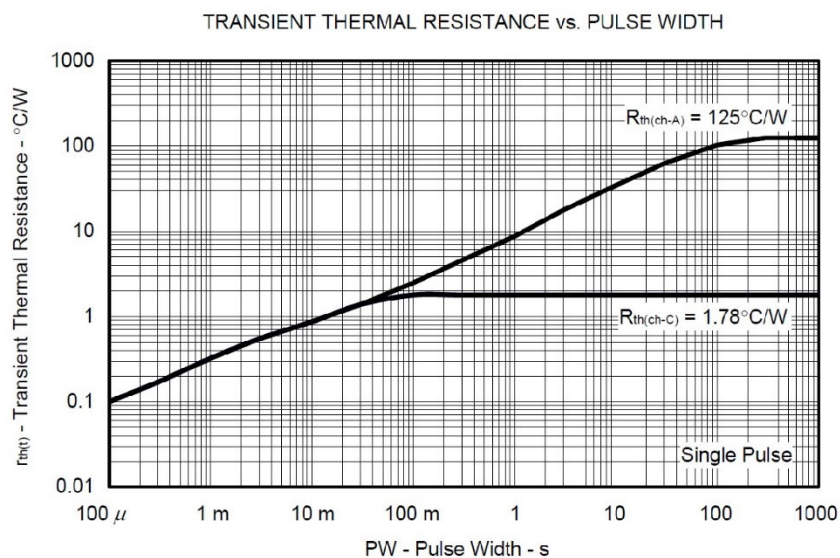
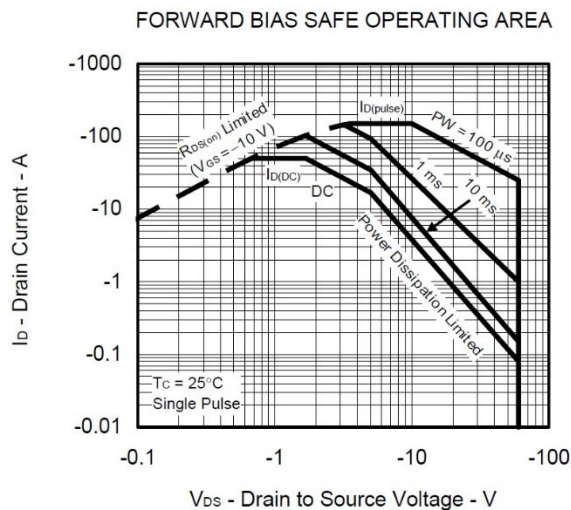
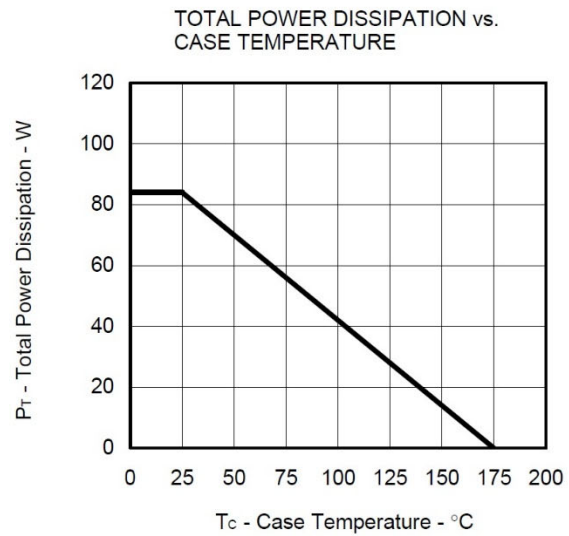
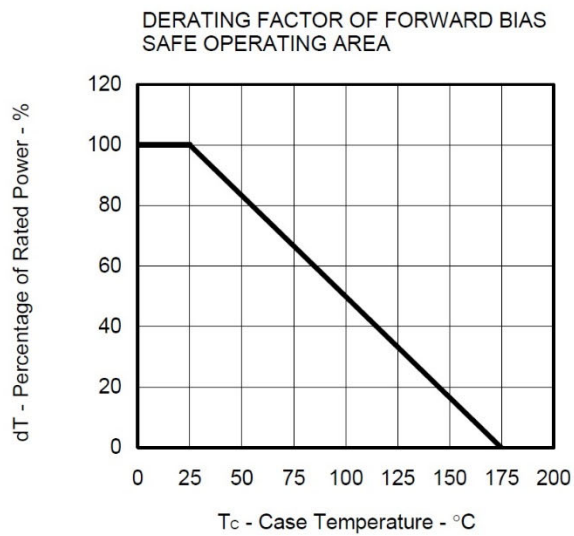
(T_a=25°C)

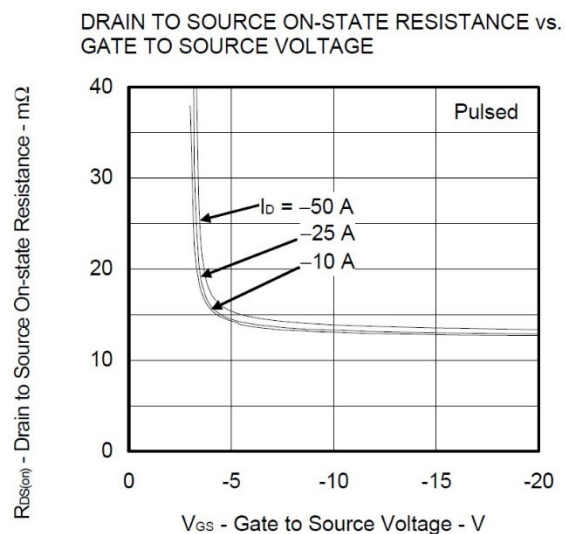
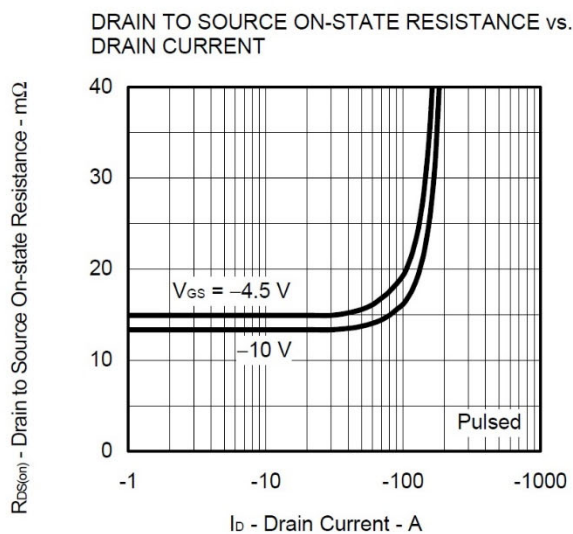
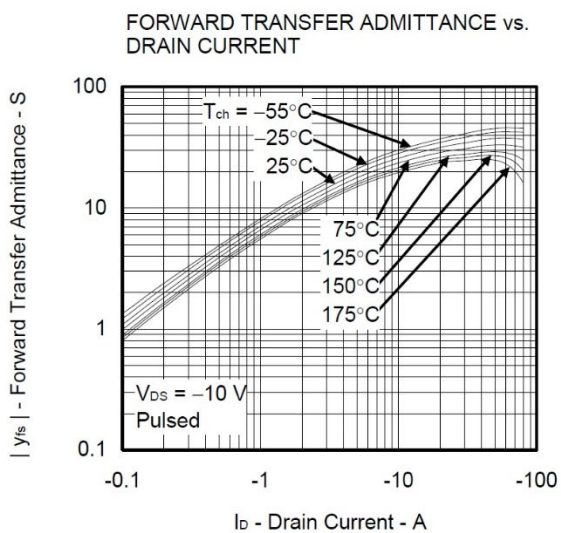
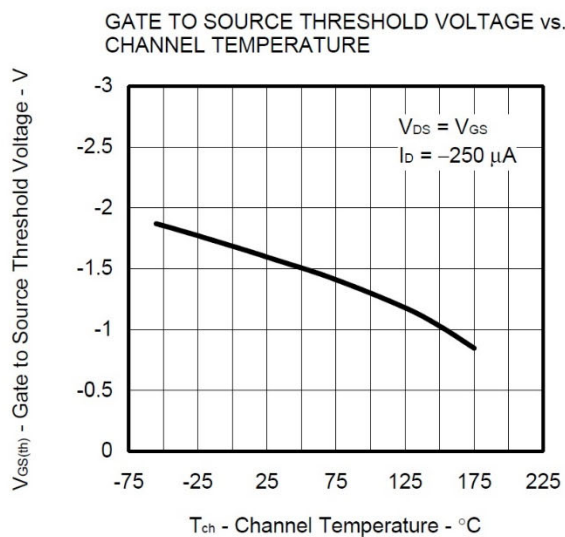
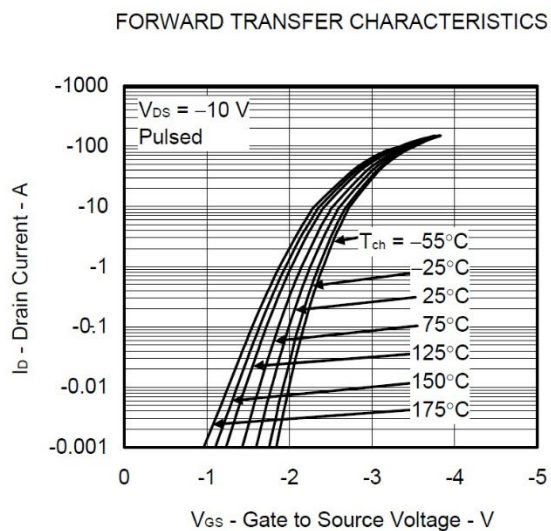
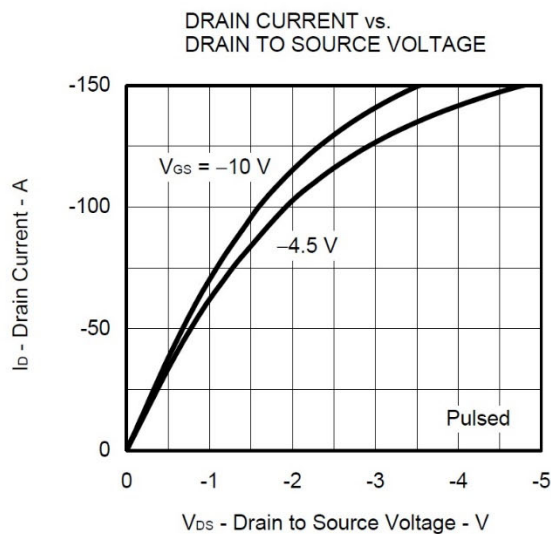
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Zero Gate Voltage Drain Current	I_{DSS}	—	—	-10	μA	$V_{DS} = -60\text{ V}$, $V_{GS} = 0\text{ V}$
Gate Leakage Current	I_{GSS}	—	—	±100	nA	$V_{GS} = \pm 20\text{ V}$, $V_{DS} = 0\text{ V}$
Gate to Source Threshold Voltage	$V_{GS(th)}$	-1.0	-1.6	-2.5	V	$V_{DS} = V_{GS}$, $I_D = -250\text{ μA}$
Forward Transfer Admittance	$ y_{fs} $ ^{Notes4}	15	33	—	S	$V_{DS} = -10\text{ V}$, $I_D = -25\text{ A}$
Drain to Source On-state Resistance	$R_{DS(on)1}$ ^{Notes4}	—	13.2	16.5	mΩ	$V_{GS} = -10\text{ V}$, $I_D = -25\text{ A}$
	$R_{DS(on)2}$ ^{Notes4}	—	14.9	23.0	mΩ	$V_{GS} = -4.5\text{ V}$, $I_D = -25\text{ A}$
Input Capacitance	C_{iss}	—	5000	—	pF	$V_{DS} = -10\text{ V}$
Output Capacitance	C_{oss}	—	600	—	pF	$V_{GS} = 0\text{ V}$
Reverse Transfer Capacitance	C_{rss}	—	300	—	pF	$f = 1\text{ MHz}$
Turn-on Delay Time	$t_{d(on)}$	—	13	—	ns	$V_{DD} = -30\text{ V}$
Rise Time	t_r	—	13	—	ns	$I_D = -25\text{ A}$
Turn-off Delay Time	$t_{d(off)}$	—	405	—	ns	$V_{GS} = -10\text{ V}$
Fall Time	t_f	—	180	—	ns	$R_G = 0\text{ Ω}$
Total Gate Charge	Q_g	—	100	—	nC	$V_{DD} = -48\text{ V}$
Gate to Source Charge	Q_{gs}	—	11	—	nC	$V_{GS} = -10\text{ V}$
Gate to Drain Charge	Q_{gd}	—	30	—	nC	$I_D = -50\text{ A}$
Body Diode Forward Voltage	$V_{F(S-D)}$ ^{Notes4}	—	0.97	1.5	V	$I_F = -50\text{ A}$, $V_{GS} = 0\text{ V}$
Reverse Recovery Time	t_{rr}	—	50	—	ns	$I_F = -50\text{ A}$, $V_{GS} = 0\text{ V}$
Reverse Recovery Charge	Q_{rr}	—	72	—	nC	$di/dt = -100\text{ A/μs}$

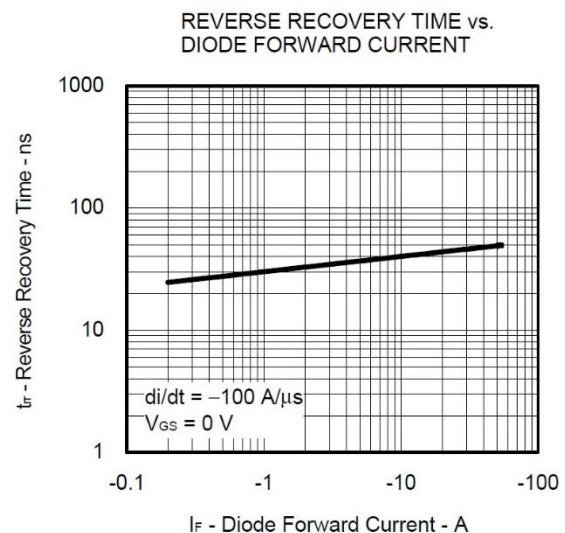
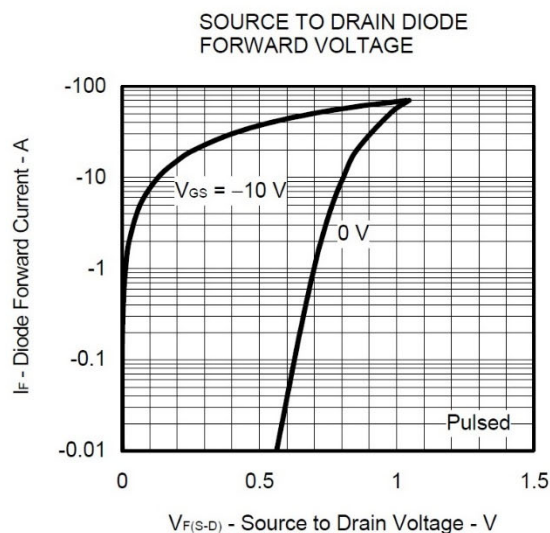
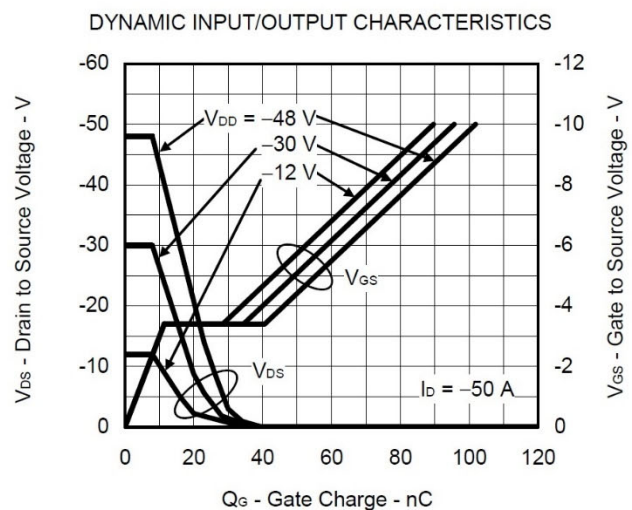
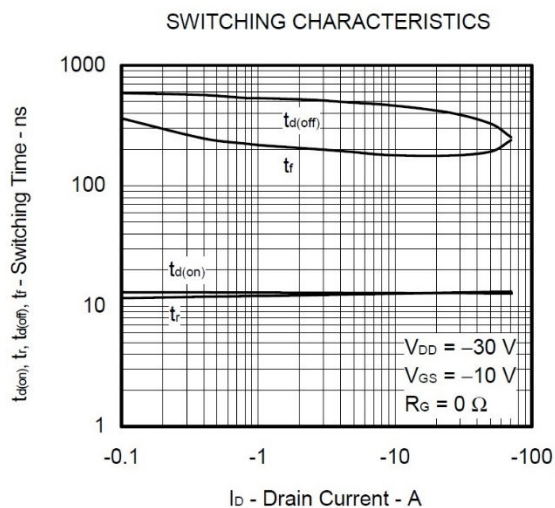
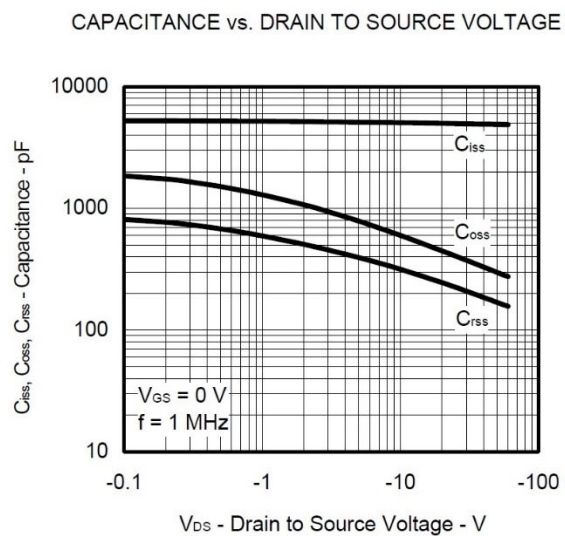
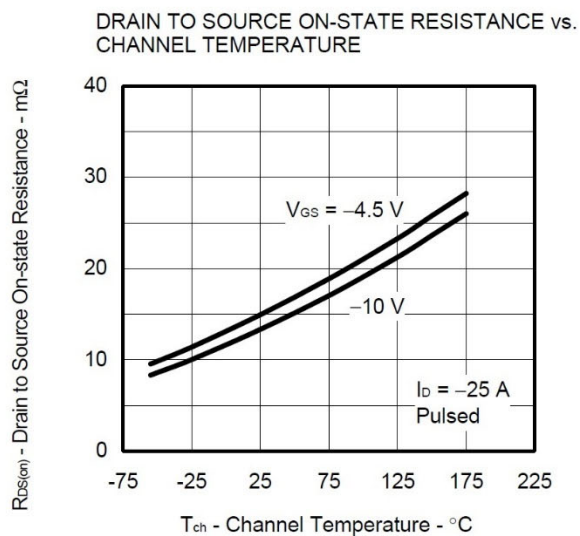
Notes 3. Designed target value on Renesas measurement condition. Not subject to production test.

4. Pulse test.

Typical Characteristics



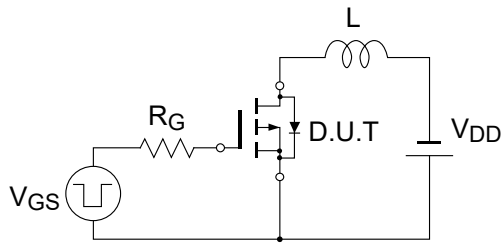




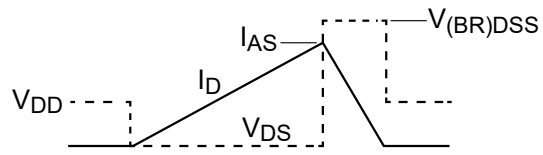
Test Circuit

Avalanche

Test Circuit



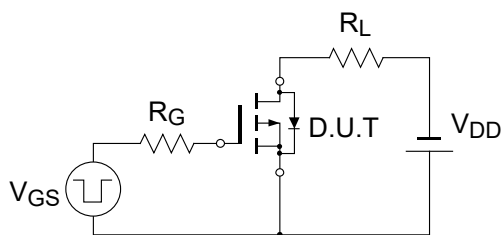
Waveform



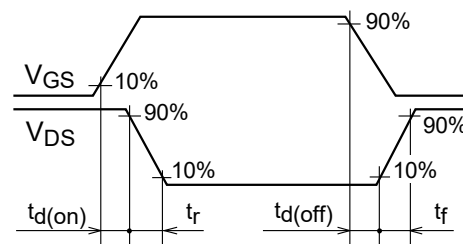
$$E_{AS} = \frac{1}{2} \cdot L \cdot I_{AS}^2 \cdot \frac{V_{(BR)DSS}}{V_{(BR)DSS} - V_{DD}}$$

Switching Time

Test Circuit

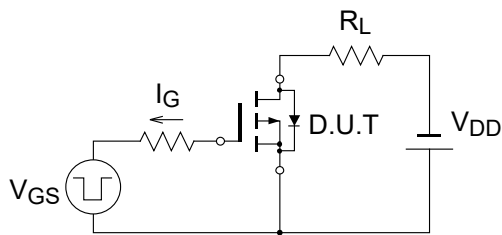


Waveform

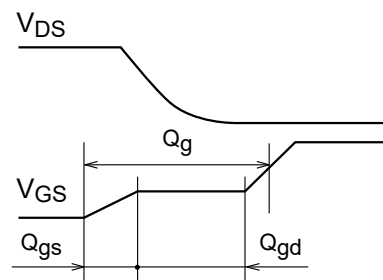


Gate Charge

Test Circuit

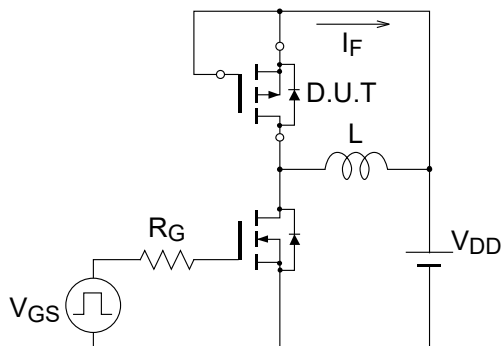


Waveform

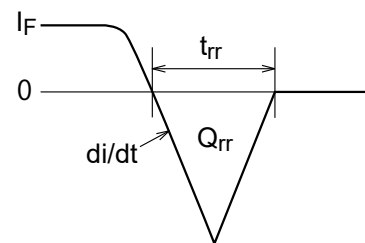


Reverse Recovery

Test Circuit



Waveform



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