



PXN011-100QL

N-channel 100 V, 11 mOhm, logic level Trench MOSFET in MLPAK33

21 September 2023

Product data sheet

1. General description

General purpose MOSFET for standard applications, 56 A, logic level N-channel enhancement mode Power MOSFET in MLPAK33 package.

2. Features and benefits

- Logic level compatibility
- Trench MOSFET technology
- Thermally efficient package in a small form factor (3.3 mm x 3.3 mm footprint)

3. Applications

- Secondary side synchronous rectification
- DC-to-DC converters
- Home appliance
- Motor drive
- Load switching
- LED lighting

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V _{DS}	drain-source voltage	25 °C ≤ T _j ≤ 150 °C		-	-	100	V
I _D	drain current	V _{GS} = 10 V; T _{mb} = 25 °C; Fig. 2		-	-	56	A
P _{tot}	total power dissipation	T _{mb} = 25 °C; Fig. 1		-	-	66	W
T _j	junction temperature			-55	-	150	°C
Static characteristics							
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 10 A; T _j = 25 °C; Fig. 9		-	8.3	11	mΩ
		V _{GS} = 4.5 V; I _D = 10 A; T _j = 25 °C; Fig. 9		-	10.4	14	mΩ
Dynamic characteristics							
Q _{GD}	gate-drain charge	I _D = 10 A; V _{DS} = 50 V; V _{GS} = 4.5 V; T _j = 25 °C; Fig. 11 ; Fig. 12		-	7.5	-	nC
Q _{G(tot)}	total gate charge			-	18	-	nC
Avalanche ruggedness							
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I _D = 9.2 A; V _{sup} ≤ 100 V; V _{GS} = 10 V; T _{j(init)} = 25 °C; unclamped	[1]	-	-	168.9	mJ

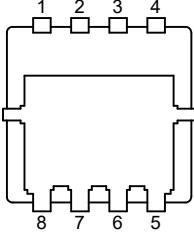
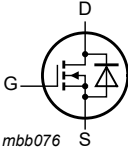
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Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Source-drain diode							
Q _r	recovered charge	I _S = 10 A; dI _S /dt = -100 A/μs; V _{GS} = 0 V; V _{DS} = 50 V; T _J = 25 °C; Fig. 15	[2]	-	19	-	nC

[1] Protected by 100% test
[2] includes capacitive recovery

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 MLPAK33 (SOT8002-1)	 mbb076
2	S	source		
3	S	source		
4	G	gate		
5	D	drain		
6	D	drain		
7	D	drain		
8	D	drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PXN011-100QL	MLPAK33	plastic thermal enhanced surface mounted package; mini leads; 8 terminals; pitch 0.65 mm; 3.3 x 3.3 x 0.8 mm body	SOT8002-1

7. Marking

Table 4. Marking codes

Type number	Marking code
PXN011-100QL	9AL

8. Limiting values

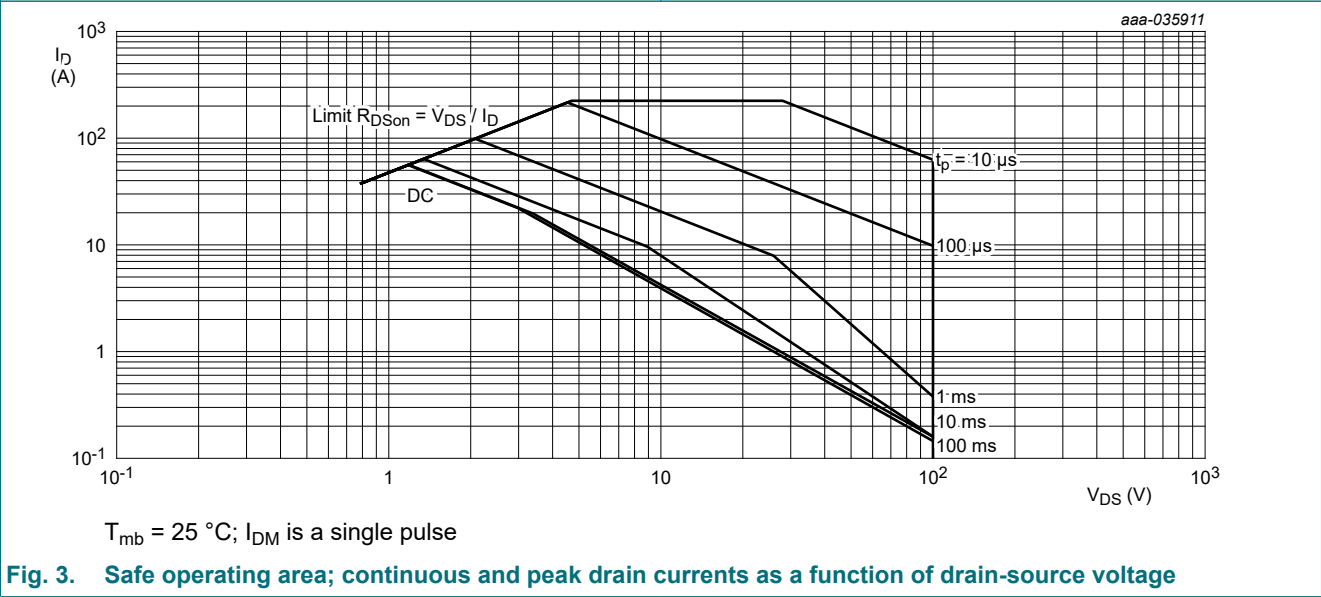
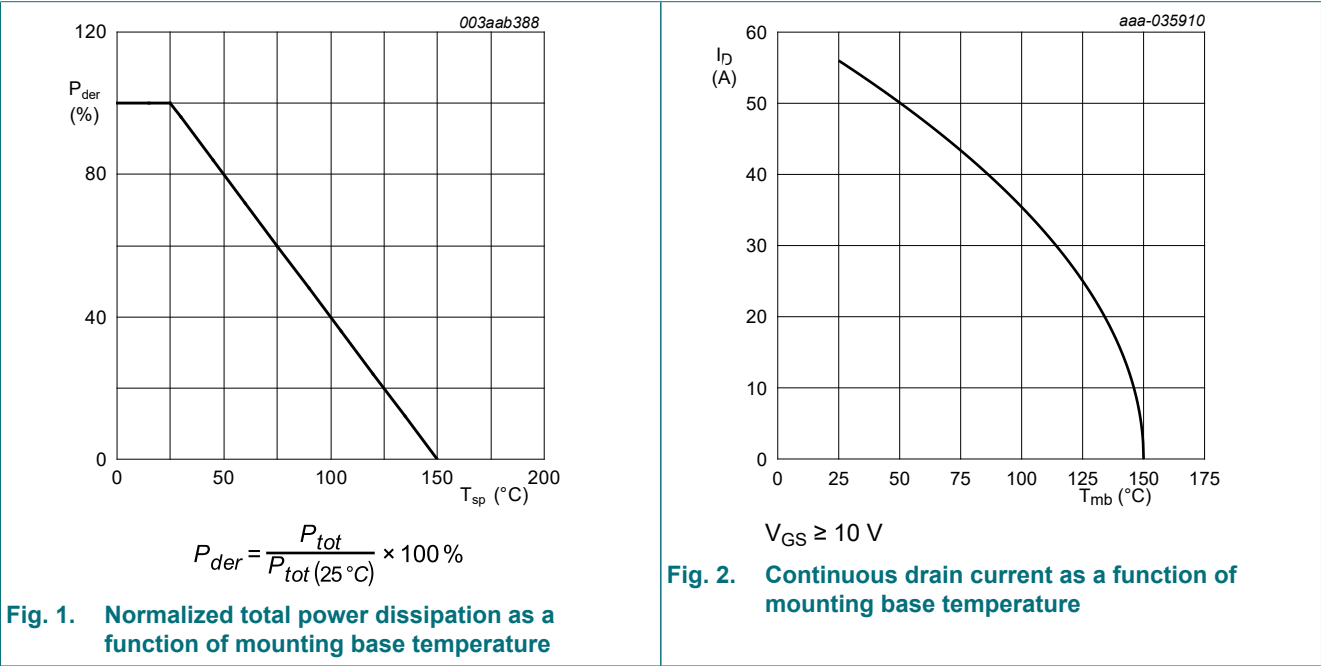
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). T_J = 25 °C unless otherwise stated.

Symbol	Parameter	Conditions		Min	Max	Unit
V _{DS}	drain-source voltage	25 °C ≤ T _J ≤ 150 °C		-	100	V
V _{GS}	gate-source voltage			-20	20	V
P _{tot}	total power dissipation	T _{mb} = 25 °C; Fig. 1		-	66	W
I _D	drain current	V _{GS} = 10 V; T _{mb} = 25 °C; Fig. 2		-	56	A
		V _{GS} = 10 V; T _{mb} = 100 °C; Fig. 2		-	35	A
I _{DM}	peak drain current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C; Fig. 3		-	224	A
T _{stg}	storage temperature			-55	150	°C

Symbol	Parameter	Conditions		Min	Max	Unit
T _j	junction temperature			-55	150	°C
T _{sld(M)}	peak soldering temperature			-	260	°C
Source-drain diode						
I _S	source current	T _{mb} = 25 °C		-	55	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C		-	224	A
Avalanche ruggedness						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I _D = 9.2 A; V _{sup} ≤ 100 V; V _{GS} = 10 V; T _{J(init)} = 25 °C; unclamped	[1]	-	168.9	mJ
I _{AS}	non-repetitive avalanche current	T _{J(init)} = 25 °C	[1]	-	9.2	A

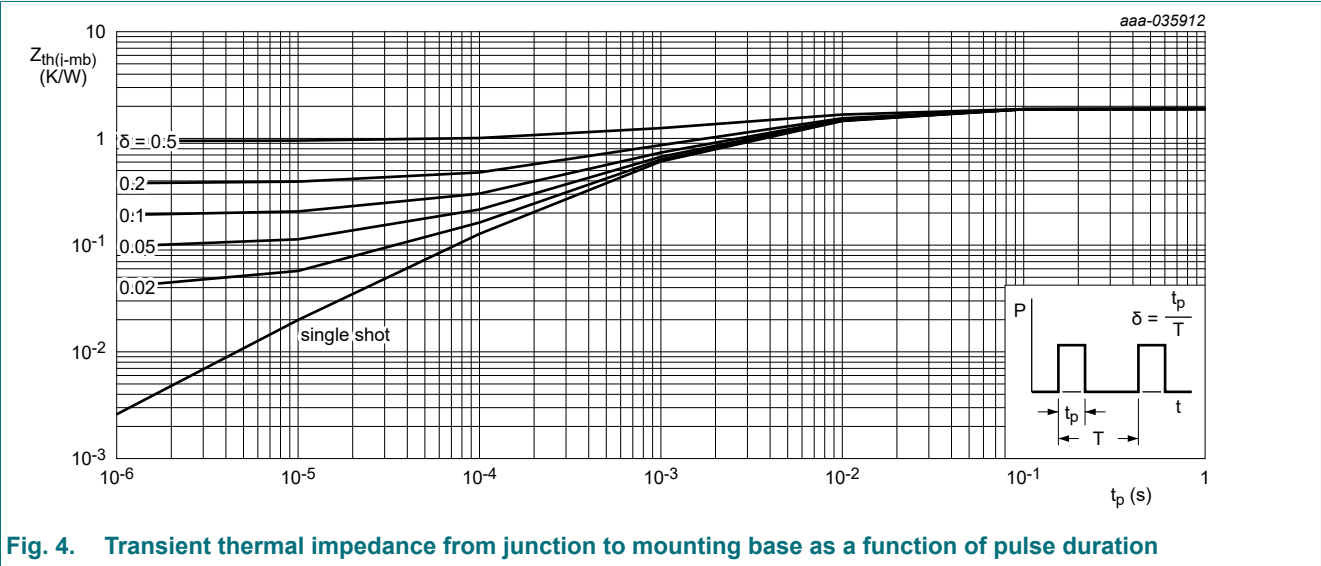
[1] Protected by 100% test



9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 4	-	1.57	1.89	K/W



10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\text{ }\mu\text{A}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$	100	-	-	V
		$I_D = 250\text{ }\mu\text{A}$; $V_{GS} = 0\text{ V}$; $T_j = -55\text{ }^\circ\text{C}$	-	100	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 0.25\text{ mA}$; $V_{DS}=V_{GS}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 8	1.2	1.53	2.2	V
		$I_D = 0.25\text{ mA}$; $V_{DS}=V_{GS}$; $T_j = 150\text{ }^\circ\text{C}$	-	0.8	-	V
		$I_D = 0.25\text{ mA}$; $V_{DS}=V_{GS}$; $T_j = -55\text{ }^\circ\text{C}$	-	1.9	-	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	$25\text{ }^\circ\text{C} \leq T_j \leq 150\text{ }^\circ\text{C}$	-	-6.1	-	mV/K
I_{DSS}	drain leakage current	$V_{DS} = 100\text{ V}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$	-	0.02	1	μA
		$V_{DS} = 100\text{ V}$; $V_{GS} = 0\text{ V}$; $T_j = 150\text{ }^\circ\text{C}$	-	22	-	μA
I_{GSS}	gate leakage current	$V_{GS} = 20\text{ V}$; $V_{DS} = 0\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$	-	2	100	nA
		$V_{GS} = -20\text{ V}$; $V_{DS} = 0\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$	-	2	100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 10\text{ A}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 9	-	8.3	11	m Ω
		$V_{GS} = 10\text{ V}$; $I_D = 10\text{ A}$; $T_j = 150\text{ }^\circ\text{C}$; Fig. 10	-	-	21	m Ω
		$V_{GS} = 4.5\text{ V}$; $I_D = 10\text{ A}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 9	-	10.4	14	m Ω
		$V_{GS} = 4.5\text{ V}$; $I_D = 10\text{ A}$; $T_j = 150\text{ }^\circ\text{C}$; Fig. 10	-	-	27	m Ω

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Symbol	Parameter	Conditions		Min	Typ	Max	Unit
R_G	gate resistance	$f = 1 \text{ MHz}$; $T_J = 25 \text{ }^\circ\text{C}$		-	1	-	Ω
Dynamic characteristics							
$Q_{G(\text{tot})}$	total gate charge	$I_D = 10 \text{ A}$; $V_{DS} = 50 \text{ V}$; $V_{GS} = 4.5 \text{ V}$; $T_J = 25 \text{ }^\circ\text{C}$; Fig. 11 ; Fig. 12		-	18	-	nC
		$I_D = 10 \text{ A}$; $V_{DS} = 50 \text{ V}$; $V_{GS} = 10 \text{ V}$; $T_J = 25 \text{ }^\circ\text{C}$; Fig. 11 ; Fig. 12		-	35	-	nC
		$I_D = 0 \text{ A}$; $V_{DS} = 0 \text{ V}$; $V_{GS} = 10 \text{ V}$; $T_J = 25 \text{ }^\circ\text{C}$		-	30	-	nC
Q_{GS}	gate-source charge	$I_D = 10 \text{ A}$; $V_{DS} = 50 \text{ V}$; $V_{GS} = 4.5 \text{ V}$; $T_J = 25 \text{ }^\circ\text{C}$; Fig. 11 ; Fig. 12		-	4.6	-	nC
$Q_{GS(\text{th})}$	pre-threshold gate-source charge			-	3	-	nC
$Q_{GS(\text{th-pl})}$	post-threshold gate-source charge			-	1.6	-	nC
Q_{GD}	gate-drain charge			-	7.5	-	nC
$V_{GS(\text{pl})}$	gate-source plateau voltage	$I_D = 10 \text{ A}$; $V_{DS} = 50 \text{ V}$; $T_J = 25 \text{ }^\circ\text{C}$; Fig. 11 ; Fig. 12		-	2.6	-	V
C_{iss}	input capacitance	$V_{DS} = 50 \text{ V}$; $V_{GS} = 0 \text{ V}$; $f = 1 \text{ MHz}$; $T_J = 25 \text{ }^\circ\text{C}$; Fig. 13		-	1898	-	pF
C_{oss}	output capacitance			-	567	-	pF
C_{rss}	reverse transfer capacitance			-	22	-	pF
$t_{d(\text{on})}$	turn-on delay time	$V_{DS} = 50 \text{ V}$; $R_L = 5 \text{ } \Omega$; $V_{GS} = 4.5 \text{ V}$; $R_{G(\text{ext})} = 5 \text{ } \Omega$; $T_J = 25 \text{ }^\circ\text{C}$		-	13	-	ns
t_r	rise time			-	21	-	ns
$t_{d(\text{off})}$	turn-off delay time			-	22	-	ns
t_f	fall time			-	18	-	ns
Q_{oss}	output charge	$V_{GS} = 0 \text{ V}$; $V_{DS} = 50 \text{ V}$; $f = 1 \text{ MHz}$; $T_J = 25 \text{ }^\circ\text{C}$		-	42	-	nC
Source-drain diode							
V_{SD}	source-drain voltage	$I_S = 10 \text{ A}$; $V_{GS} = 0 \text{ V}$; $T_J = 25 \text{ }^\circ\text{C}$; Fig. 14		-	0.8	1.2	V
t_{rr}	reverse recovery time	$I_S = 10 \text{ A}$; $dI_S/dt = -100 \text{ A}/\mu\text{s}$; $V_{GS} = 0 \text{ V}$; $V_{DS} = 50 \text{ V}$; $T_J = 25 \text{ }^\circ\text{C}$; Fig. 15		-	29	-	ns
Q_r	recovered charge		[1]	-	19	-	nC

[1] includes capacitive recovery

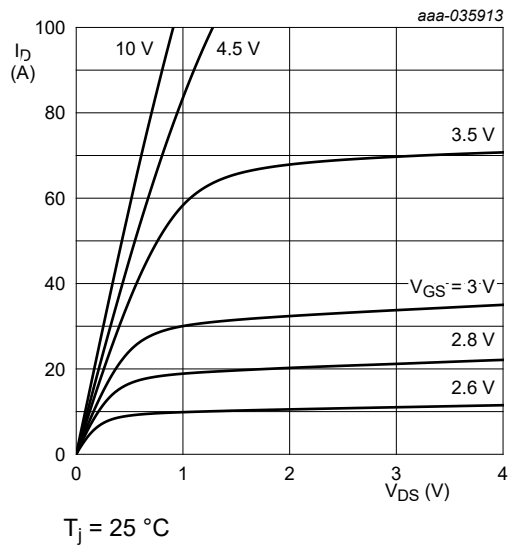


Fig. 5. Output characteristics; drain current as a function of drain-source voltage; typical values

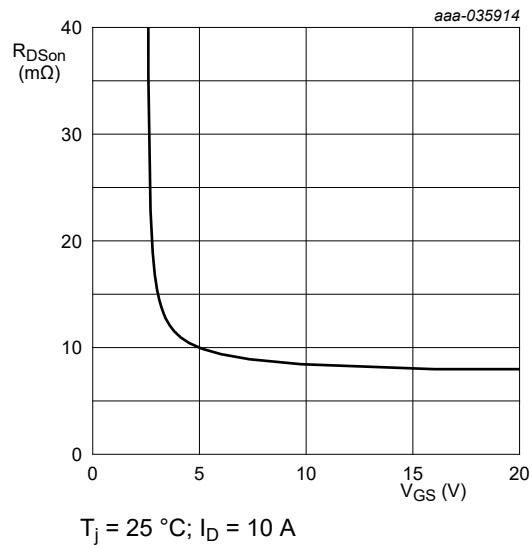


Fig. 6. Drain-source on-state resistance as a function of gate-source voltage; typical values

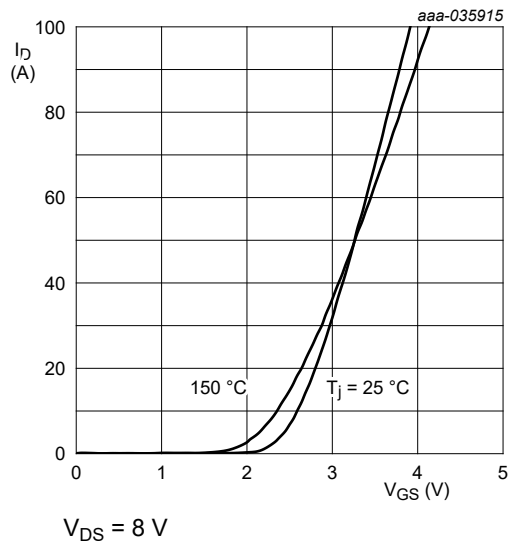


Fig. 7. Transfer characteristics; drain current as a function of gate-source voltage; typical values

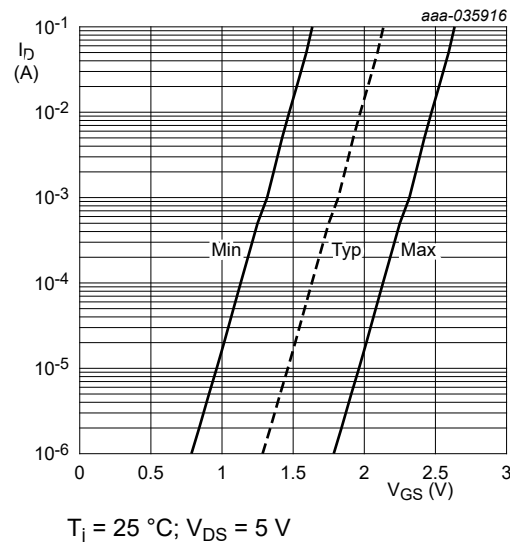


Fig. 8. Sub-threshold drain current as a function of gate-source voltage

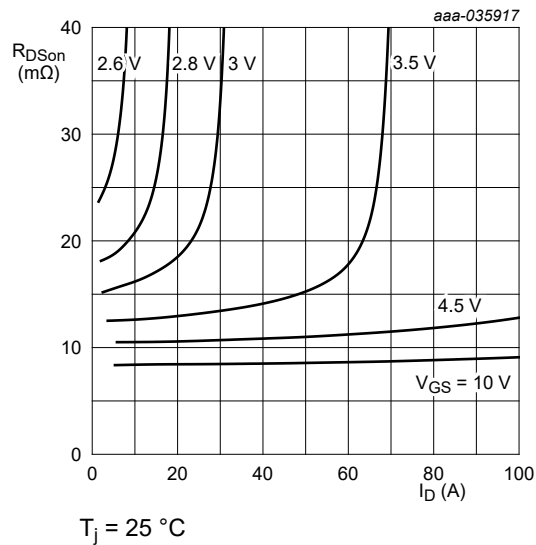


Fig. 9. Drain-source on-state resistance as a function of drain current; typical values

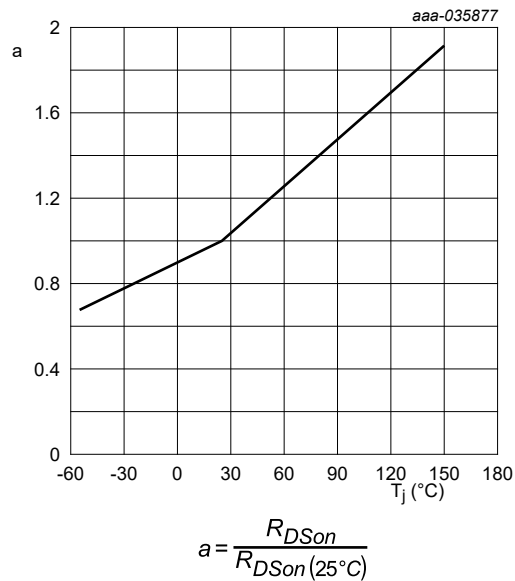


Fig. 10. Normalized drain-source on-state resistance factor as a function of junction temperature

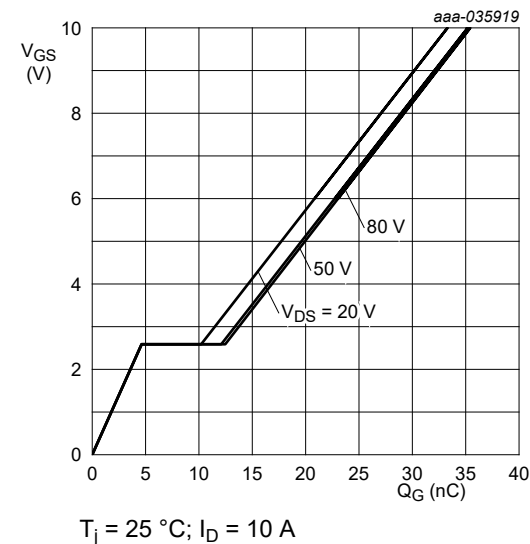


Fig. 11. Gate-source voltage as a function of gate charge; typical values

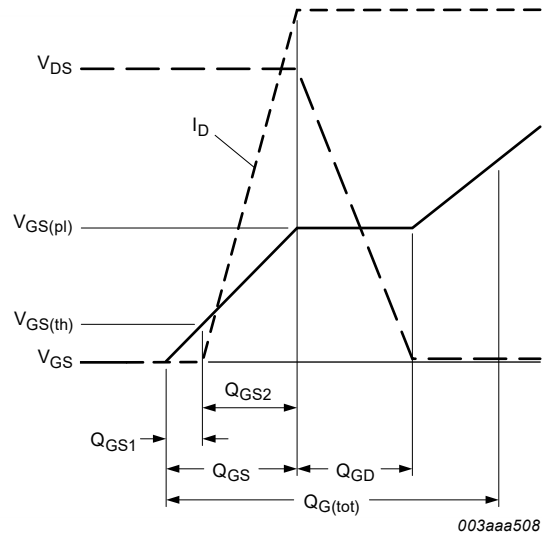


Fig. 12. Gate charge waveform definitions

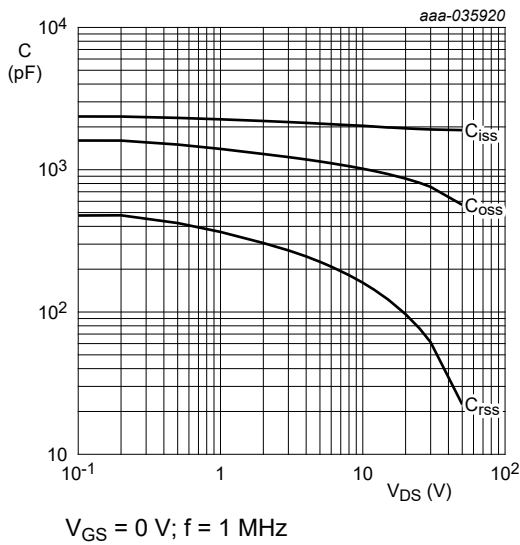


Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

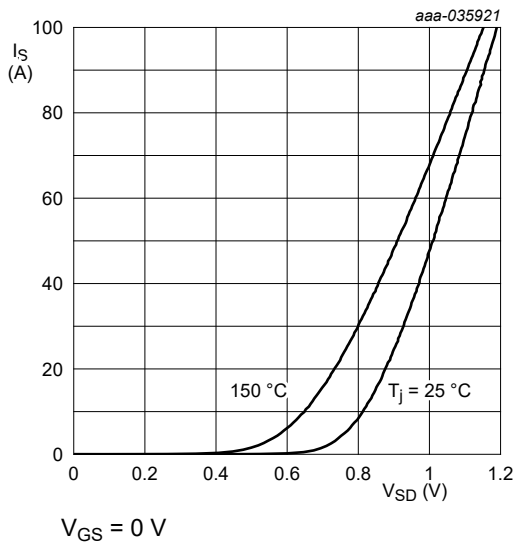


Fig. 14. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

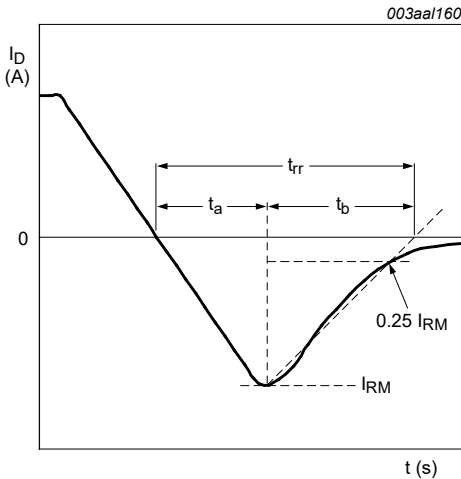


Fig. 15. Reverse recovery timing definition

11. Package outline

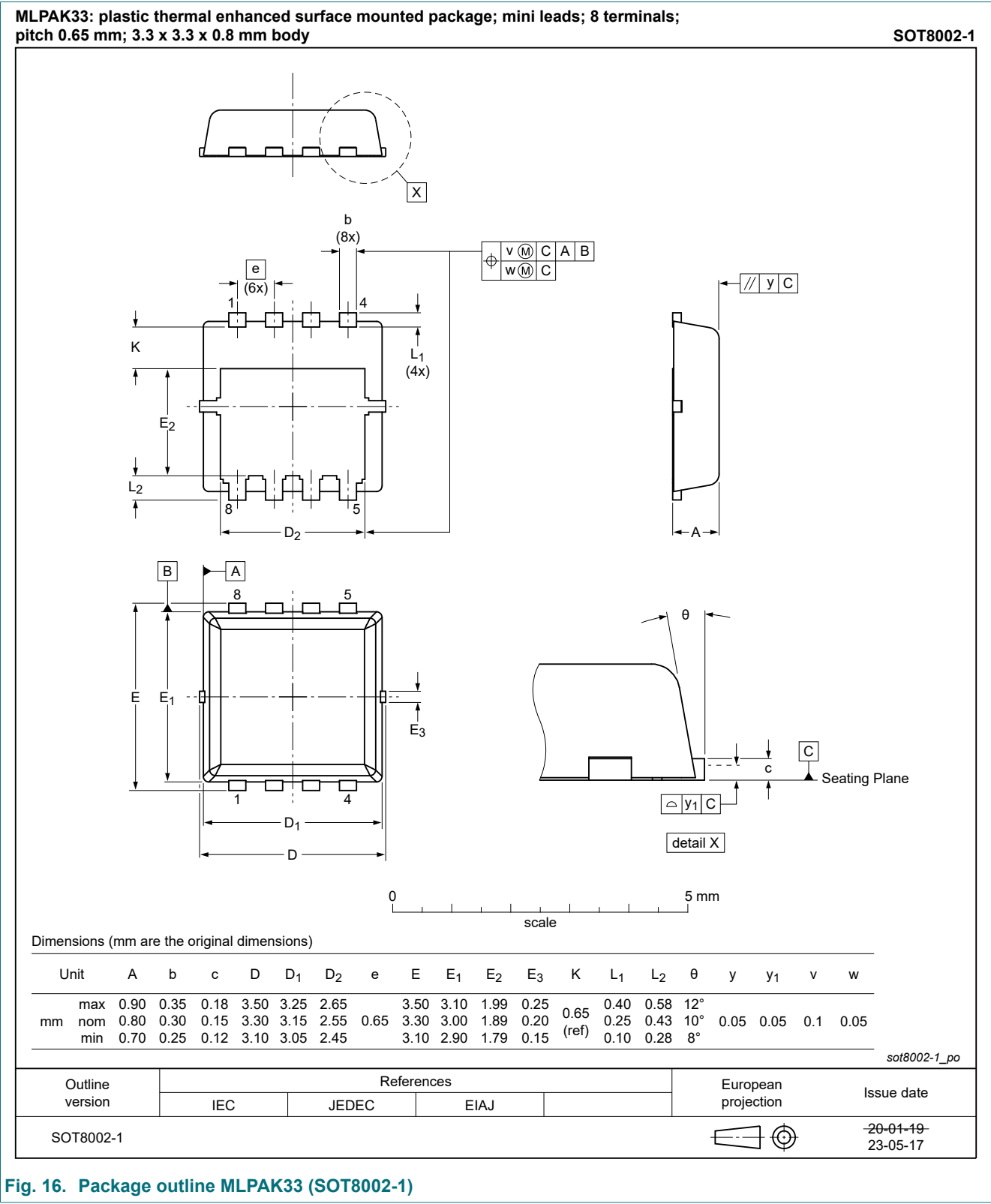


Fig. 16. Package outline MLPAK33 (SOT8002-1)

12. Soldering

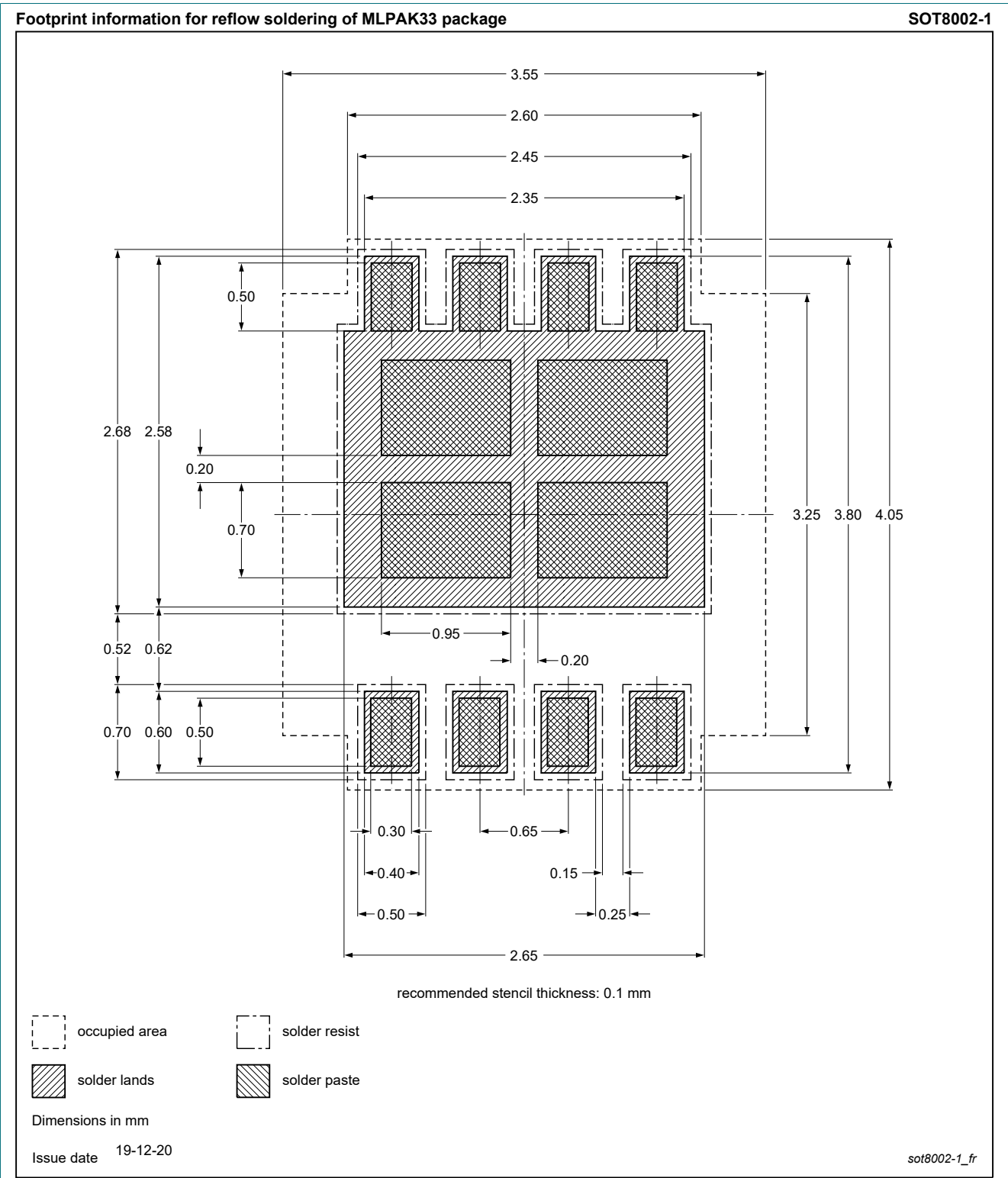


Fig. 17. Reflow soldering footprint for MLPAK33 (SOT8002-1)

13. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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