

TOSHIBA Field Effect Transistor Silicon N Channel MOS Type

SSM3K09FU

High Speed Switching Applications

- Small package
- Low on resistance
 - : $R_{on} = 0.7 \Omega$ (max) (@ $V_{GS} = 10 V$)
 - : $R_{on} = 1.2 \Omega$ (max) (@ $V_{GS} = 4 V$)

Absolute Maximum Ratings ($T_a = 25^\circ C$)

Characteristics		Symbol	Rating	Unit
Drain-Source voltage		V_{DS}	30	V
Gate-Source voltage		V_{GSS}	± 20	V
Drain current	DC	I_D	400	mA
	Pulse	I_{DP}	800	
Drain power dissipation ($T_a = 25^\circ C$)		P_D (Note 1)	150	mW
Channel temperature		T_{ch}	150	$^\circ C$
Storage temperature		T_{stg}	-55 to 150	$^\circ C$

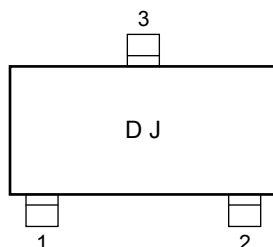
Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Mounted on FR4 board

(25.4 mm $\times$ 25.4 mm $\times$ 1.6 t, Cu Pad: 0.6 mm² $\times$ 3) Figure 1.

Marking



Equivalent Circuit (top view)

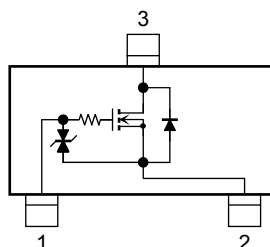
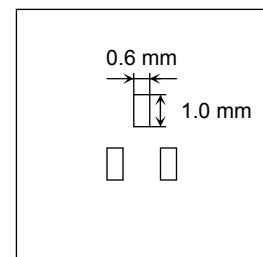


Figure 1: 25.4 mm $\times$ 25.4 mm $\times$ 1.6 t, Cu Pad: 0.6 mm² $\times$ 3



Handling Precaution

When handling individual devices (which are not yet mounting on a circuit board), be sure that the environment is protected against electrostatic electricity. Operators should wear anti-static clothing, and containers and other objects that come into direct contact with devices should be made of anti-static materials.

Start of commercial production
2000-01

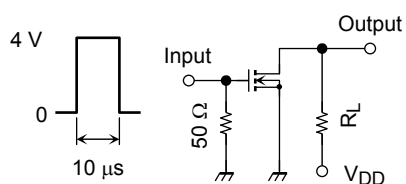
Electrical Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current	I_{GSS}	$V_{GS} = \pm 16 \text{ V}, V_{DS} = 0$	—	—	± 1	μA
Drain-Source breakdown voltage	$V_{(BR)DSS}$	$I_D = 1 \text{ mA}, V_{GS} = 0$	30	—	—	V
Drain cut-off current	I_{DSS}	$V_{DS} = 30 \text{ V}, V_{GS} = 0$	—	—	1	μA
Gate threshold voltage	V_{th}	$V_{DS} = 5 \text{ V}, I_D = 0.1 \text{ mA}$	1.1	—	1.8	V
Forward transfer admittance	$ Y_{fs} $	$V_{DS} = 5 \text{ V}, I_D = 200 \text{ mA}$ (Note2)	270	—	—	mS
Drain-Source ON resistance	$R_{DS(ON)}$	$I_D = 200 \text{ mA}, V_{GS} = 10 \text{ V}$ (Note2)	—	0.5	0.7	Ω
		$I_D = 200 \text{ mA}, V_{GS} = 4 \text{ V}$ (Note2)	—	0.8	1.2	
		$I_D = 200 \text{ mA}, V_{GS} = 3.3 \text{ V}$ (Note2)	—	1.0	1.7	
Input capacitance	C_{iss}	$V_{DS} = 5 \text{ V}, V_{GS} = 0, f = 1 \text{ MHz}$	—	20	—	pF
Reverse transfer capacitance	C_{rss}	$V_{DS} = 5 \text{ V}, V_{GS} = 0, f = 1 \text{ MHz}$	—	7	—	pF
Output capacitance	C_{oss}	$V_{DS} = 5 \text{ V}, V_{GS} = 0, f = 1 \text{ MHz}$	—	16	—	pF
Switching time	Turn-on time	$V_{DD} = 5 \text{ V}, I_D = 200 \text{ mA},$ $V_{GS} = 0 \text{ to } 4 \text{ V}$	—	72	—	ns
	Turn-off time		—	68	—	ns

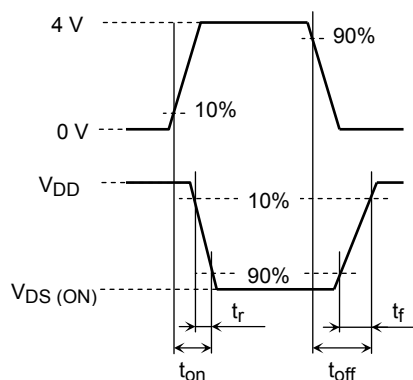
Note2: Pulse test

Switching Time Test Circuit

(a) Test circuit



$V_{DD} = 5 \text{ V}$
 D.U. $\leq 1\%$
 Input: $t_r, t_f < 5 \text{ ns}$
 $(Z_{out} = 50 \Omega)$
 Common Source
 $T_a = 25^\circ\text{C}$

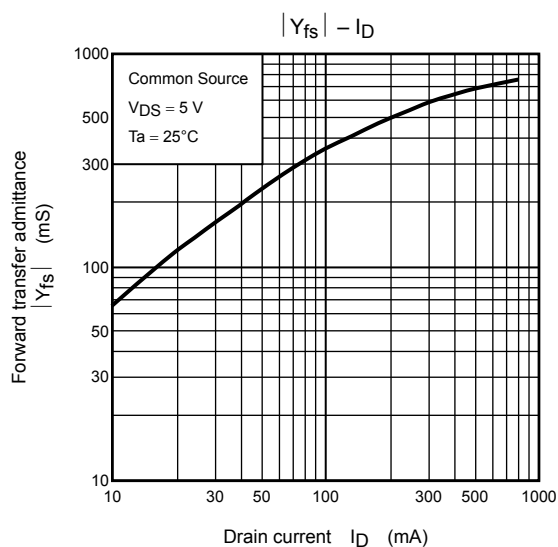
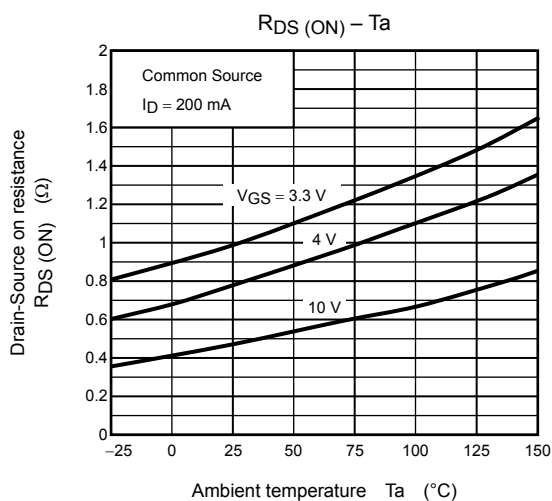
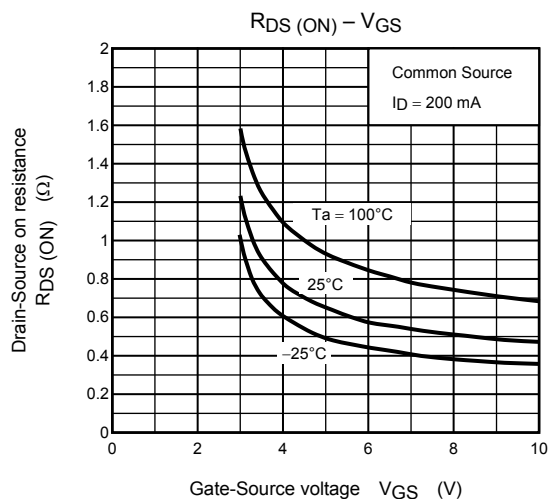
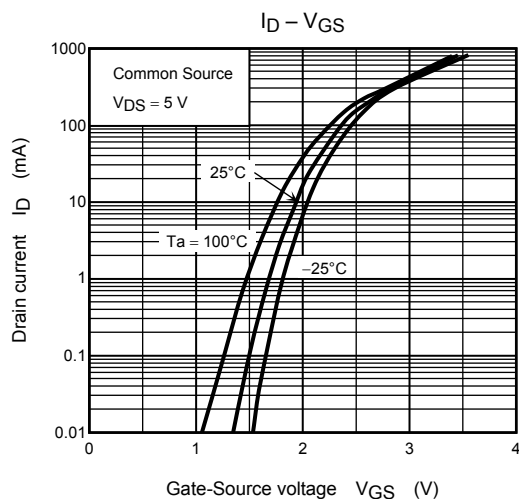
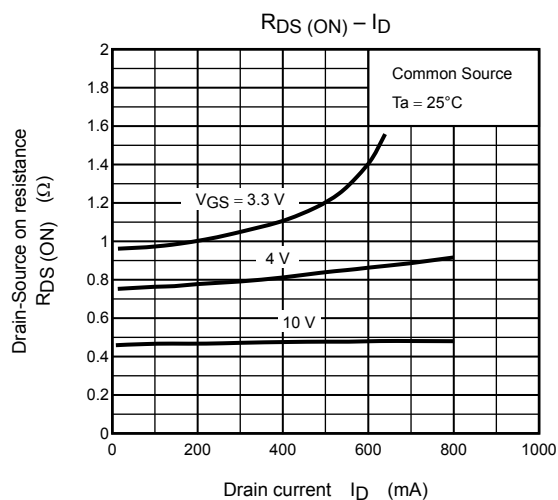
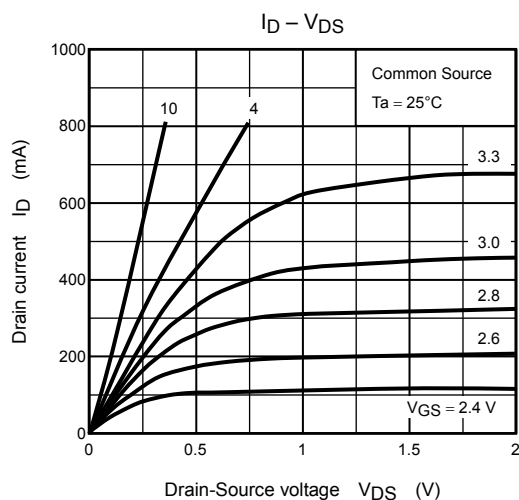
(b) V_{IN} (c) V_{OUT}

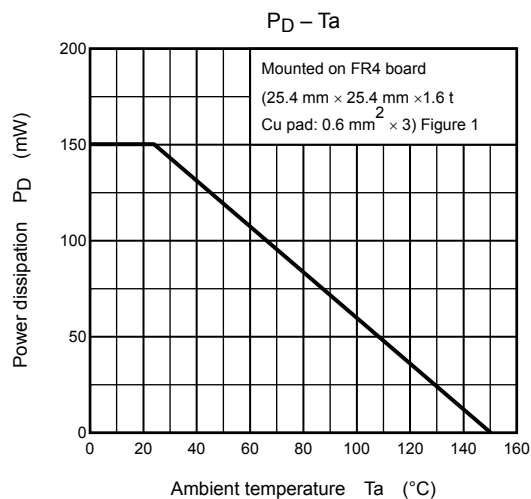
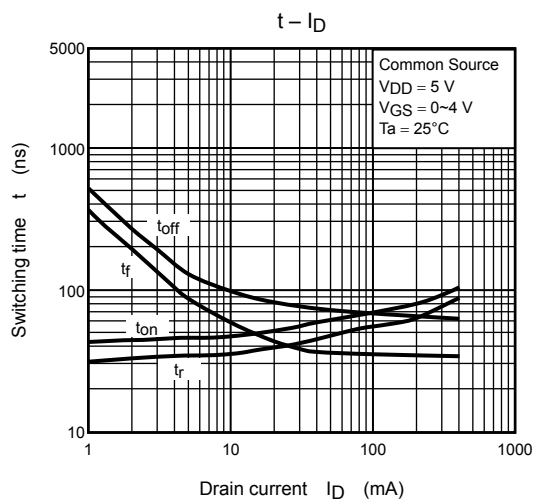
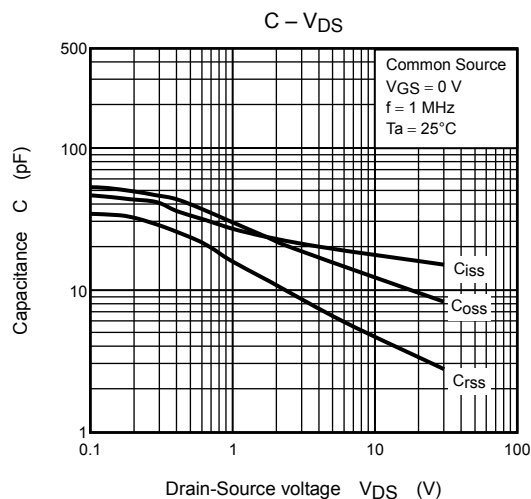
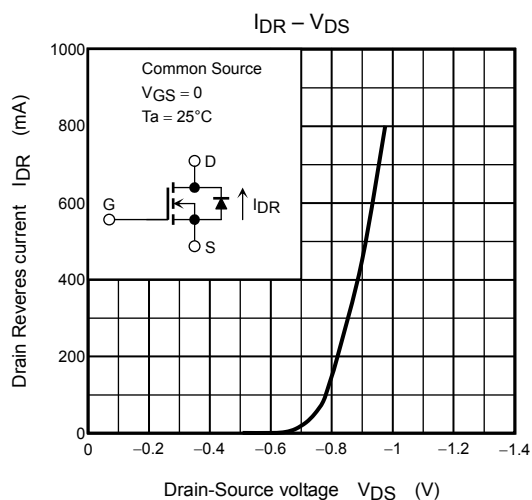
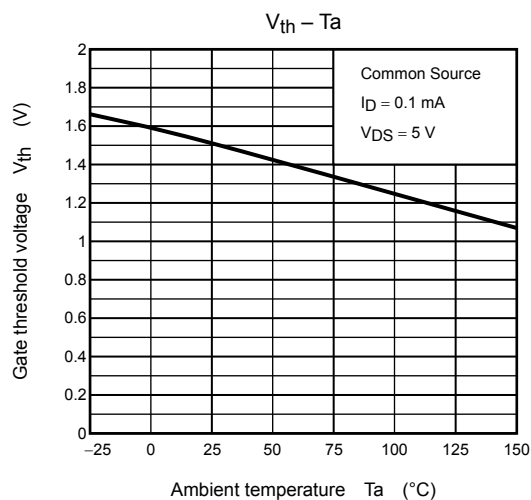
Precaution

V_{th} can be expressed as voltage between gate and source when low operating current value is $I_D = 100 \mu\text{A}$ for this product. For normal switching operation, $V_{GS(on)}$ requires higher voltage than V_{th} and $V_{GS(off)}$ requires lower voltage than V_{th} .

(relationship can be established as follows: $V_{GS(off)} < V_{th} < V_{GS(on)}$)

Please take this into consideration for using the device.





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