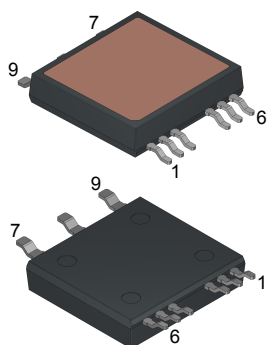
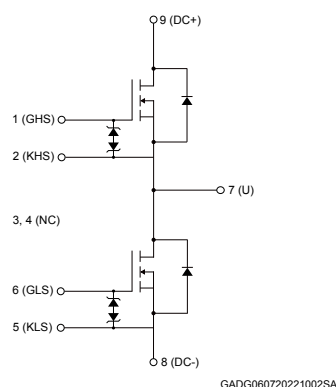


Automotive-grade N-channel 650 V, 56 mΩ typ., 53 A MDmesh DM6 half-bridge topology Power MOSFET in an ACEPACK SMIT package



ACEPACK SMIT



Features

Order code	V _{DS}	R _{DS(on)} max.	I _D
SH63N65DM6AG	650 V	64 mΩ	53 A

- AQG 324 qualified 
- Half-bridge power module
- 650 V blocking voltage
- Fast recovery body diode
- Very low switching energies
- Low package inductance
- Dice on direct bond copper (DBC) substrate
- Low thermal resistance
- Isolation rating of 3.4 kVrms/min

Applications

- Switching applications

Description

This device combines two MOSFETs in a half-bridge topology. The ACEPACK SMIT is a very compact and rugged power module in a surface mount package for easy assembly. Thanks to the DBC substrate, the ACEPACK SMIT package offers low thermal resistance coupled with an isolated top-side thermal pad. The high design flexibility of the package enables several configurations, including phase legs, boost, and single switch through different combinations of the internal power switches.



Product status link

[SH63N65DM6AG](#)

Product summary

Order code	SH63N65DM6AG
Marking	H63N65DM6
Package	ACEPACK SMIT
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 25	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	53	A
	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	33	
$I_{DM}^{(1)}$	Drain current (pulsed)	170	A
P_{TOT}	Total power dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	424	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	100	V/ns
$di/dt^{(2)}$	Peak diode recovery current slope	1000	A/ μ s
$dv/dt^{(3)}$	MOSFET dv/dt ruggedness	100	V/ns
V_{ISO}	Isolation withstand voltage applied between each pin and heat sink plate (AC voltage 50/60 Hz, $t = 60\text{ s}$)	3.4	kVrms
T_{STG}	Storage temperature range	-55 to 150	$^{\circ}\text{C}$
T_J	Operating junction temperature range		$^{\circ}\text{C}$

1. Pulse width limited by safe operating area.
2. $I_{SD} \leq 53\text{ A}$, $V_{DS}(\text{peak}) < V_{(BR)DSS}$, $V_{DD} = 400\text{ V}$.
3. $V_{DS} \leq 520\text{ V}$.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance, junction-to-case	0.29	$^{\circ}\text{C/W}$

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (t_p limited by T_J max.)	6	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ }^{\circ}\text{C}$, $I_D = I_{AR}$)	778	mJ

2 Electrical characteristics

$T_C = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 1\text{ mA}$	650			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 650\text{ V}$			5	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 650\text{ V}$, $T_C^{(1)}$			300	
I_{GSS}	Gate-body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 25\text{ V}$			± 5	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	3.25	4	4.75	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$, $I_D = 23\text{ A}$		56	64	m Ω

1. Specified by design, not tested in production.

Table 5. Dynamic characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	3344	-	pF
C_{oss}	Output capacitance		-	161	-	pF
C_{rss}	Reverse transfer capacitance		-	0.4	-	pF
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{DS} = 0\text{ to }520\text{ V}$, $V_{GS} = 0\text{ V}$	-	510	-	pF
R_G	Intrinsic gate resistance	$f = 1\text{ MHz}$, $I_D = 0\text{ A}$	-	1.4	-	Ω
Q_g	Total gate charge	$V_{DD} = 520\text{ V}$, $I_D = 50\text{ A}$, $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 13. Test circuit for gate charge behavior)	-	80	-	nC
Q_{gs}	Gate-source charge		-	21.5	-	nC
Q_{gd}	Gate-drain charge		-	36	-	nC

1. $C_{oss\text{ eq}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

Table 6. Switching characteristics (resistive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 325\text{ V}$, $I_D = 23\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$	-	28	-	ns
t_r	Rise time		-	8	-	ns
$t_{d(off)}$	Turn-off delay time	(see Figure 12. Switching times test circuit for resistive load and Figure 17. Switching time waveform)	-	68	-	ns
t_f	Fall time		-	8	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		53	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		170	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$, $I_{SD} = 46\text{ A}$	-		1.55	V
t_{rr}	Reverse recovery time	$I_{SD} = 46\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$ (see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	162		ns
Q_{rr}	Reverse recovery charge		-	0.95		μC
I_{RRM}	Reverse recovery current		-	10.7		A
t_{rr}	Reverse recovery time	$I_{SD} = 46\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$, $T_J = 150\text{ }^\circ\text{C}$ (see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	355		ns
Q_{rr}	Reverse recovery charge		-	4.8		μC
I_{RRM}	Reverse recovery current		-	25.3		A

1. Pulse width is limited by safe operating area.
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

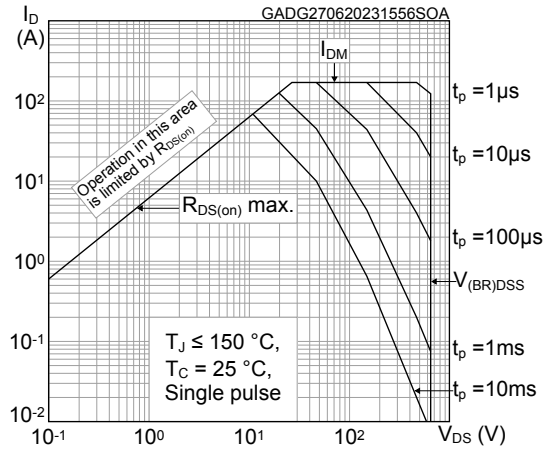


Figure 2. Maximum transient thermal impedance

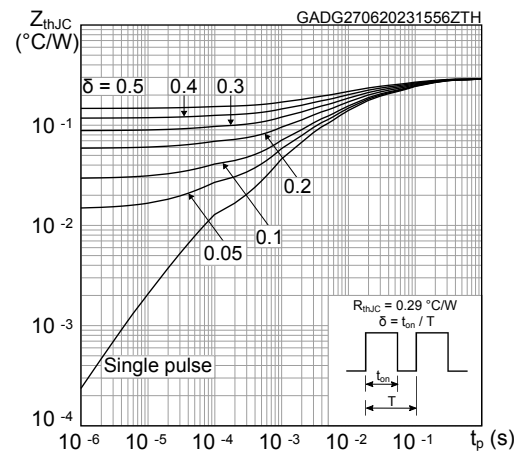


Figure 3. Typical output characteristics

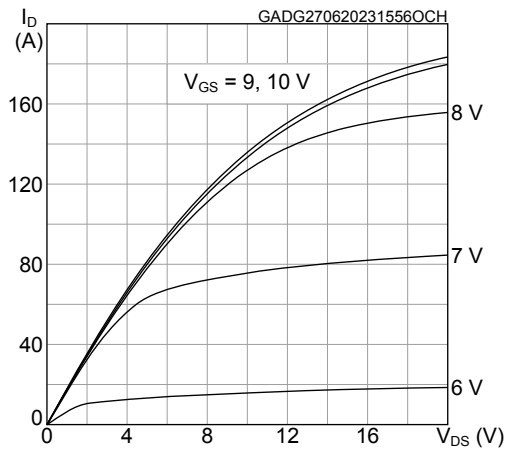


Figure 4. Typical transfer characteristics

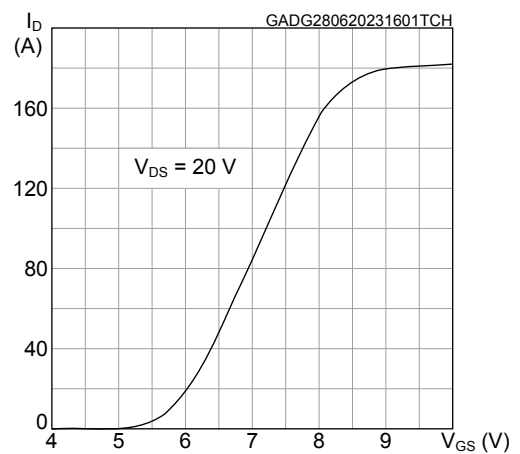


Figure 5. Typical drain-source on-resistance

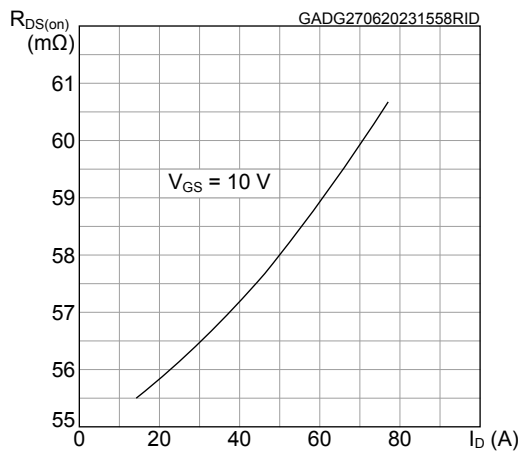


Figure 6. Typical gate charge characteristics

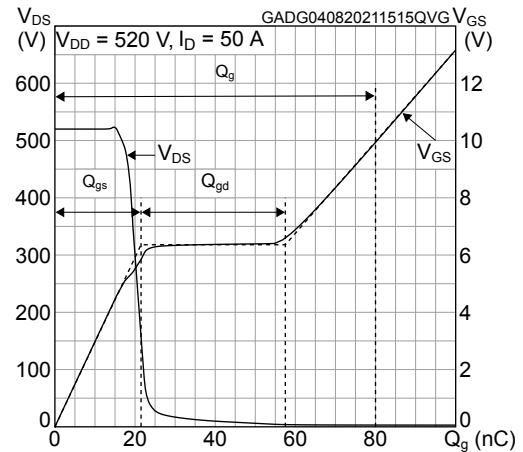


Figure 7. Typical capacitance characteristics

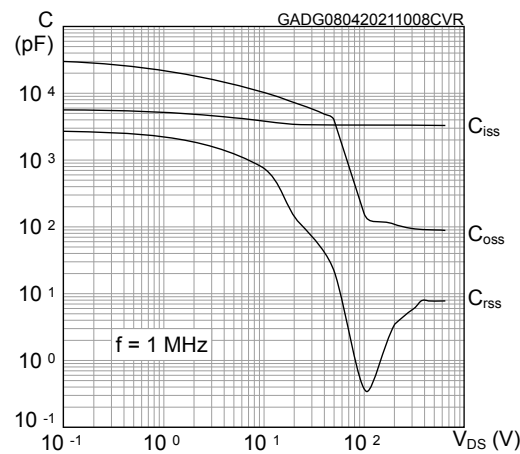


Figure 8. Normalized gate threshold vs temperature

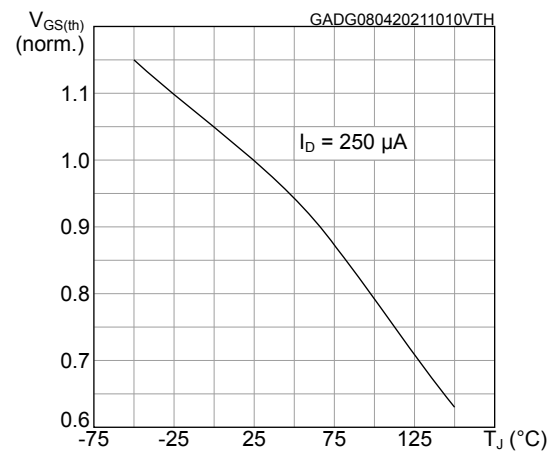


Figure 9. Normalized on-resistance vs temperature

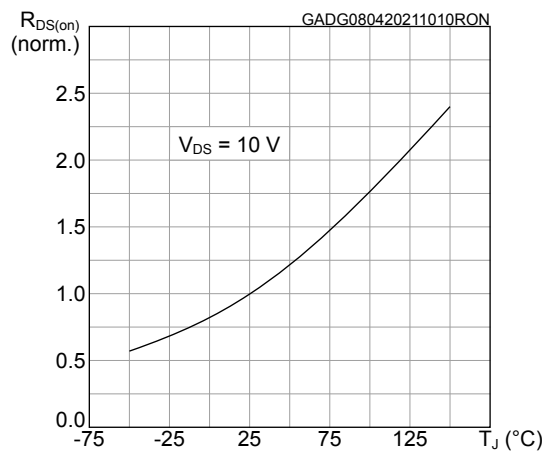


Figure 10. Normalized breakdown voltage vs temperature

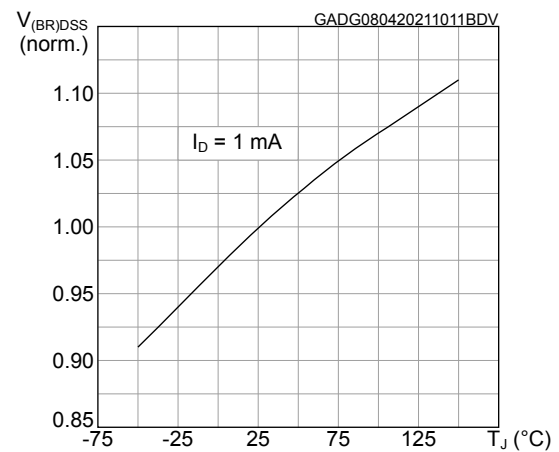
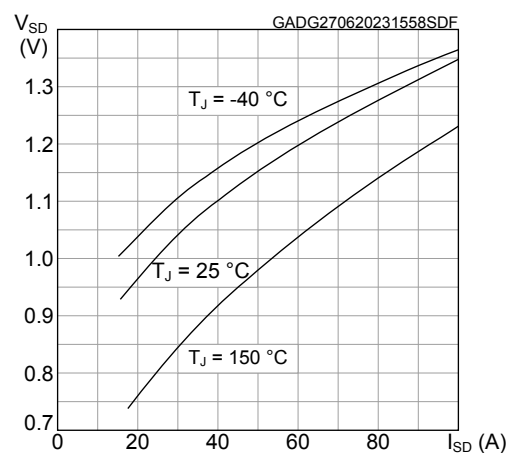
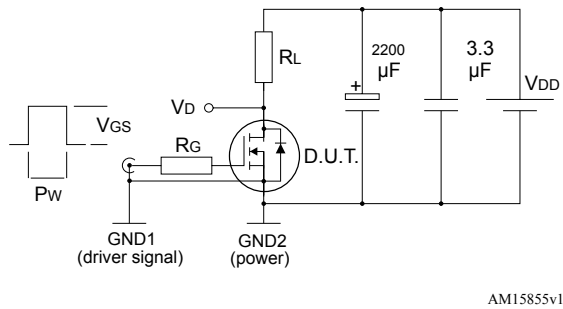
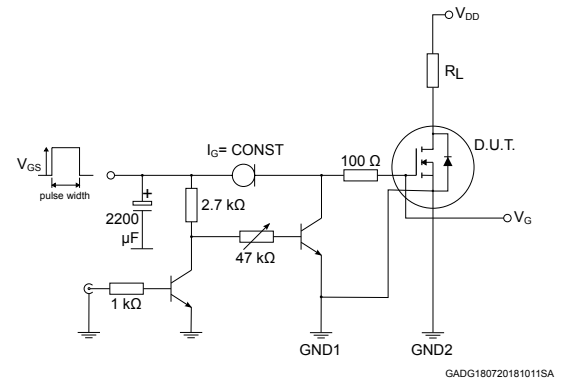
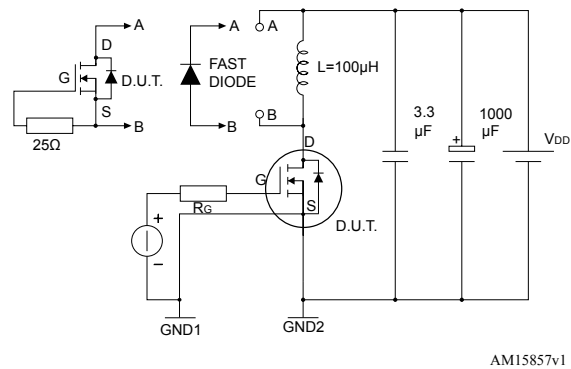
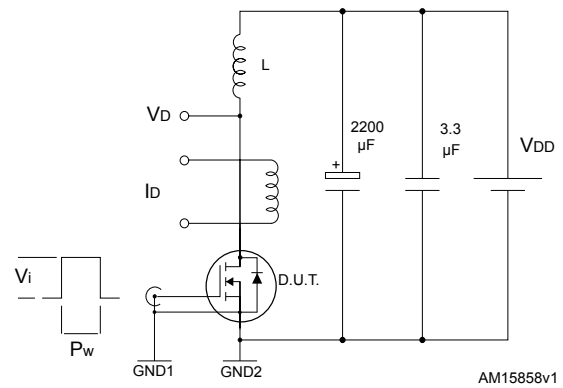
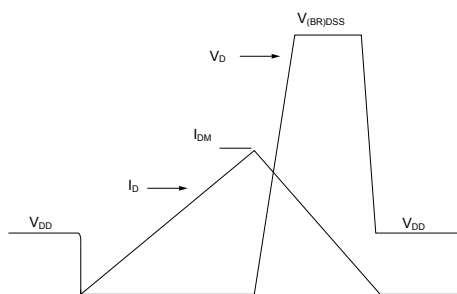
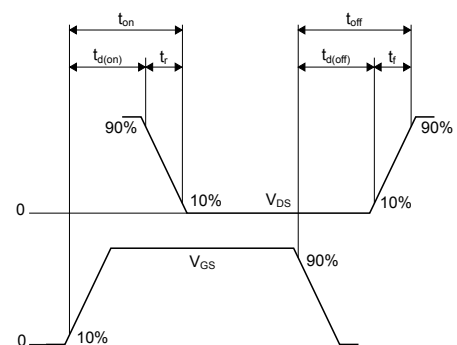


Figure 11. Typical reverse diode forward characteristics



3 Test circuits

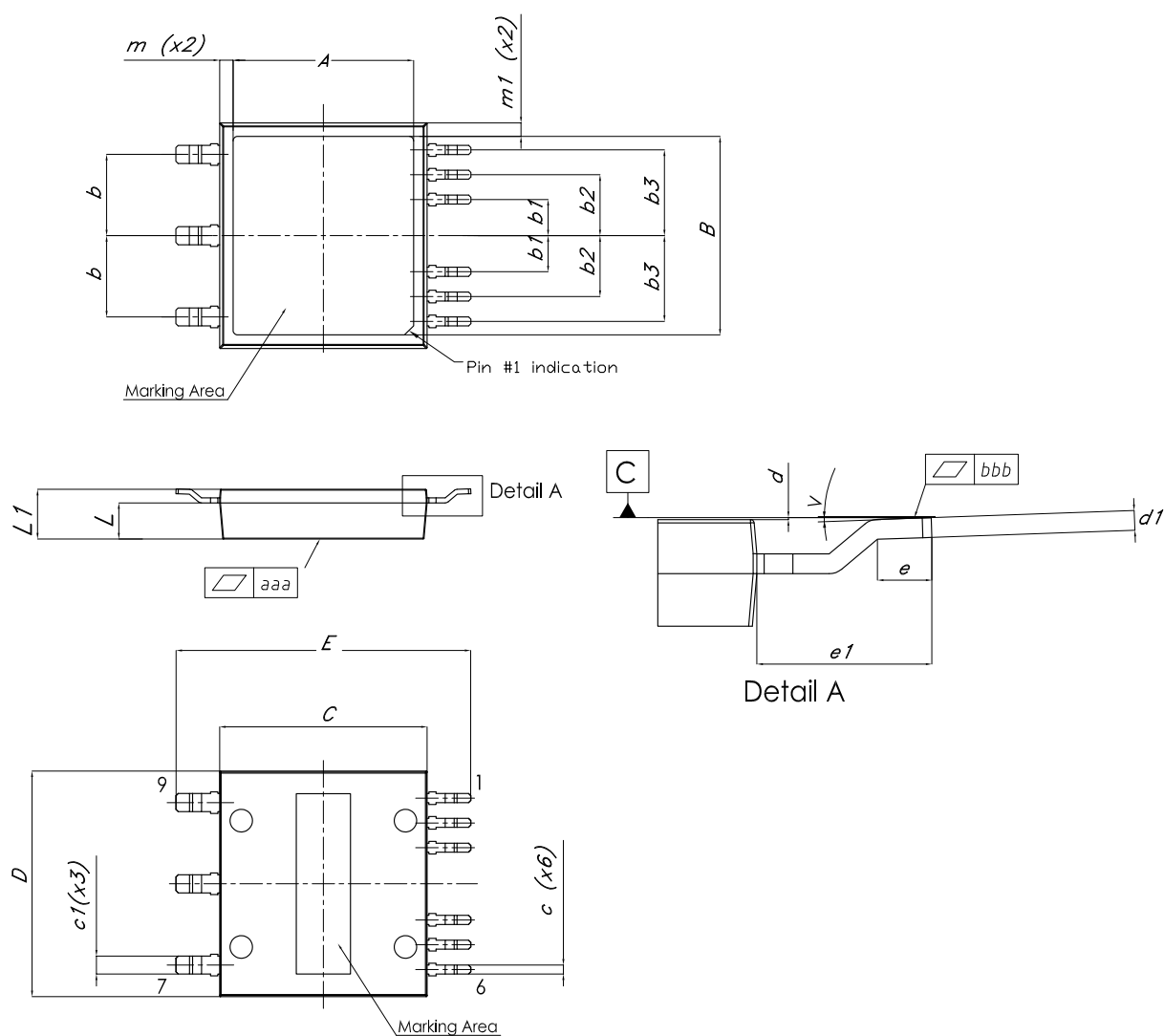
Figure 12. Switching times test circuit for resistive load

Figure 13. Test circuit for gate charge behavior

Figure 14. Test circuit for inductive load switching and diode recovery times

Figure 15. Unclamped inductive load test circuit

Figure 16. Unclamped inductive waveform

Figure 17. Switching time waveform


4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 ACEPACK SMIT package information

Figure 18. ACEPACK SMIT package outline

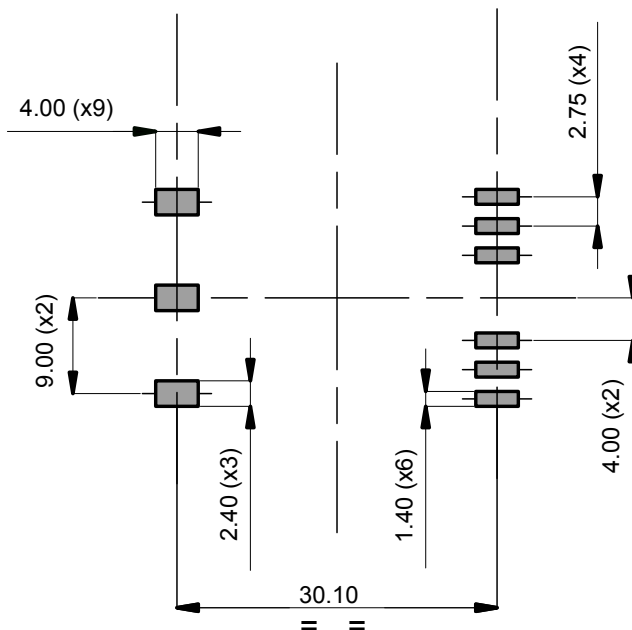


DM00447519_Rev.6

Table 8. ACEPACK SMIT package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	19.50	20.00	20.50
B	21.50	22.00	22.50
C	22.80	23.00	23.20
D	24.80	25.00	25.20
E	32.20	32.70	33.20
b		9.00	
b1		4.00	
b2		6.75	
b3		9.50	
c	0.95	1.00	1.10
c1	1.95	2.00	2.10
d	0.00		0.15
d1	0.45	0.55	0.65
e	1.30	1.50	1.70
e1	4.65	4.85	5.05
L	3.95	4.00	4.05
L1	5.40	5.50	5.60
m	1.30	1.50	1.80
m1	1.30	1.50	1.80
V	0°	2°	4°
aaa	0.01		0.05
bbb	0.00		0.10

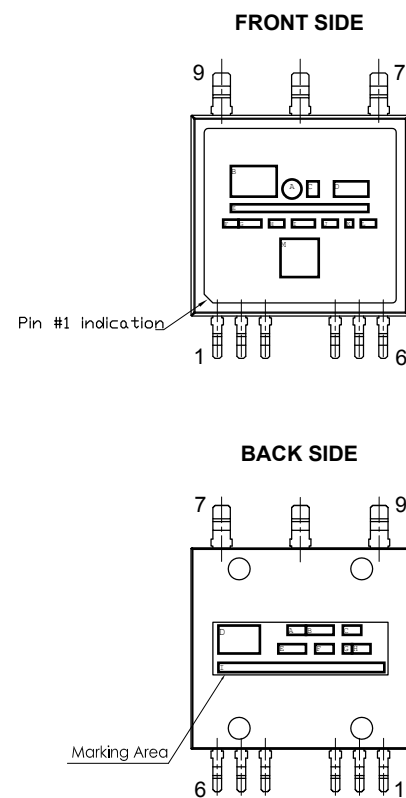
Figure 19. ACEPACK SMIT recommended footprint



DM00447519_FP_Rev.6

Note: Dimensions in mm.

Figure 20. ACEPACK SMIT marking orientation vs pinout



DM00447519_MO_Rev.6

Revision history

Table 9. Document revision history

Date	Revision	Changes
29-Jun-2023	1	First release.

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