



PSMN7R2-100YSF

NextPower 100 V, 6.9 mOhm N-channel MOSFET in LPAK56 package

20 June 2023

Product data sheet

1. General description

NextPower 100 V, standard level gate drive MOSFET. Qualified to 175 °C and recommended for industrial and consumer applications.

2. Features and benefits

- Low Q_{rr} for higher efficiency and lower spiking
- Low $Q_G \times R_{DS(on)}$ FOM for high efficiency switching applications
- Strong avalanche energy rating (E_{AS})
- Avalanche rated and 100% tested
- Ha-free and RoHS compliant LPAK56 package
- Wave-solderable LPAK56 package

3. Applications

- Synchronous rectifier in AC-DC and DC-DC
- Primary side switch in 48 V DC-DC
- BLDC motor control
- USB-PD and mobile fast-charge adapters
- Flyback and resonant topologies

4. Quick reference data

Table 1. Quick reference data

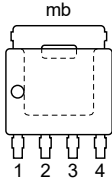
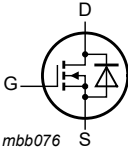
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V _{DS}	drain-source voltage	25 °C ≤ T _j ≤ 175 °C		-	-	100	V
I _D	drain current	V _{GS} = 10 V; T _{mb} = 25 °C; Fig. 2		-	-	111	A
P _{tot}	total power dissipation	T _{mb} = 25 °C; Fig. 1		-	-	194	W
T _j	junction temperature			-55	-	175	°C
Static characteristics							
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 25 A; T _j = 25 °C; Fig. 12		-	5.7	6.9	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _j = 100 °C; Fig. 13		-	8.9	11	mΩ
Dynamic characteristics							
Q _{GD}	gate-drain charge	I _D = 25 A; V _{DS} = 50 V; V _{GS} = 10 V; T _j = 25 °C; Fig. 14 ; Fig. 15		3	10	23	nC
Q _{G(tot)}	total gate charge			25	50	75	nC
Avalanche ruggedness							
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I _D = 38 A; V _{sup} ≤ 100 V; R _{GS} = 50 Ω; V _{GS} = 10 V; T _{j(i nit)} = 25 °C; unclamped; t _p = 70 μs; Fig. 4	[1]	-	-	173	mJ

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Source-drain diode						
Q _r	recovered charge	I _S = 25 A; dI _S /dt = -100 A/μs; V _{GS} = 0 V; V _{DS} = 50 V; T _J = 25 °C; Fig. 18	-	23	-	nC

[1] Protected by 100% test

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 LPAK56; Power-SO8 (SOT669)	 <i>mbb076</i>
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN7R2-100YSF	LPAK56; Power-SO8	plastic, single-ended surface-mounted package; 4 terminals	SOT669

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN7R2-100YSF	7F2S10Y

8. Limiting values

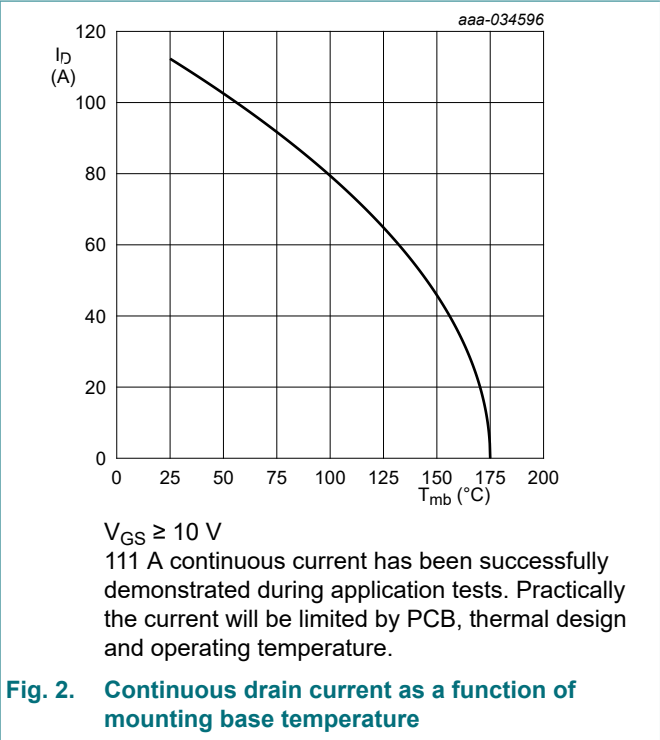
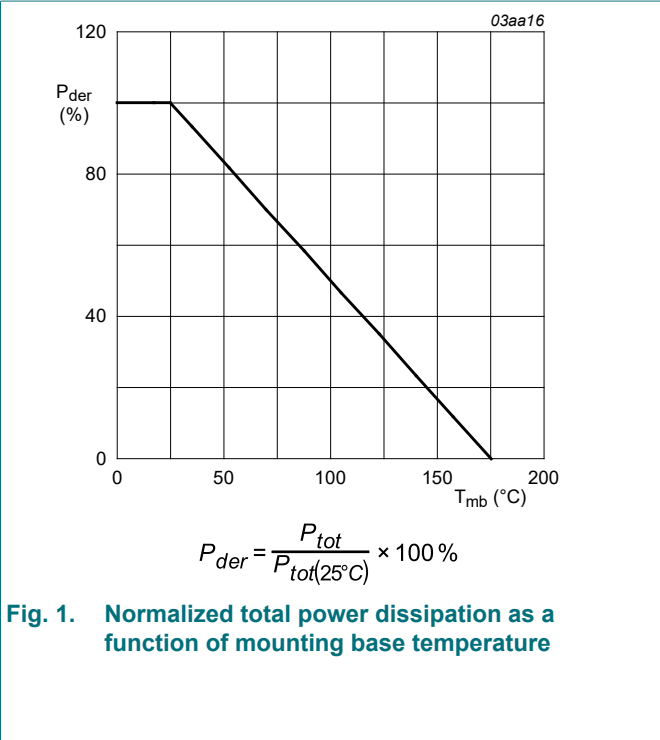
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). T_J = 25 °C unless otherwise stated.

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DS}	drain-source voltage	25 °C ≤ T _J ≤ 175 °C	-	100	V
V _{DGR}	drain-gate voltage	25 °C ≤ T _J ≤ 175 °C; R _{GS} = 20 kΩ	-	100	V
V _{GS}	gate-source voltage		-20	20	V
P _{tot}	total power dissipation	T _{mb} = 25 °C; Fig. 1	-	194	W
I _D	drain current	V _{GS} = 10 V; T _{mb} = 25 °C; Fig. 2	-	111	A
		V _{GS} = 10 V; T _{mb} = 100 °C; Fig. 2	-	78	A
I _{DM}	peak drain current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C; Fig. 3	-	443	A
T _{stg}	storage temperature		-55	175	°C
T _J	junction temperature		-55	175	°C

Symbol	Parameter	Conditions		Min	Max	Unit
T _{slid(M)}	peak soldering temperature			-	260	°C
Source-drain diode						
I _S	source current	T _{mb} = 25 °C		-	111	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C		-	443	A
Avalanche ruggedness						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I _D = 38 A; V _{sup} ≤ 100 V; R _{GS} = 50 Ω; V _{GS} = 10 V; T _{j(init)} = 25 °C; unclamped; t _p = 70 μs; Fig. 4	[1]	-	173	mJ
I _{AS}	non-repetitive avalanche current	V _{sup} ≤ 100 V; V _{GS} = 10 V; T _{j(init)} = 25 °C; R _{GS} = 50 Ω; Fig. 4	[1]	-	38	A

[1] Protected by 100% test



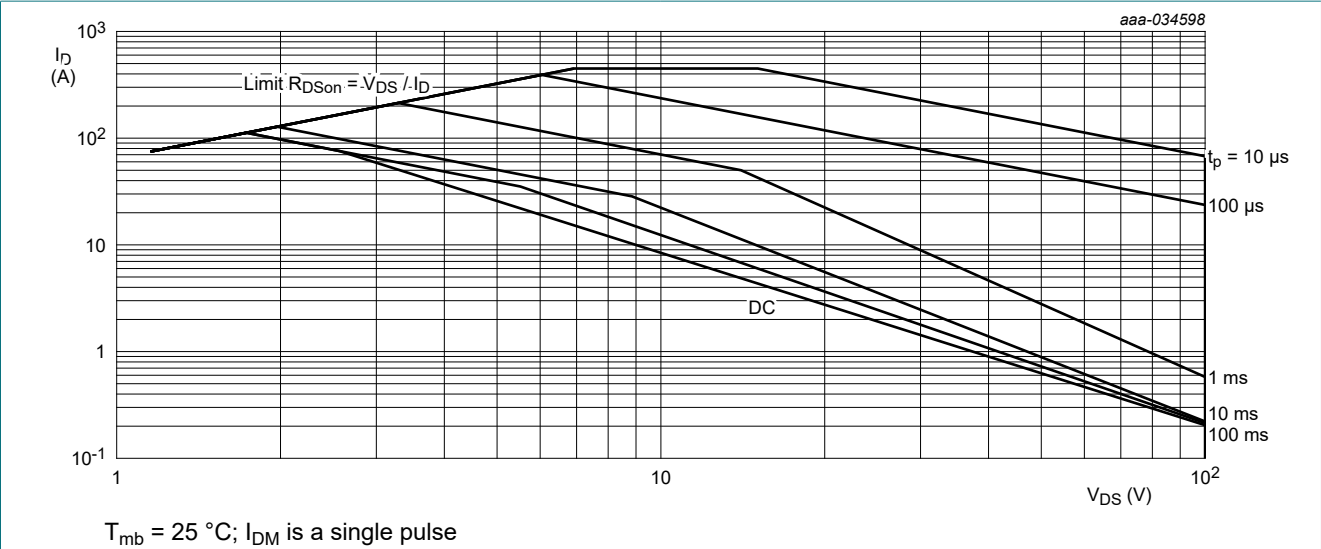


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

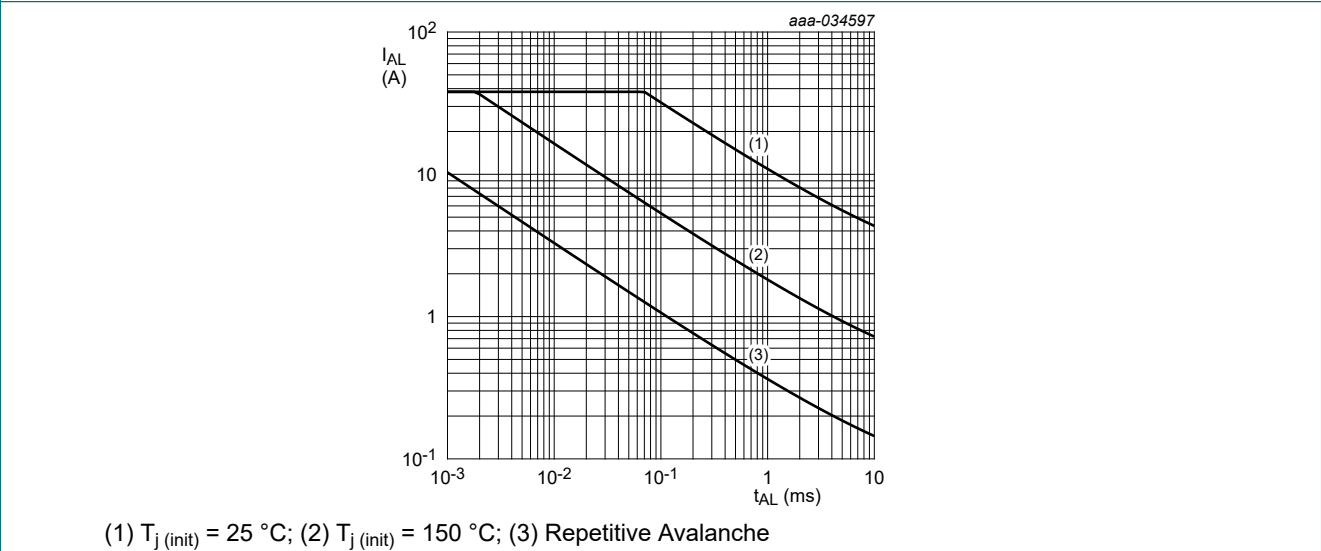


Fig. 4. Avalanche rating; avalanche current as a function of avalanche time

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	0.69	0.77	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Fig. 6	-	42	-	K/W
		Fig. 7	-	85	-	K/W

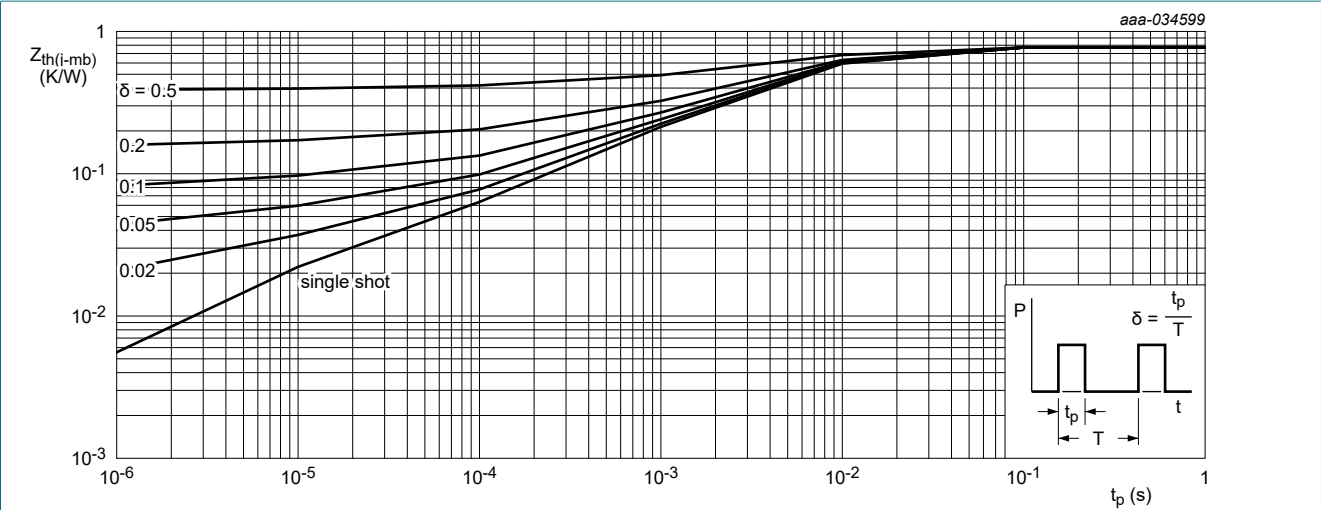
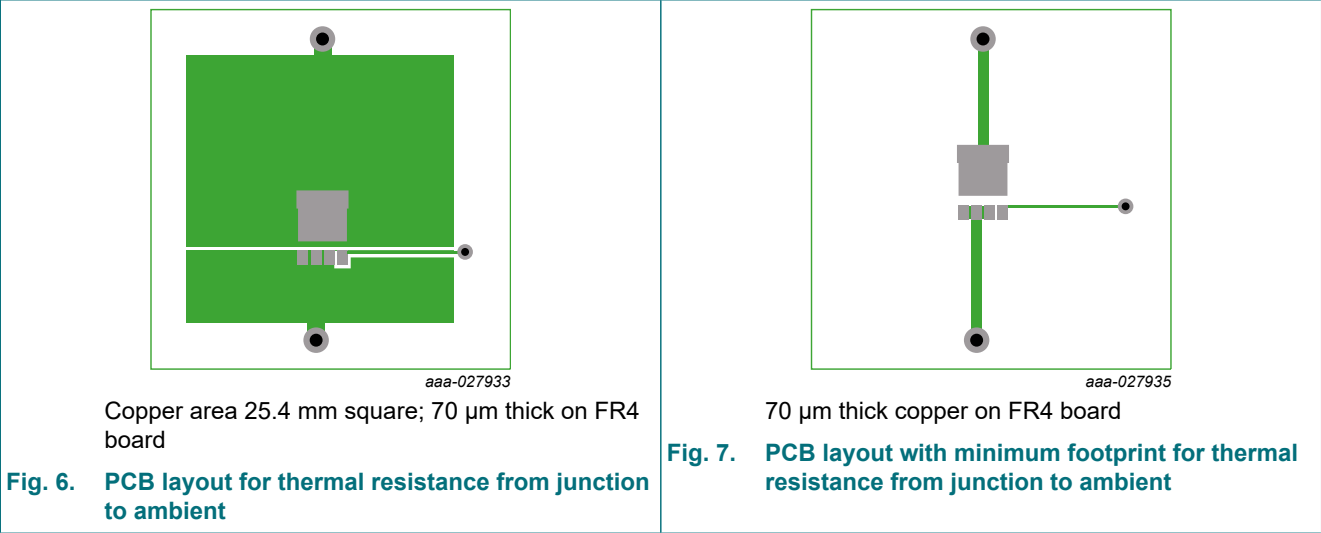


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration



10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 250 μA; V _{GS} = 0 V; T _J = 25 °C	100	-	-	V
		I _D = 250 μA; V _{GS} = 0 V; T _J = -55 °C	90	-	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} =V _{GS} ; T _J = 25 °C; Fig. 11	2	3	4	V
		I _D = 1 mA; V _{DS} =V _{GS} ; T _J = 175 °C	-	1.7	-	V
		I _D = 1 mA; V _{DS} =V _{GS} ; T _J = -55 °C	-	3.4	-	V
ΔV _{GS(th)} /ΔT	gate-source threshold voltage variation with temperature	25 °C ≤ T _J ≤ 150 °C	-	-7.5	-	mV/K
I _{DSS}	drain leakage current	V _{DS} = 100 V; V _{GS} = 0 V; T _J = 25 °C	-	0.02	1	μA
		V _{DS} = 100 V; V _{GS} = 0 V; T _J = 125 °C	-	8	100	μA
I _{GSS}	gate leakage current	V _{GS} = 20 V; V _{DS} = 0 V; T _J = 25 °C	-	2	100	nA
		V _{GS} = -20 V; V _{DS} = 0 V; T _J = 25 °C	-	2	100	nA

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 25 A; T _j = 25 °C; Fig. 12		-	5.7	6.9	mΩ
		V _{GS} = 7 V; I _D = 25 A; T _j = 25 °C; Fig. 12		-	6.8	10.4	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _j = 100 °C; Fig. 13		-	8.9	11	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _j = 175 °C; Fig. 13		-	12.7	15.7	mΩ
R _G	gate resistance	f = 1 MHz; T _j = 25 °C		0.9	1.8	3.6	Ω
Dynamic characteristics							
Q _{G(tot)}	total gate charge	I _D = 25 A; V _{DS} = 50 V; V _{GS} = 10 V; T _j = 25 °C; Fig. 14 ; Fig. 15		25	50	75	nC
		I _D = 0 A; V _{DS} = 0 V; V _{GS} = 10 V; T _j = 25 °C		-	25.6	-	nC
Q _{GS}	gate-source charge	I _D = 25 A; V _{DS} = 50 V; V _{GS} = 10 V; T _j = 25 °C; Fig. 14 ; Fig. 15		9	15	21	nC
Q _{GS(th)}	pre-threshold gate-source charge			-	9.7	-	nC
Q _{GS(th-pl)}	post-threshold gate-source charge			-	5.6	-	nC
Q _{GD}	gate-drain charge			3	10	23	nC
V _{GS(pl)}	gate-source plateau voltage	I _D = 25 A; V _{DS} = 50 V; T _j = 25 °C; Fig. 14 ; Fig. 15		-	4.6	-	V
C _{iss}	input capacitance	V _{DS} = 50 V; V _{GS} = 0 V; f = 1 MHz; T _j = 25 °C; Fig. 16		2065	3442	4818	pF
C _{oss}	output capacitance			535	893	1428	pF
C _{rss}	reverse transfer capacitance			2.5	24.7	64	pF
t _{d(on)}	turn-on delay time	V _{DS} = 50 V; R _L = 2 Ω; V _{GS} = 10 V; R _{G(ext)} = 5 Ω; T _j = 25 °C		-	14	-	ns
t _r	rise time			-	15	-	ns
t _{d(off)}	turn-off delay time			-	34	-	ns
t _f	fall time			-	18	-	ns
Source-drain diode							
V _{SD}	source-drain voltage	I _S = 25 A; V _{GS} = 0 V; T _j = 25 °C; Fig. 17		-	0.83	1	V
t _{rr}	reverse recovery time	I _S = 25 A; dI _S /dt = -100 A/μs; V _{GS} = 0 V; V _{DS} = 50 V; T _j = 25 °C; Fig. 18		-	32	-	ns
Q _r	recovered charge			-	23	-	nC

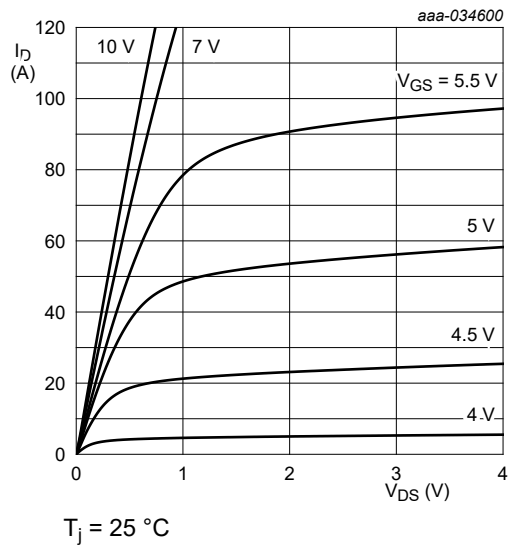


Fig. 8. Output characteristics; drain current as a function of drain-source voltage; typical values

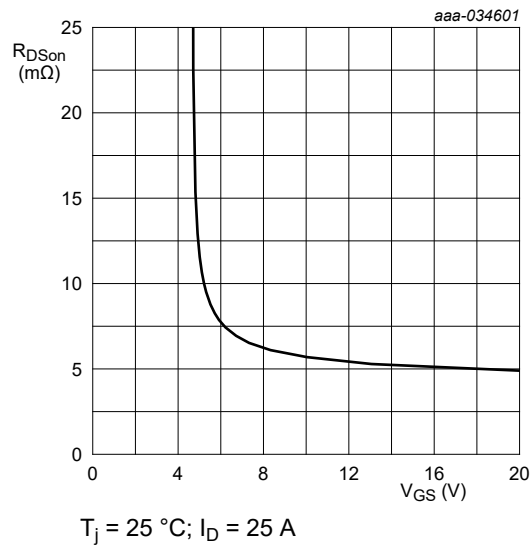


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

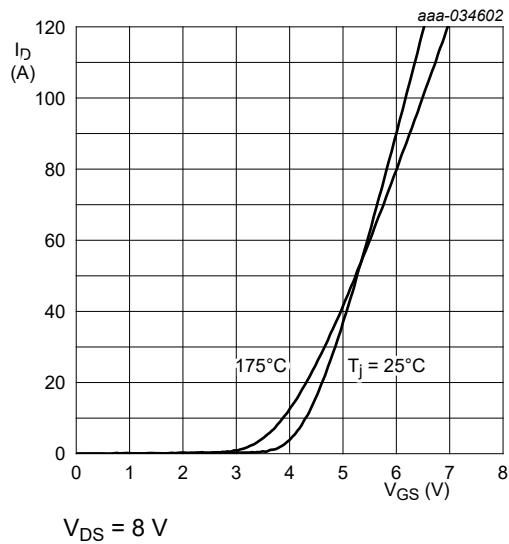


Fig. 10. Transfer characteristics; drain current as a function of gate-source voltage; typical values

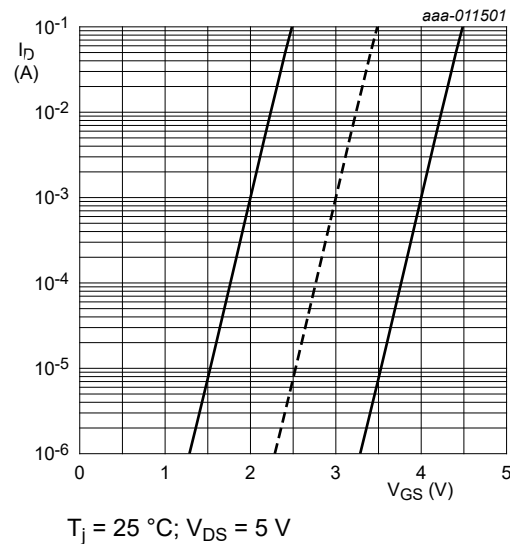


Fig. 11. Sub-threshold drain current as a function of gate-source voltage

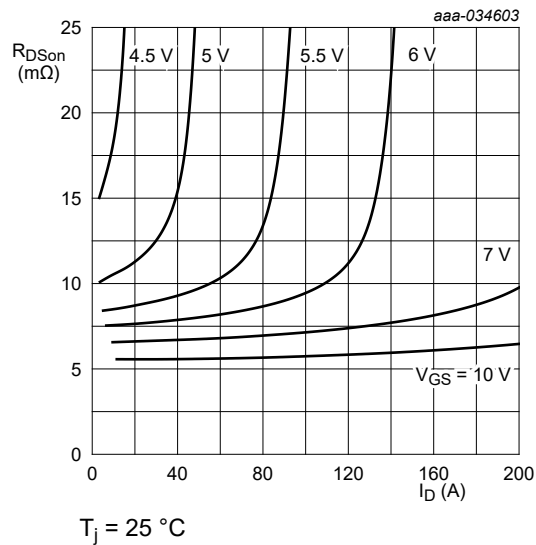


Fig. 12. Drain-source on-state resistance as a function of drain current; typical values

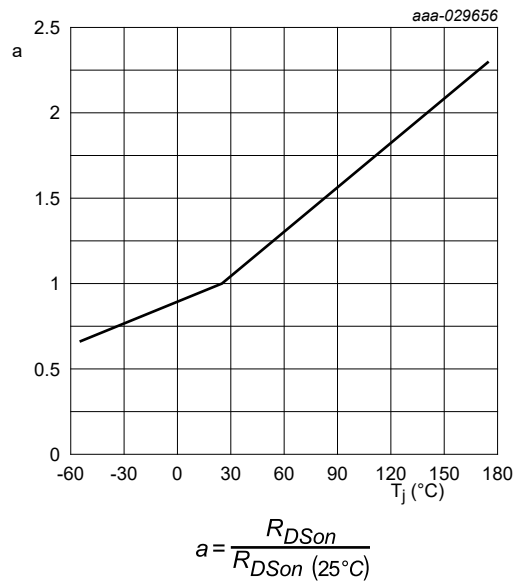


Fig. 13. Normalized drain-source on-state resistance factor as a function of junction temperature

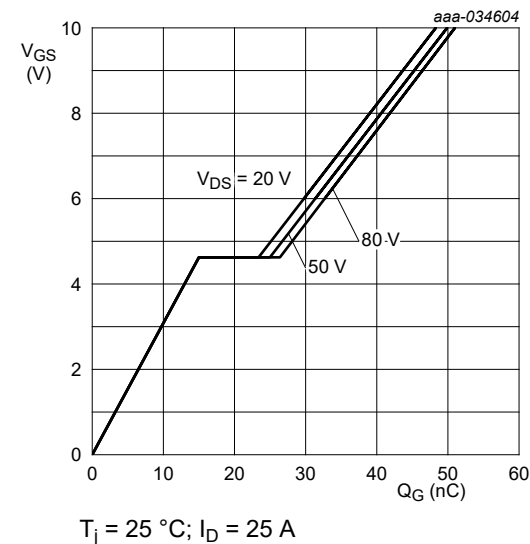


Fig. 14. Gate-source voltage as a function of gate charge; typical values

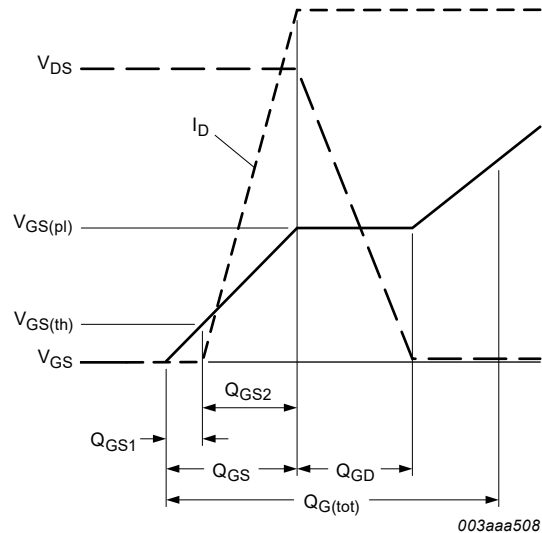


Fig. 15. Gate charge waveform definitions

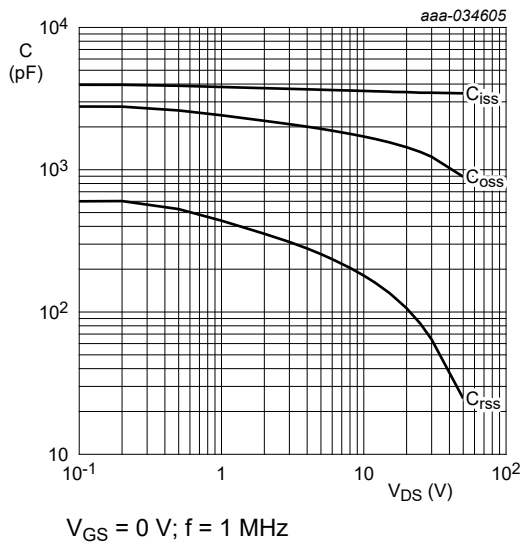


Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

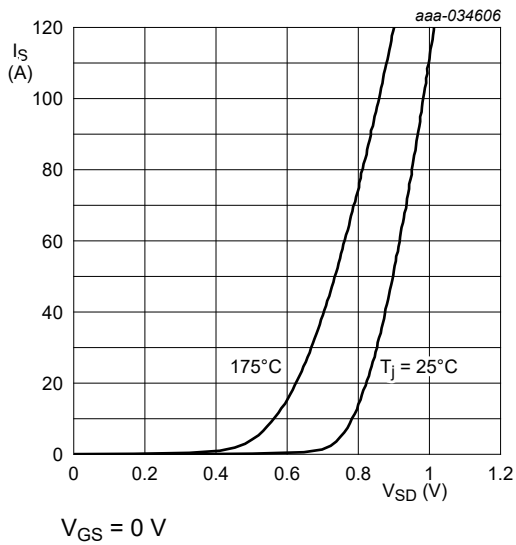


Fig. 17. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

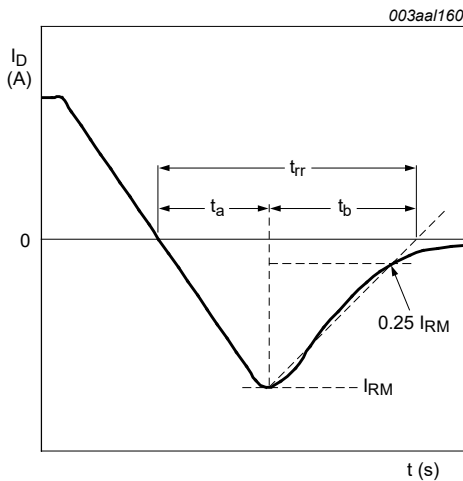


Fig. 18. Reverse recovery timing definition

11. Package outline

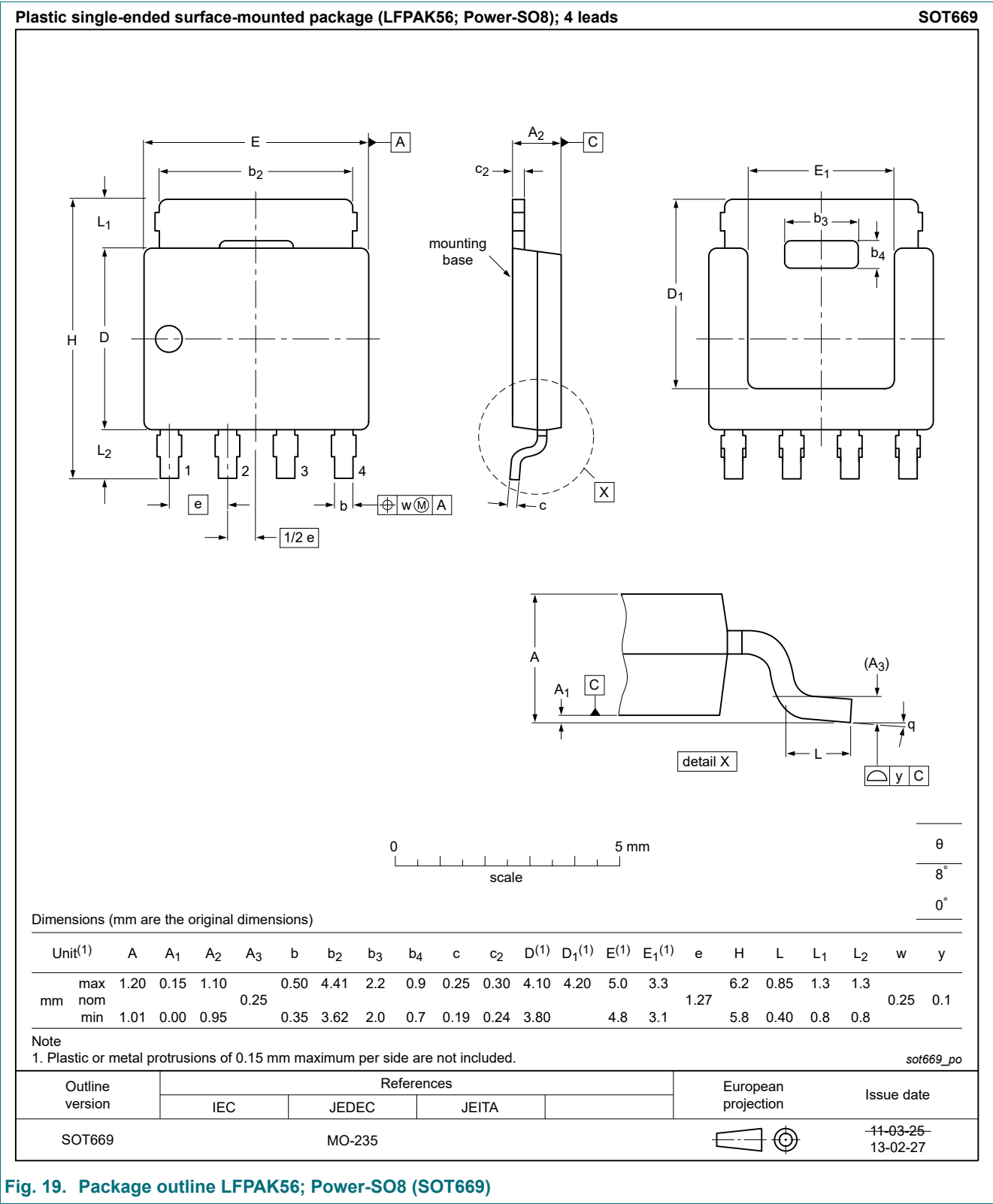


Fig. 19. Package outline LPAK56; Power-SO8 (SOT669)

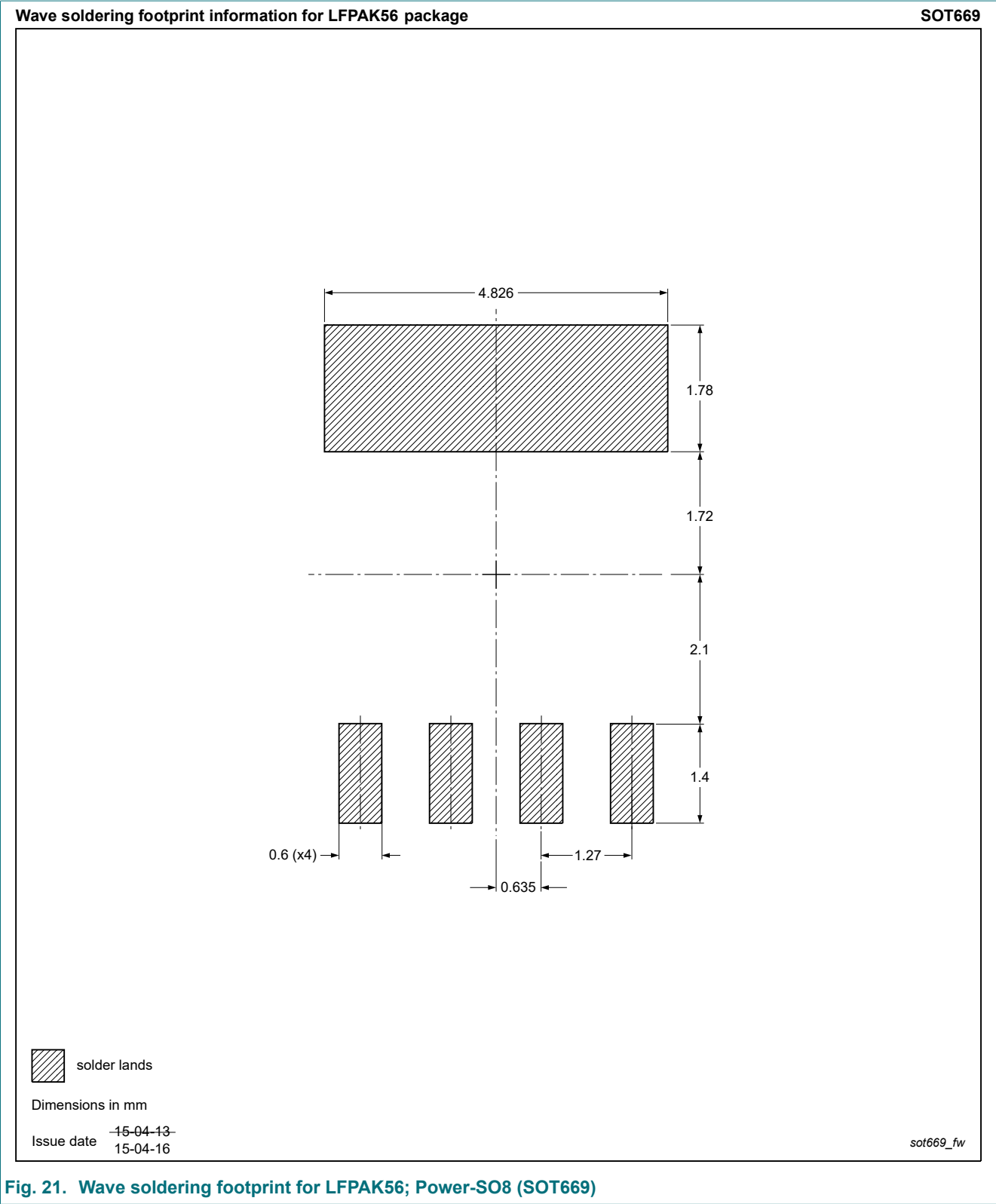


Fig. 21. Wave soldering footprint for LPAK56; Power-SO8 (SOT669)

13. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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