



PSMN1R4-40YSH

N-channel 40 V, 1.4 mOhm, 240 A standard level MOSFET in LPAK56 using NextPower-S3 Schottky-Plus technology

18 October 2023

Product data sheet

1. General description

240 A, standard level gate drive N-channel enhancement mode MOSFET in 175 °C LPAK56 package using advanced TrenchMOS Superjunction technology. This product has been designed and qualified for high performance power switching applications.

2. Features and benefits

- 240 A continuous $I_{D(max)}$ rating
- Avalanche rated, 100% tested at $I_{AS} = 190$ A
- Strong SOA (linear-mode) rating
- NextPower-S3 technology delivers 'superfast switching with soft body-diode recovery'
- Low Q_{RR} , Q_G and Q_{GD} for high system efficiency and low EMI designs
- Schottky-Plus body-diode with low V_{SD} , low Q_{RR} , soft recovery and low I_{DSS} leakage
- High reliability LPAK (Power SO8) package, with copper-clip and solder die attach, qualified to 175 °C
- Exposed leads can be wave soldered, visual solder joint inspection and high quality solder joints
- Low parasitic inductance and resistance

3. Applications

- High-performance synchronous rectification
- DC-to-DC converters
- High performance and high efficiency server power supply
- Brushless DC motor control
- Battery protection
- Load-switch and eFuse
- Inrush management, hotswap

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_J \leq 175\text{ °C}$		-	-	40	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	[1]	-	-	240	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1		-	-	333	W
T_J	junction temperature			-55	-	175	°C
Static characteristics							
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; $T_J = 25\text{ °C}$; Fig. 10		-	1.06	1.4	mΩ

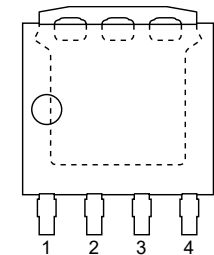
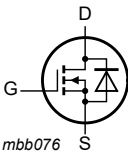
N-channel 40 V, 1.4 mOhm, 240 A standard level MOSFET in LFPAK56 using NextPower-S3 Schottky-Plus technology

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Dynamic characteristics						
Q _{GD}	gate-drain charge	I _D = 25 A; V _{DS} = 20 V; V _{GS} = 10 V;	2.8	9.3	19	nC
Q _{G(tot)}	total gate charge	T _j = 25 °C; Fig. 12; Fig. 13	44	68	96	nC

[1] 240 A Continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 LFPAK56E; Power-SO8 (SOT1023)	 mbb076
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN1R4-40YSH	LFPAK56E; Power-SO8	plastic, single-ended surface-mounted package (LFPAK56); 4 leads; 1.27 mm pitch	SOT1023

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN1R4-40YSH	1H4S40Y

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). T_j = 25 °C unless otherwise stated.

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DS}	drain-source voltage	25 °C ≤ T _j ≤ 175 °C	-	40	V
V _{DSM}	peak drain-source voltage	t _p = 20 ns; f = 500 kHz; E _{DS(AL)} = 200 nJ; pulsed	-	45	V
V _{DGR}	drain-gate voltage	25 °C ≤ T _j ≤ 175 °C; R _{GS} = 20 kΩ	-	40	V
V _{GS}	gate-source voltage		-20	20	V
P _{tot}	total power dissipation	T _{mb} = 25 °C; Fig. 1	-	333	W

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Symbol	Parameter	Conditions		Min	Max	Unit
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	[1]	-	240	A
		$V_{GS} = 10\text{ V}$; $T_{mb} = 100\text{ °C}$; Fig. 2		-	234	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$; Fig. 3		-	1322	A
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C
$T_{sld(M)}$	peak soldering temperature			-	260	°C
Source-drain diode						
I_S	source current	$T_{mb} = 25\text{ °C}$		-	240	A
I_{SM}	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$		-	1322	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 71.2\text{ A}$; $V_{sup} \leq 40\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 10\text{ V}$; $T_{j(init)} = 25\text{ °C}$; unclamped; $t_p = 240\text{ }\mu\text{s}$	[2]	-	445	mJ
		$I_D = 25\text{ A}$; $V_{sup} \leq 40\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 10\text{ V}$; $T_{j(init)} = 25\text{ °C}$; unclamped; $t_p = 2.69\text{ ms}$	[2]	-	1750	mJ
I_{AS}	non-repetitive avalanche current	$V_{sup} \leq 40\text{ V}$; $V_{GS} = 10\text{ V}$; $T_{j(init)} = 25\text{ °C}$; $R_{GS} = 50\text{ }\Omega$	[2]	-	190	A

- [1] 240 A Continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.
 [2] Protected by 100% test

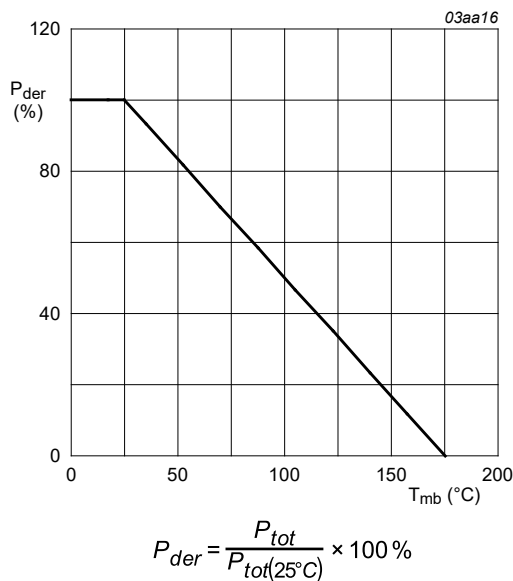
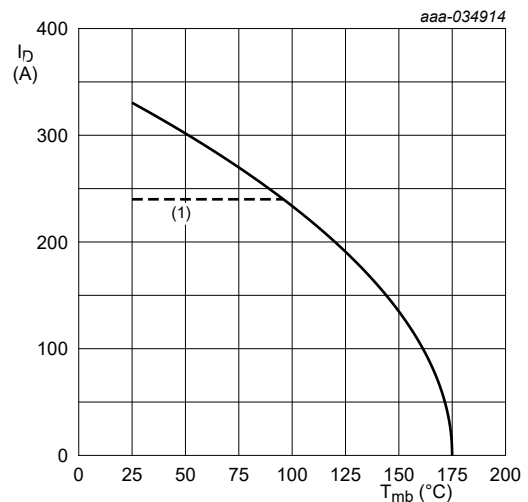


Fig. 1. Normalized total power dissipation as a function of mounting base temperature

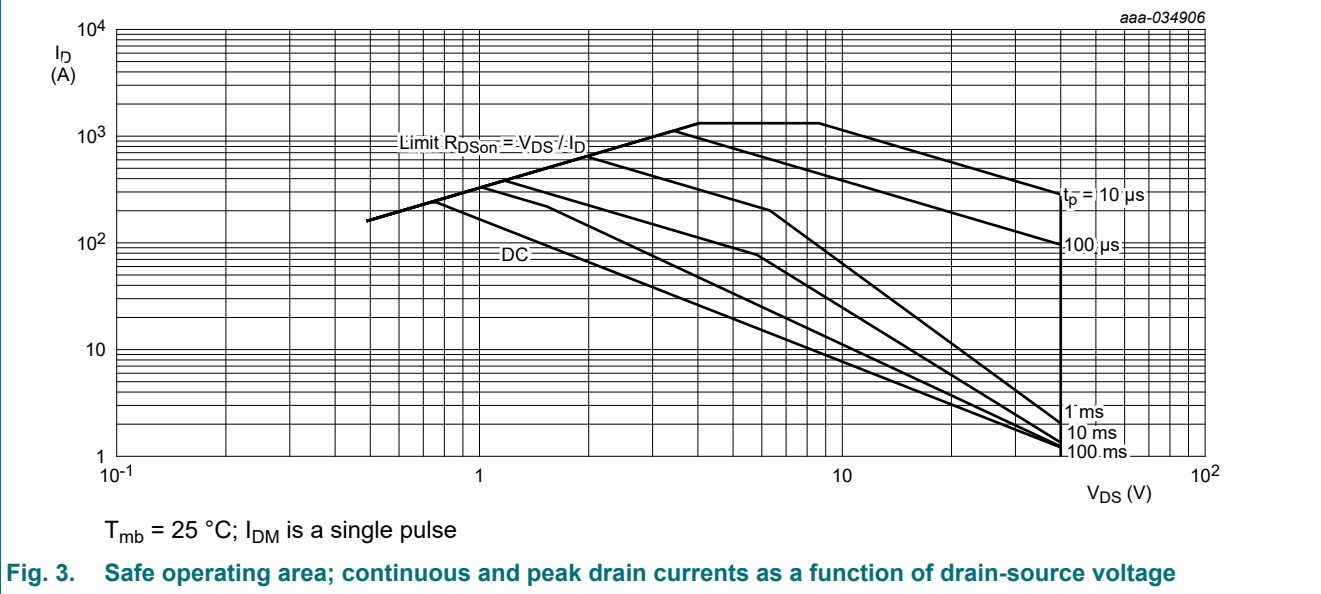


$V_{GS} \geq 10\text{ V}$

(1) 240 A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

Fig. 2. Continuous drain current as a function of mounting base temperature

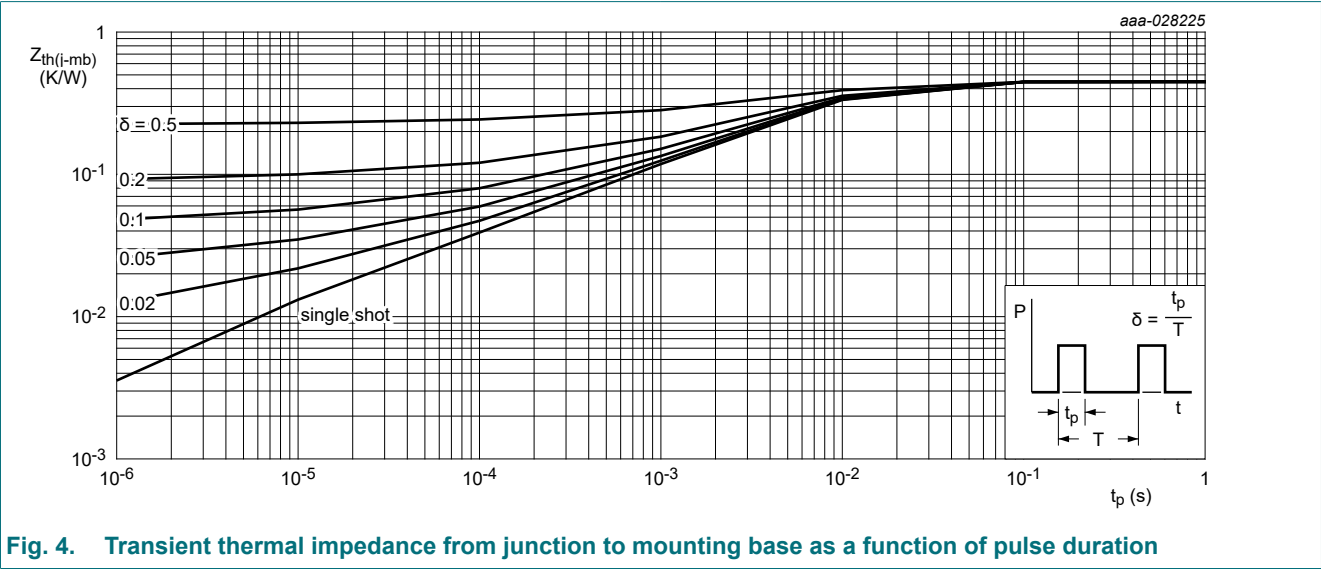
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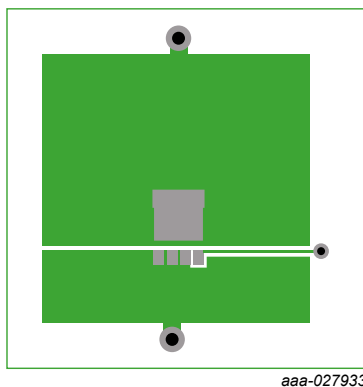
9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 4	-	0.33	0.45	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Fig. 5	-	42	-	K/W
		Fig. 6	-	85	-	K/W

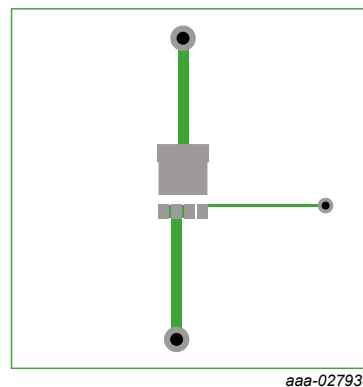


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Copper area 25.4 mm square; 70 μm thick on FR4 board

Fig. 5. PCB layout for thermal resistance from junction to ambient



70 μm thick copper on FR4 board

Fig. 6. PCB layout with minimum footprint for thermal resistance from junction to ambient

10. Characteristics

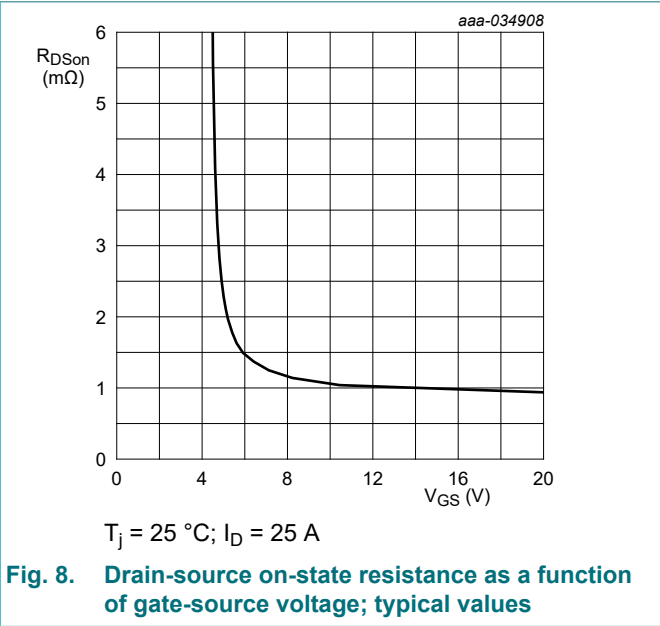
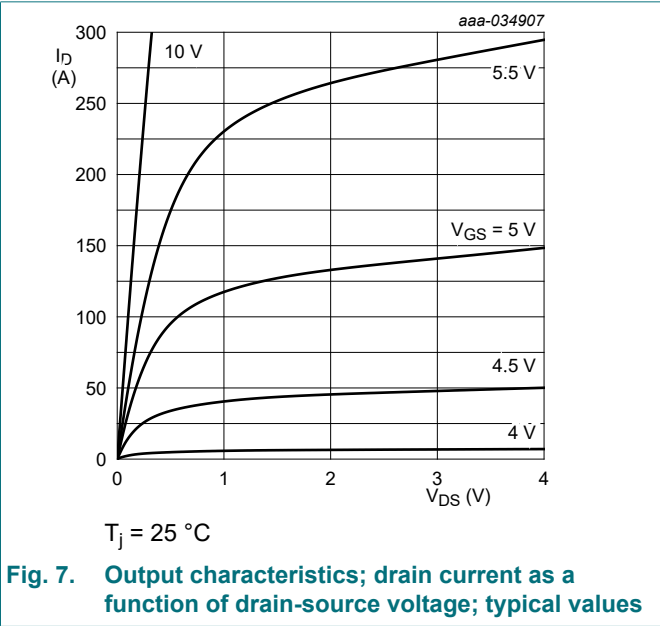
Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25^\circ C$	40	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55^\circ C$	36	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 mA; V_{DS} = V_{GS}; T_j = 25^\circ C$	2.4	3.1	3.6	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	$25^\circ C \leq T_j \leq 150^\circ C$	-	-8	-	mV/K
I_{DSS}	drain leakage current	$V_{DS} = 32 V; V_{GS} = 0 V; T_j = 25^\circ C$	-	0.01	1	μA
		$V_{DS} = 32 V; V_{GS} = 0 V; T_j = 125^\circ C$	-	3	-	μA
I_{GSS}	gate leakage current	$V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25^\circ C$	-	2	100	nA
		$V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25^\circ C$	-	2	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 V; I_D = 25 A; T_j = 25^\circ C$; Fig. 10	-	1.06	1.4	mΩ
		$V_{GS} = 10 V; I_D = 25 A; T_j = 175^\circ C$; Fig. 11	-	-	3.05	mΩ
R_G	gate resistance	$f = 1 MHz; T_j = 25^\circ C$	0.4	1	2.5	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 25 A; V_{DS} = 20 V; V_{GS} = 10 V$; $T_j = 25^\circ C$; Fig. 12 ; Fig. 13	44	68	96	nC
		$I_D = 0 A; V_{DS} = 0 V; V_{GS} = 10 V$; $T_j = 25^\circ C$	-	35	-	nC
Q_{GS}	gate-source charge	$I_D = 25 A; V_{DS} = 20 V; V_{GS} = 10 V$; $T_j = 25^\circ C$; Fig. 12 ; Fig. 13	13	22	33	nC
$Q_{GS(th)}$	pre-threshold gate-source charge		8.7	15	23	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		4.2	7.1	11	nC
Q_{GD}	gate-drain charge		2.8	9.3	19	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 25 A; V_{DS} = 20 V; T_j = 25^\circ C$; Fig. 12 ; Fig. 13	-	4.4	-	V

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Symbol	Parameter	Conditions		Min	Typ	Max	Unit
C _{iss}	input capacitance	V _{DS} = 20 V; V _{GS} = 0 V; f = 1 MHz; T _j = 25 °C; Fig. 14		3492	5373	7523	pF
C _{oss}	output capacitance			885	1361	1905	pF
C _{rss}	reverse transfer capacitance			70.5	235	517	pF
t _{d(on)}	turn-on delay time	V _{DS} = 20 V; R _L = 0.8 Ω; V _{GS} = 10 V; R _{G(ext)} = 5 Ω; T _j = 25 °C		-	19	-	ns
t _r	rise time			-	14	-	ns
t _{d(off)}	turn-off delay time			-	39	-	ns
t _f	fall time			-	16	-	ns
Q _{oss}	output charge	V _{GS} = 0 V; V _{DS} = 20 V; f = 1 MHz; T _j = 25 °C		-	46	-	nC
Source-drain diode							
V _{SD}	source-drain voltage	I _S = 25 A; V _{GS} = 0 V; T _j = 25 °C; Fig. 15		-	0.77	1	V
t _{rr}	reverse recovery time	I _S = 25 A; dI _S /dt = -100 A/μs; V _{GS} = 0 V; V _{DS} = 20 V; T _j = 25 °C; Fig. 16		-	36	-	ns
Q _r	recovered charge		[1]	-	34	-	nC
t _a	reverse recovery rise time			-	20	-	ns
t _b	reverse recovery fall time			-	16	-	ns

[1] includes capacitive recovery



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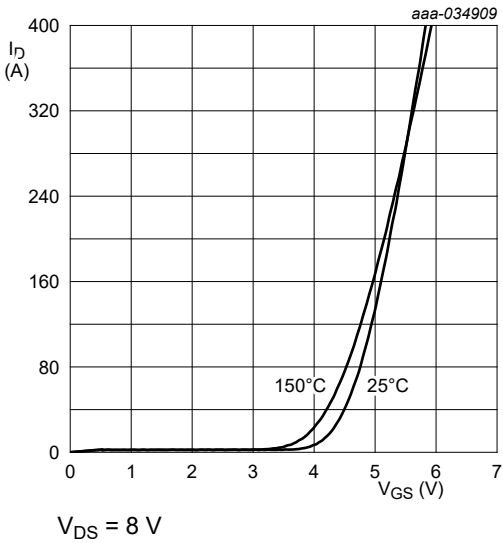


Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values

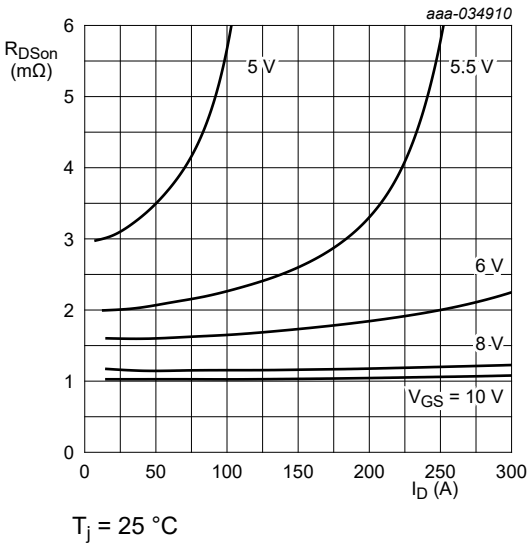


Fig. 10. Drain-source on-state resistance as a function of drain current; typical values

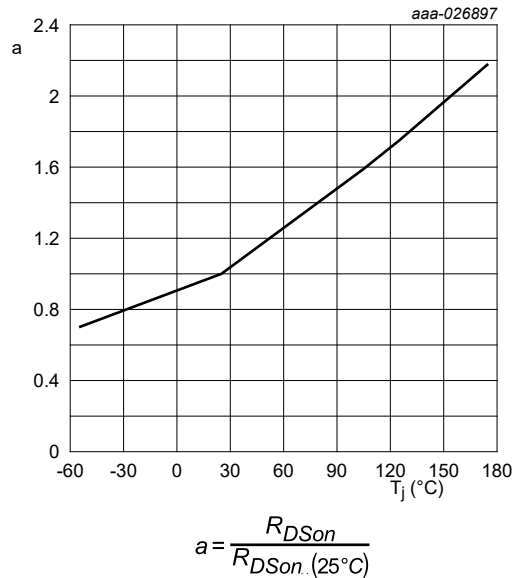


Fig. 11. Normalized drain-source on-state resistance factor as a function of junction temperature

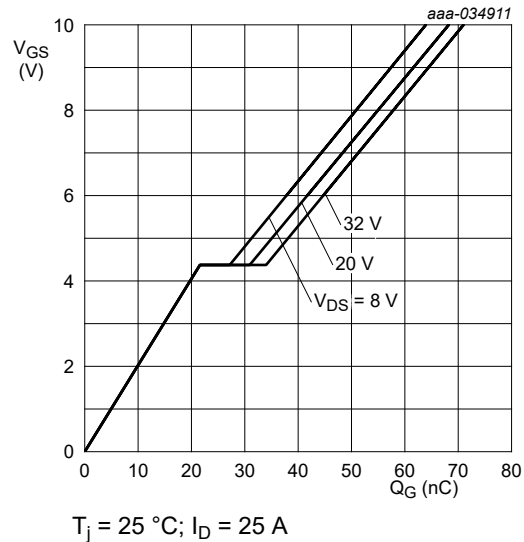


Fig. 12. Gate-source voltage as a function of gate charge; typical values

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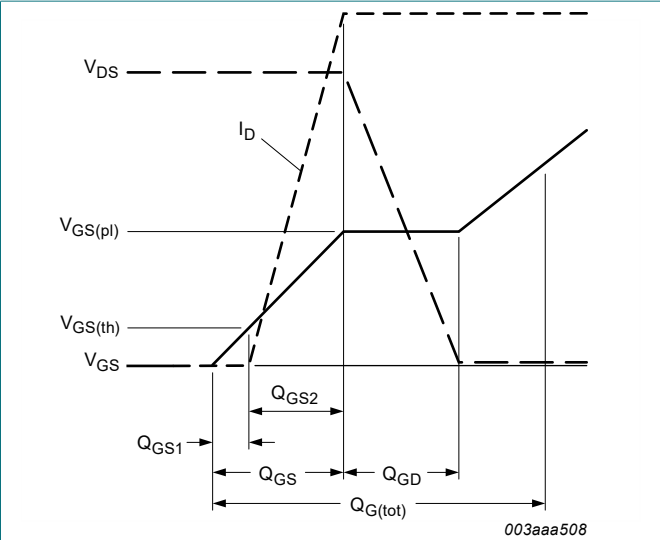


Fig. 13. Gate charge waveform definitions

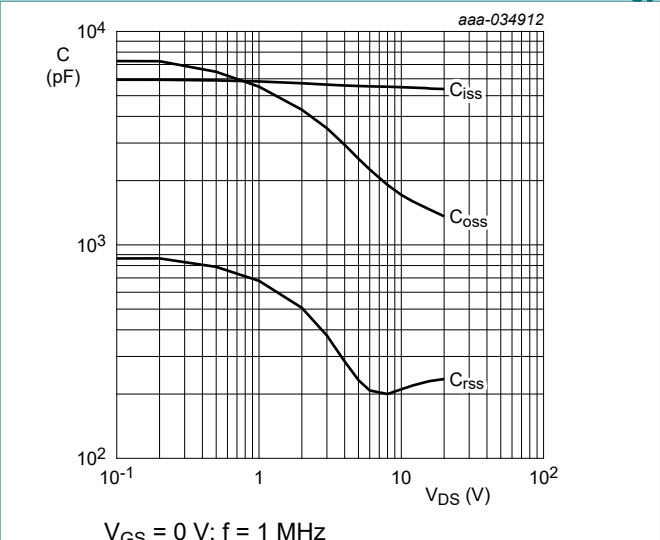


Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

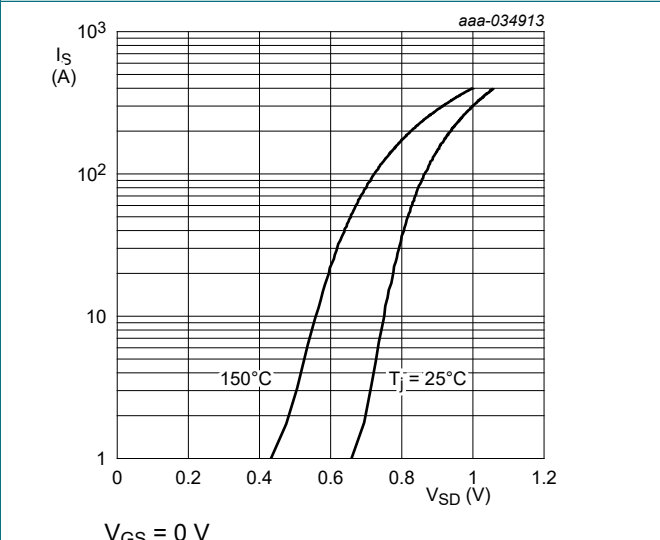


Fig. 15. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

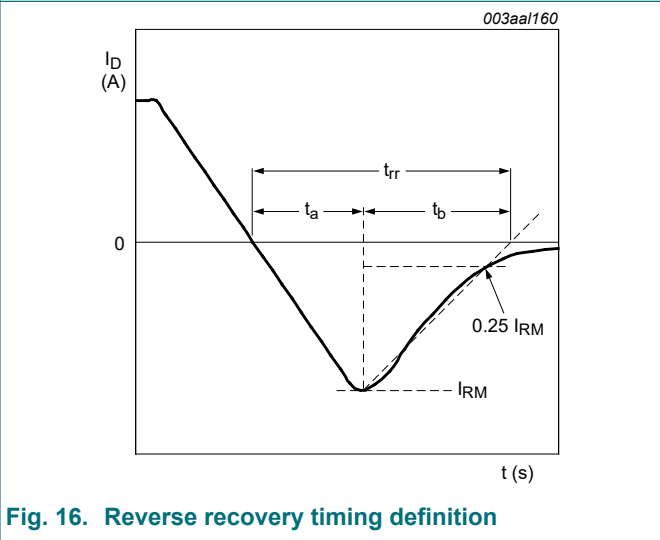


Fig. 16. Reverse recovery timing definition

11. Package outline

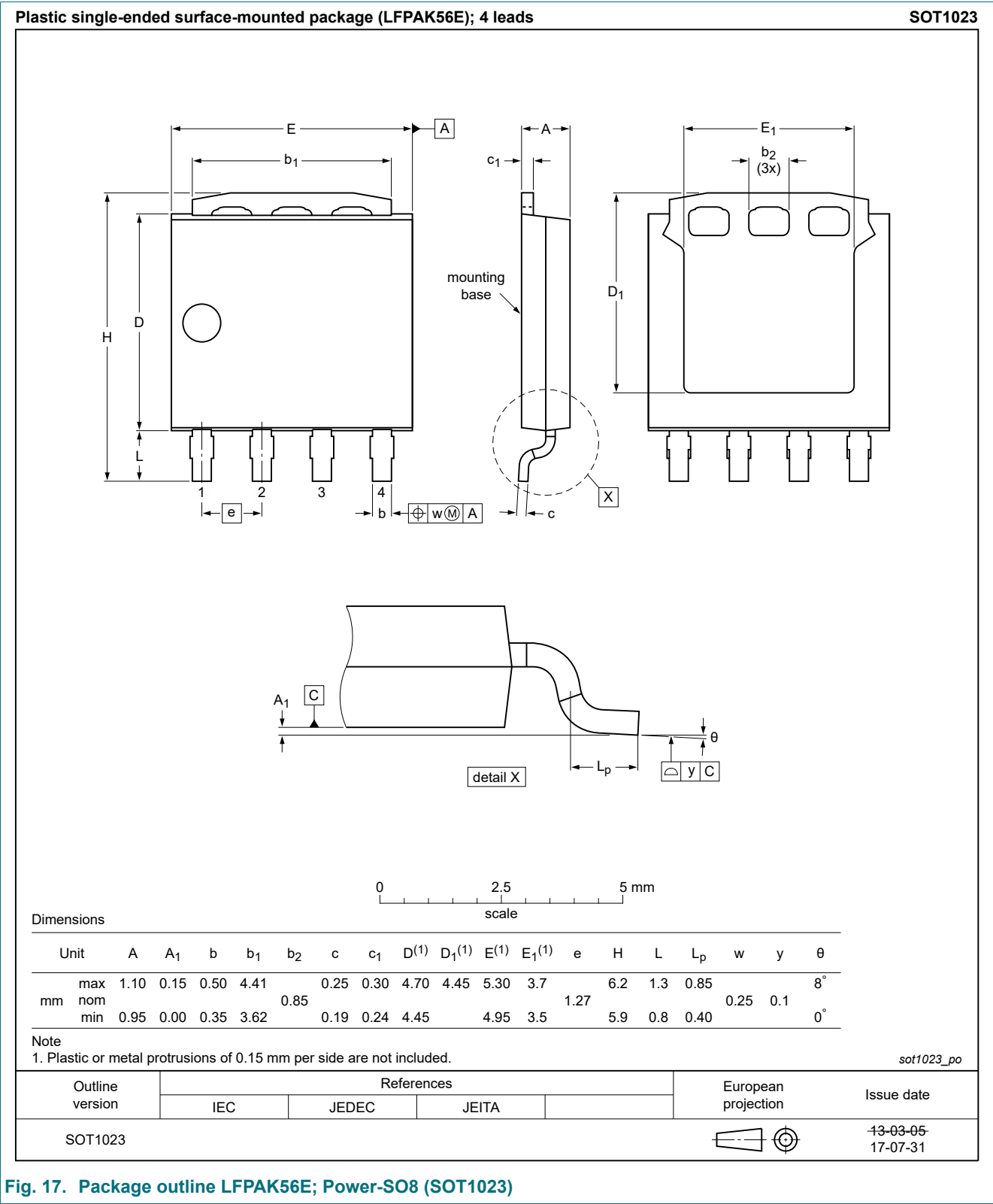
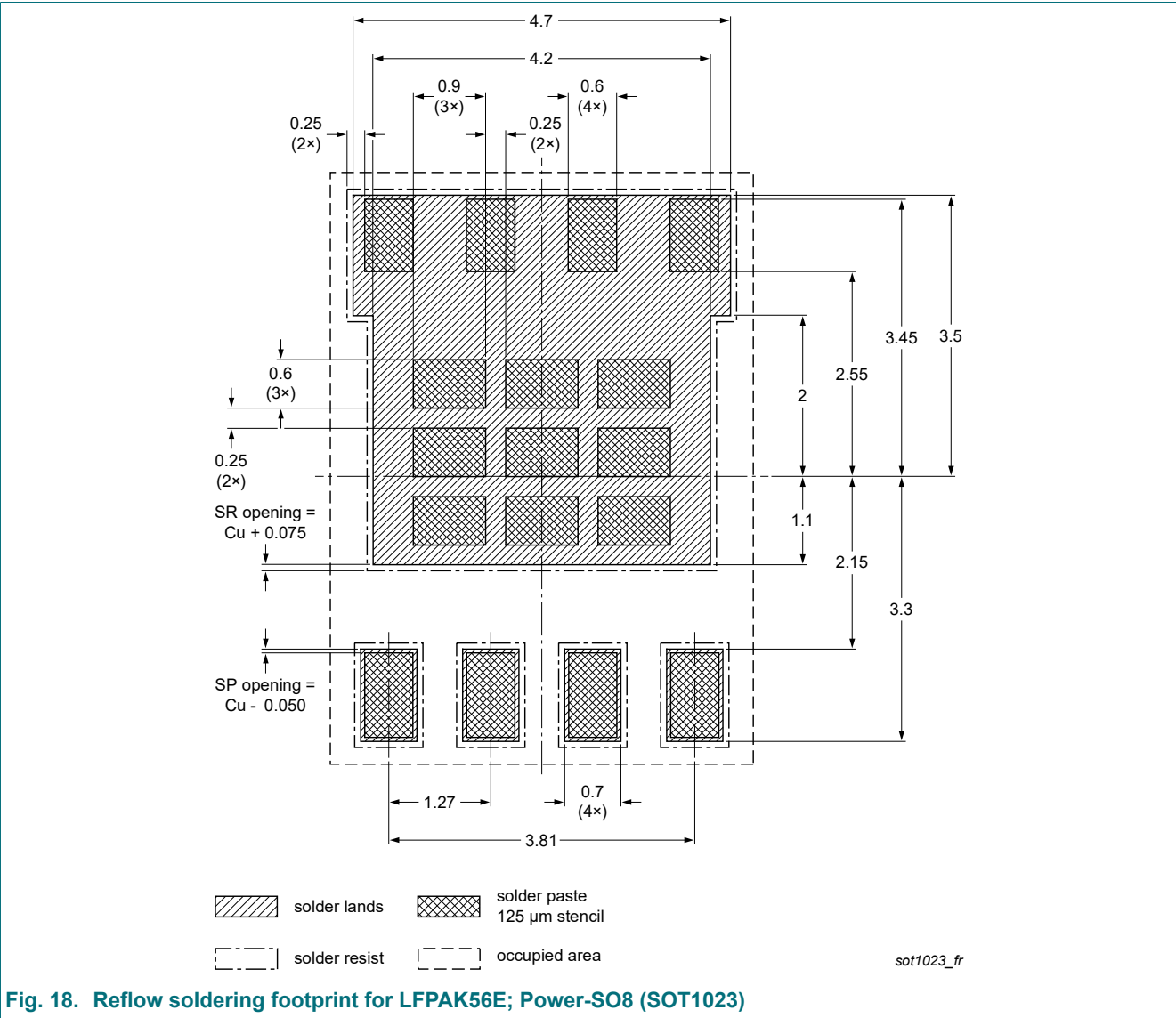


Fig. 17. Package outline LPAK56E; Power-SO8 (SOT1023)

12. Soldering



N-channel 40 V, 1.4 mOhm, 240 A standard level MOSFET in LPAK56 using NextPower-S3 Schottky-Plus technology

13. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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