



PSMNR56-25YLE

N-channel 25 V, 0.63 mOhm, ASFET for hotswap with enhanced SOA in LPAK56E

10 November 2022

Product data sheet

1. General description

N-channel enhancement mode ASFET for hotswap with enhanced SOA in LPAK56E package optimized for low R_{DSon} and strong safe operating area, optimized for hot-swap, inrush and linear-mode applications.

2. Features and benefits

- Fully optimized Safe Operating Area (SOA) for superior linear mode operation
- Optimized for low R_{DSon} / low I^2R conduction losses
- LPAK56E package for applications that demand the highest performance and reliability in a 30 mm² footprint
- Low leakage <1 μ A at 25 °C
- Copper-clip for low parasitic inductance and resistance
- High reliability LPAK package, qualified to 175 °C

3. Applications

- Hot swap in 12 V - 20 V applications
- e-Fuse
- DC switch
- Load switch
- Battery protection

4. Quick reference data

Table 1. Quick reference data

Table 1. Quick reference data							
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V _{DS}	drain-source voltage	25 °C ≤ T _j ≤ 175 °C		-	-	25	V
I _D	drain current	V _{GS} = 10 V; T _{mb} = 25 °C; Fig. 2	[1]	-	-	320	A
P _{tot}	total power dissipation	T _{mb} = 25 °C; Fig. 1		-	-	333	W
T _j	junction temperature			-55	-	175	°C
Static characteristics							
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 25 A; T _j = 25 °C; Fig. 10		-	0.5	0.63	mΩ
		V _{GS} = 7 V; I _D = 25 A; T _j = 25 °C; Fig. 10		-	0.65	0.92	mΩ
Dynamic characteristics							
Q _{GD}	gate-drain charge	I _D = 25 A; V _{DS} = 12 V; V _{GS} = 4.5 V; T _j = 25 °C; Fig. 12 ; Fig. 13		2.7	15	30	nC
Q _{G(tot)}	total gate charge			24	54	89	nC

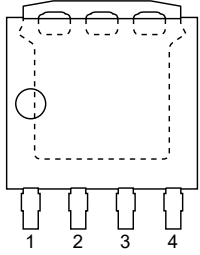
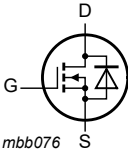
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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Source-drain diode						
S	softness factor	$I_S = 25\text{ A}$; $dI_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$; $V_{DS} = 12\text{ V}$; $T_J = 25\text{ }^\circ\text{C}$; Fig. 16	-	0.92	-	

[1] 320 A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 LPAK56E; Power-SO8 (SOT1023)	 mbb076
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMNR56-25YLE	LPAK56E; Power-SO8	plastic, single-ended surface-mounted package (LPAK56); 4 leads; 1.27 mm pitch	SOT1023

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMNR56-25YLE	E56L25J

8. Limiting values

Table 5. Limiting values

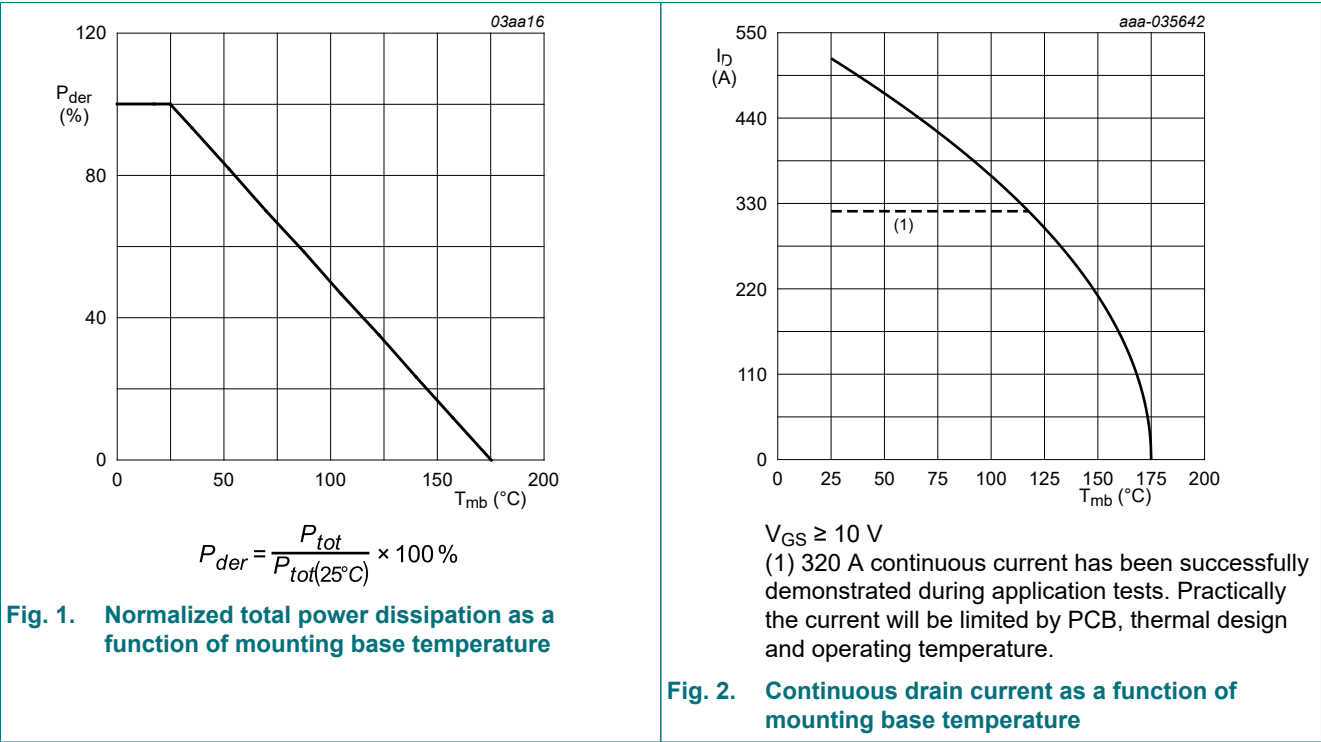
In accordance with the Absolute Maximum Rating System (IEC 60134). $T_J = 25\text{ }^\circ\text{C}$ unless otherwise stated.

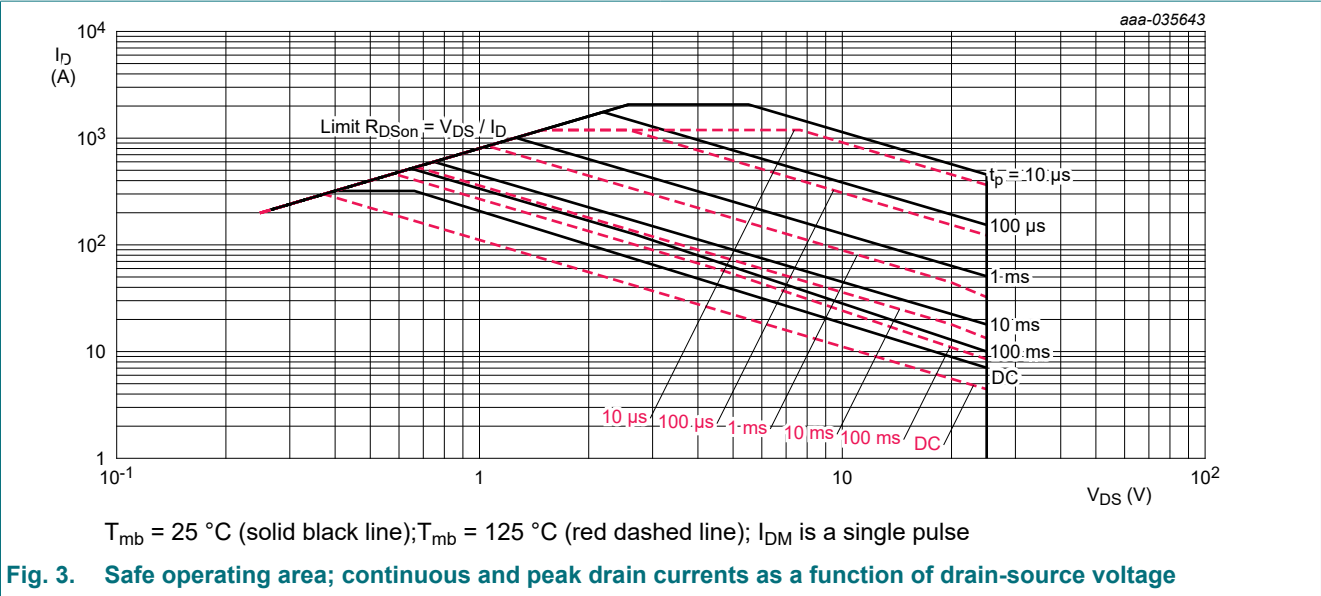
Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$25\text{ }^\circ\text{C} \leq T_J \leq 175\text{ }^\circ\text{C}$	-	25	V
V_{DGR}	drain-gate voltage	$25\text{ }^\circ\text{C} \leq T_J \leq 175\text{ }^\circ\text{C}$; $R_{GS} = 20\text{ k}\Omega$	-	25	V
V_{GS}	gate-source voltage		-20	20	V
P_{tot}	total power dissipation	$T_{mb} = 25\text{ }^\circ\text{C}$; Fig. 1	-	333	W
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ }^\circ\text{C}$; Fig. 2	[1]	320	A
		$V_{GS} = 10\text{ V}$; $T_{mb} = 100\text{ }^\circ\text{C}$; Fig. 2	-	320	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ }^\circ\text{C}$; Fig. 3	-	2068	A

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Symbol	Parameter	Conditions		Min	Max	Unit
T _{stg}	storage temperature			-55	175	°C
T _j	junction temperature			-55	175	°C
T _{slid(M)}	peak soldering temperature			-	260	°C
Source-drain diode						
I _S	source current	T _{mb} = 25 °C		-	320	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C		-	2068	A
Avalanche ruggedness						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I _D = 25 A; V _{sup} ≤ 25 V; R _{GS} = 50 Ω; V _{GS} = 10 V; T _{j(init)} = 25 °C; unclamped; t _p = 18 ms	[2]	-	7.2	J
I _{AS}	non-repetitive avalanche current	V _{sup} ≤ 25 V; V _{GS} = 10 V; T _{j(init)} = 25 °C; R _{GS} = 50 Ω	[2]	-	190	A

- [1] 320 A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.
- [2] Protected by 100% test.

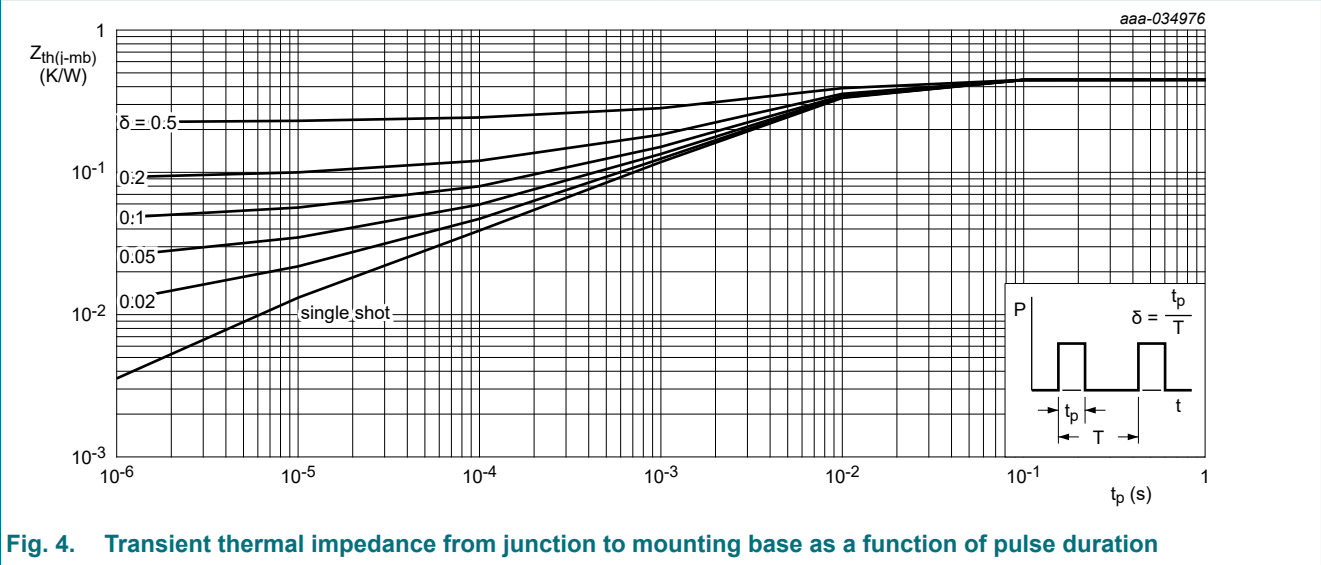


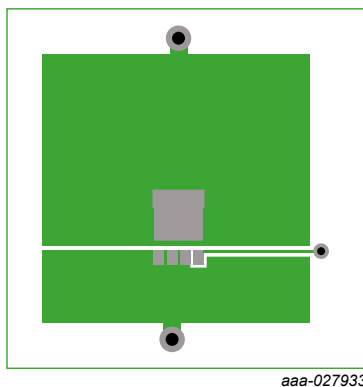


9. Thermal characteristics

Table 6. Thermal characteristics

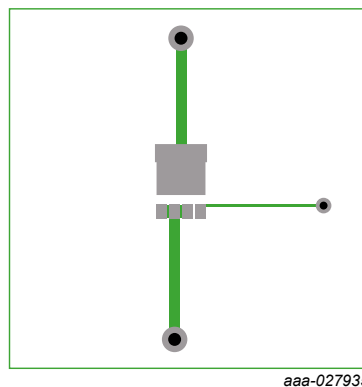
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 4	-	0.35	0.45	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Fig. 5	-	42	-	K/W
		Fig. 6	-	85	-	K/W





Copper area 25.4 mm square; 70 μm thick on FR4 board

Fig. 5. PCB layout for thermal resistance from junction to ambient



70 μm thick copper on FR4 board

Fig. 6. PCB layout with minimum footprint for thermal resistance from junction to ambient

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25^\circ C$	25	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55^\circ C$	22.5	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 2 mA; V_{DS} = V_{GS}; T_j = 25^\circ C$	1.2	1.84	2.2	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	$25^\circ C \leq T_j \leq 150^\circ C$	-	-4	-	mV/K
I_{DSS}	drain leakage current	$V_{DS} = 20 V; V_{GS} = 0 V; T_j = 25^\circ C$	-	-	1	μA
		$V_{DS} = 20 V; V_{GS} = 0 V; T_j = 125^\circ C$	-	11.8	-	μA
I_{GSS}	gate leakage current	$V_{GS} = 16 V; V_{DS} = 0 V; T_j = 25^\circ C$	-	-	100	nA
		$V_{GS} = -16 V; V_{DS} = 0 V; T_j = 25^\circ C$	-	-	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 V; I_D = 25 A; T_j = 25^\circ C; \text{Fig. 10}$	-	0.5	0.63	mΩ
		$V_{GS} = 10 V; I_D = 25 A; T_j = 150^\circ C; \text{Fig. 11}$	-	-	1.1	mΩ
		$V_{GS} = 7 V; I_D = 25 A; T_j = 25^\circ C; \text{Fig. 10}$	-	0.65	0.92	mΩ
		$V_{GS} = 7 V; I_D = 25 A; T_j = 150^\circ C; \text{Fig. 11}$	-	-	1.6	mΩ
R_G	gate resistance	$f = 1 MHz; T_j = 25^\circ C$	1.4	3.6	9	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 25 A; V_{DS} = 12 V; V_{GS} = 4.5 V; T_j = 25^\circ C; \text{Fig. 12; Fig. 13}$	24	54	89	nC
		$I_D = 25 A; V_{DS} = 12 V; V_{GS} = 10 V; T_j = 25^\circ C; \text{Fig. 12; Fig. 13}$	51	115	190	nC
		$I_D = 0 A; V_{DS} = 0 V; V_{GS} = 10 V; T_j = 25^\circ C$	-	59	-	nC

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Q_{GS}	gate-source charge	$I_D = 25\text{ A}$; $V_{DS} = 12\text{ V}$; $V_{GS} = 4.5\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 12 ; Fig. 13		6	23	44	nC
$Q_{GS(th)}$	pre-threshold gate-source charge			3.2	12	23	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge			3	11	21	nC
Q_{GD}	gate-drain charge			2.7	15	30	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 25\text{ A}$; $V_{DS} = 12\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 12 ; Fig. 13		-	3.2	-	V
C_{iss}	input capacitance	$V_{DS} = 12\text{ V}$; $V_{GS} = 0\text{ V}$; $f = 1\text{ MHz}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 14		4855	8091	12137	pF
C_{oss}	output capacitance			1865	3109	4664	pF
C_{rss}	reverse transfer capacitance			183	677	1625	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 12\text{ V}$; $R_L = 0.5\text{ }\Omega$; $V_{GS} = 4.5\text{ V}$; $R_{G(ext)} = 5\text{ }\Omega$; $T_j = 25\text{ }^\circ\text{C}$		-	65	-	ns
t_r	rise time			-	150	-	ns
$t_{d(off)}$	turn-off delay time			-	51	-	ns
t_f	fall time			-	64	-	ns
Q_{oss}	output charge	$V_{GS} = 0\text{ V}$; $V_{DS} = 12\text{ V}$; $f = 1\text{ MHz}$; $T_j = 25\text{ }^\circ\text{C}$		-	57	-	nC
Source-drain diode							
V_{SD}	source-drain voltage	$I_S = 25\text{ A}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 15		-	0.77	1	V
t_{rr}	reverse recovery time	$I_S = 25\text{ A}$; $dI_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$; $V_{DS} = 12\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 16		-	43	-	ns
Q_r	recovered charge		[1]	-	44	-	nC
t_a	reverse recovery rise time			-	22.2	-	ns
t_b	reverse recovery fall time			-	20.5	-	ns
S	softness factor			-	0.92	-	

[1] includes capacitive recovery

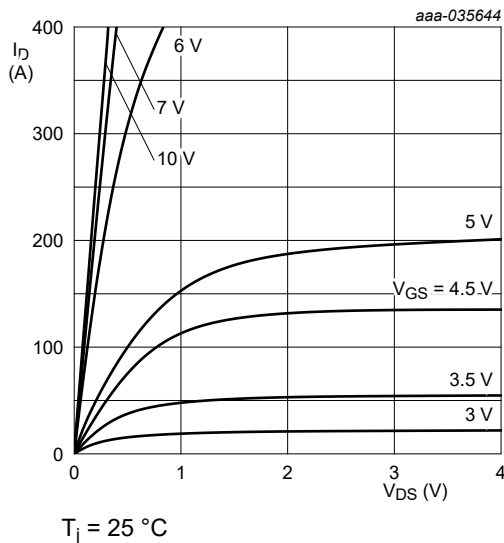


Fig. 7. Output characteristics; drain current as a function of drain-source voltage; typical values

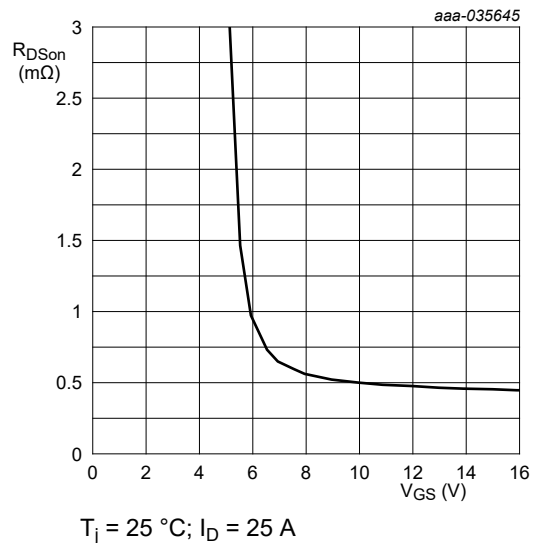


Fig. 8. Drain-source on-state resistance as a function of gate-source voltage; typical values

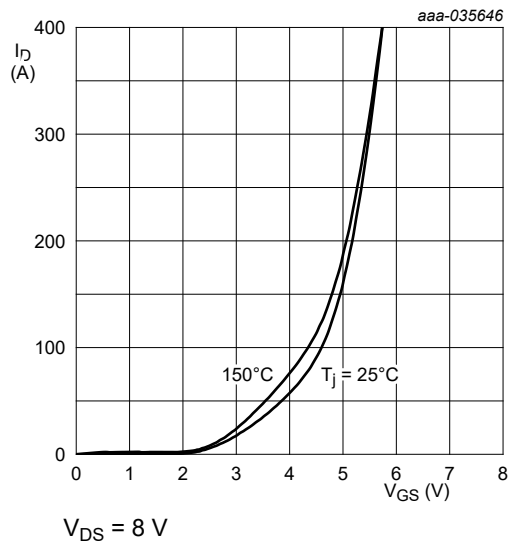


Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values

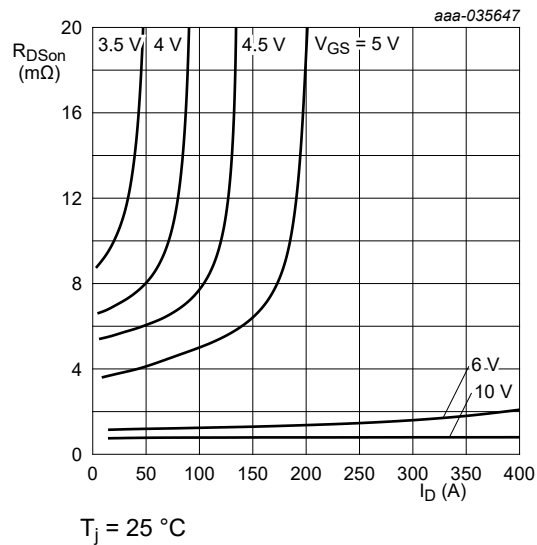


Fig. 10. Drain-source on-state resistance as a function of drain current; typical values

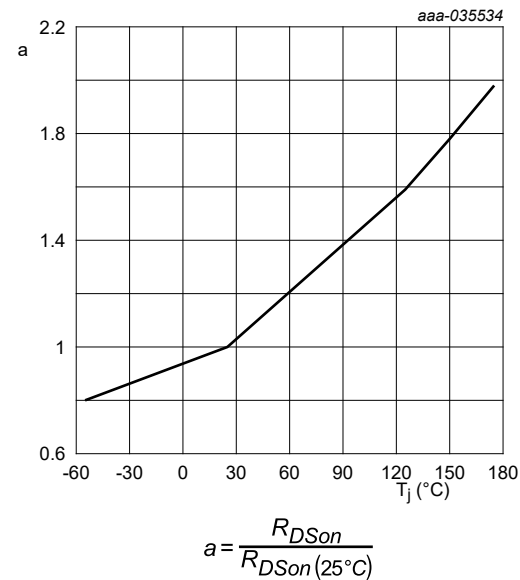


Fig. 11. Normalized drain-source on-state resistance factor as a function of junction temperature

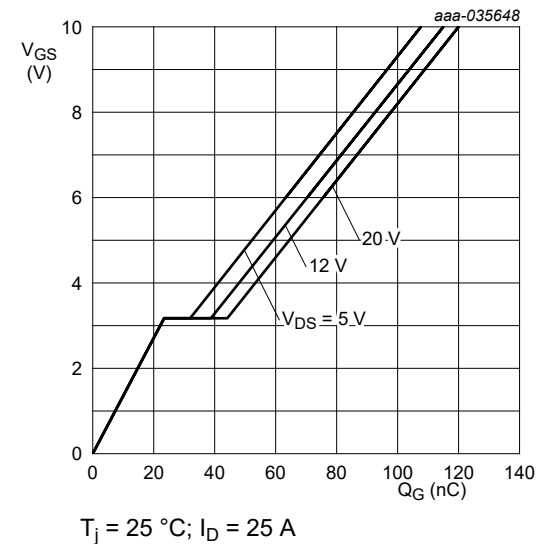


Fig. 12. Gate-source voltage as a function of gate charge; typical values

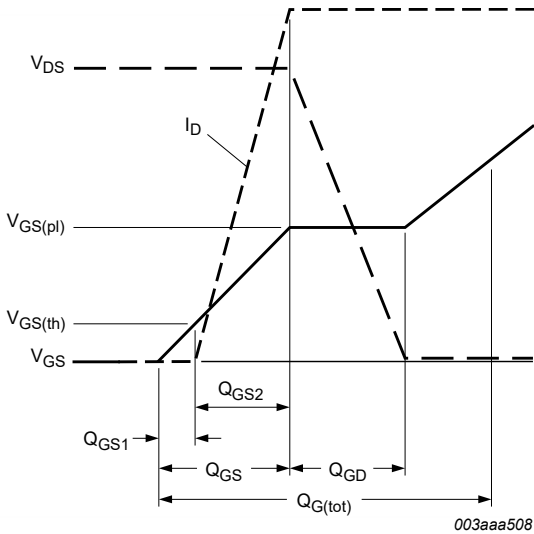


Fig. 13. Gate charge waveform definitions

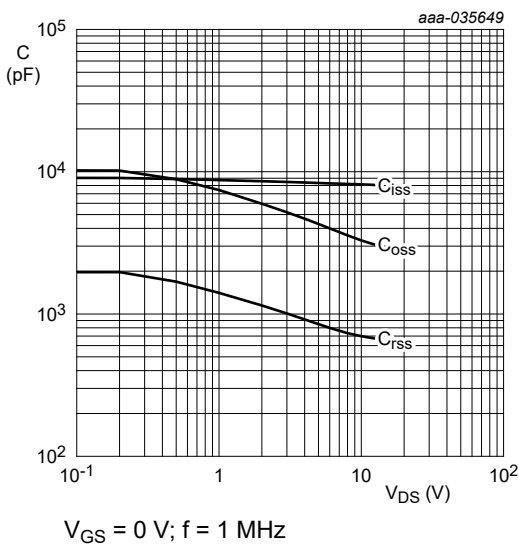


Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

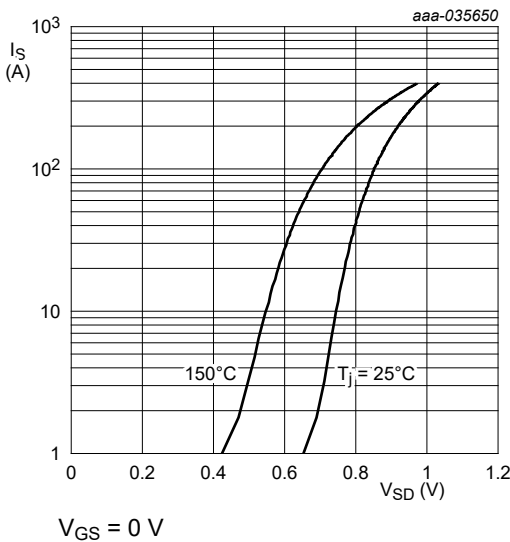


Fig. 15. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

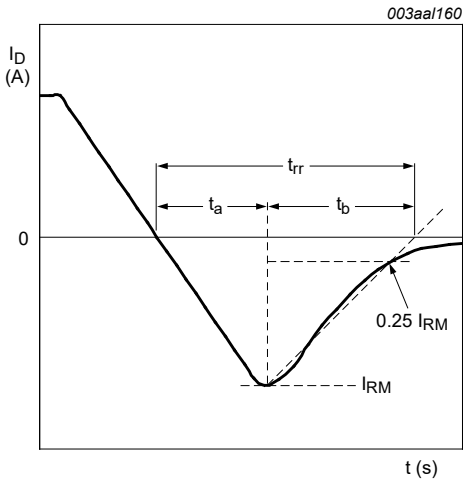


Fig. 16. Reverse recovery timing definition

11. Package outline

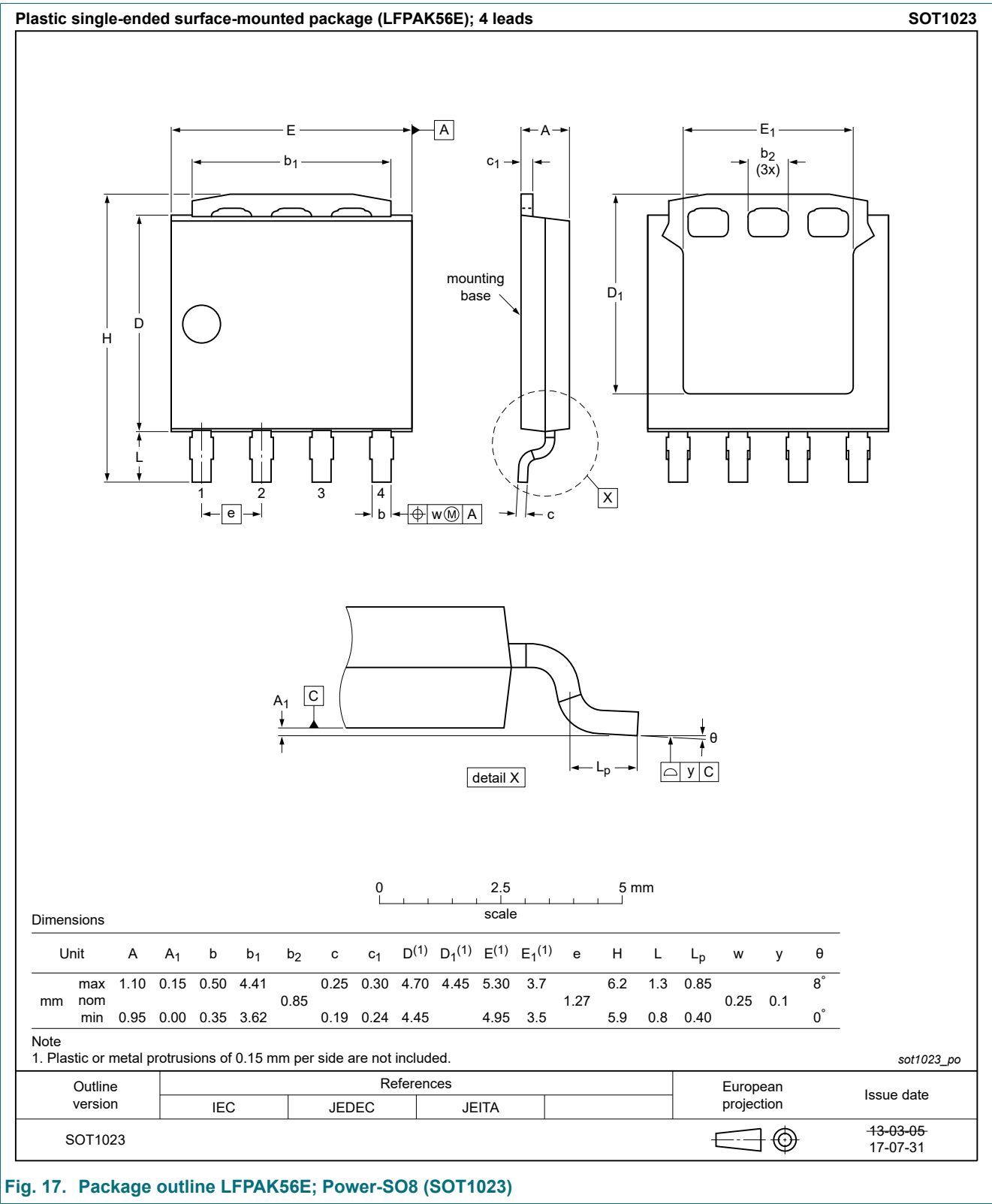


Fig. 17. Package outline LPAK56E; Power-SO8 (SOT1023)

12. Soldering

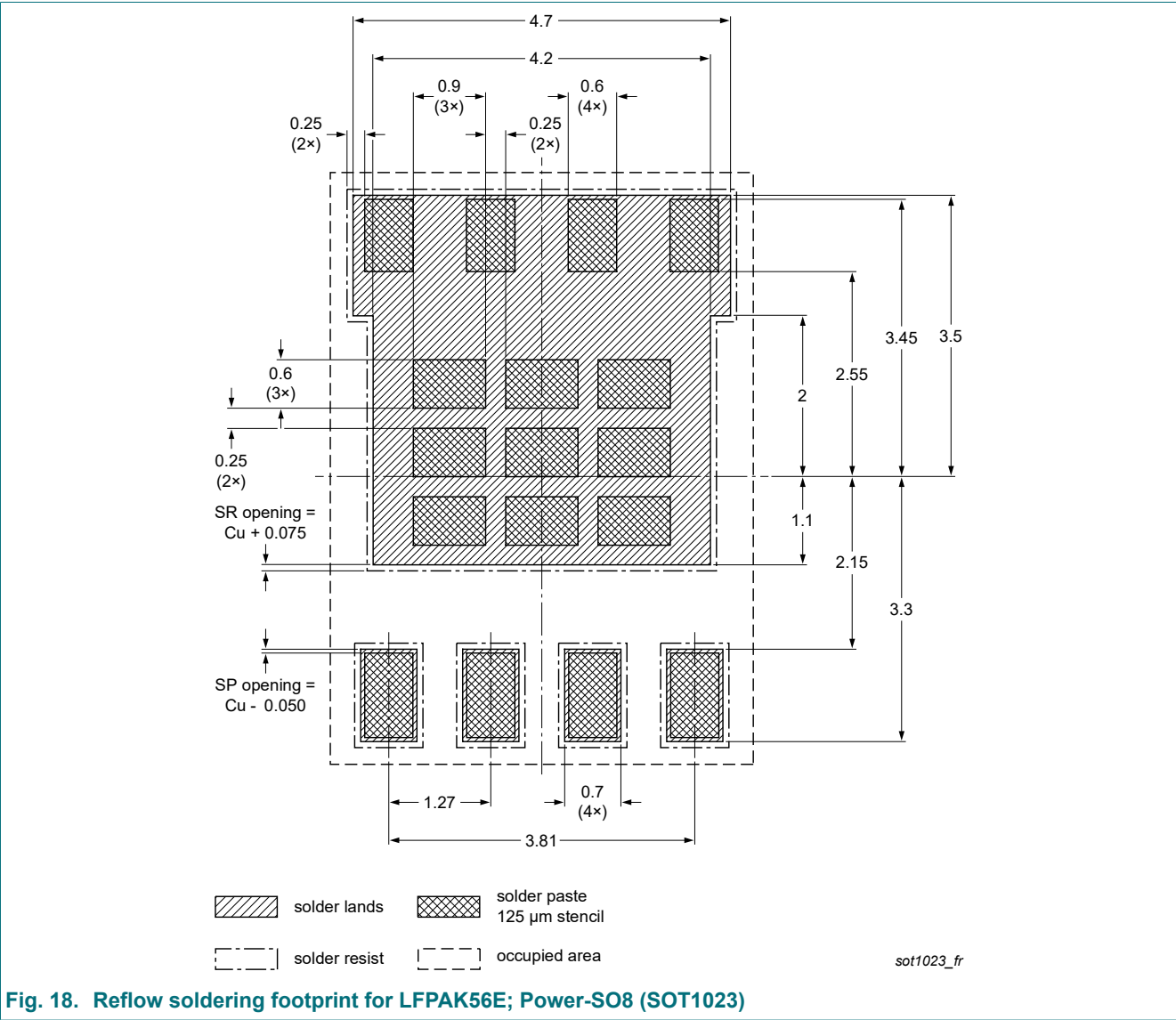


Fig. 18. Reflow soldering footprint for LPAK56E; Power-SO8 (SOT1023)

13. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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