

AK2



ESD Sensitive



2.5 x 2.0 x 1.0 mm  
RoHS/RoHS II Compliant  
MSL = 1

## Product Description

Abrakon's latest addition to the ClearClock™ family of ultra-low rms jitter oscillators is now available in a miniature 2.5 x 2.0 x 1.0 mm package. The AK2 family is based on 3rd overtone quartz crystal technology and is ideally suited for optical transceivers, networking and server systems. AK2 family is available with bias voltages of 3.3V and 2.5V for LVDS & LVPECL output configuration; and 3.3V, 2.5V & 1.8V for HCSL differential output. Production-ready frequencies include 100, 125, 148.5, 156.25 and 200MHz with better than ±30 ppm frequency stability over -40°C to +85°C operating temperature range.

The AK2 family offers best-in-class rms phase jitter of <110 fs typical at 156.25MHz carrier @  $V_{dd} = +2.5V$  with LVDS output, and is guaranteed to exhibit <200fs rms jitter @ 156.25MHz carrier with any bias voltage and RF output configuration.

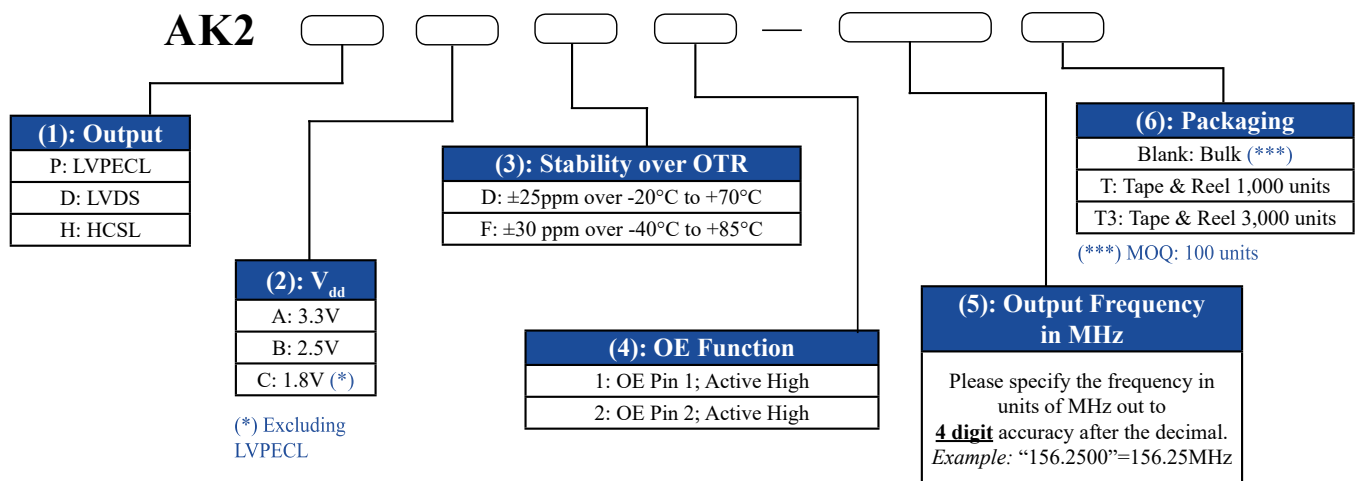
## Features

- Based on 3rd Overtone, Quartz Crystal Technology
- Ultra-low rms jitter; < 120fs typical @ 156.25MHz
- Lowest in-class power consumption (15mA max with LVDS)
- ±25ppm max & ±30ppm max stability over -20°C to +70°C and -40°C to +85°C respectively
- 3.3V, 2.5V & 1.8V supply voltage options
- LVPECL, LVDS and HCSL differential output options
- Output enabled (Active High standard default)

## Applications

- Optical Transceivers
- Optical Modules
- Networking and communications
- Gigabit Ethernet
- Fibre Channel
- SONET/SDH
- RF systems, base stations (BTS)
- Datacenter
- PCI Express
- Test & measurement
- Active cables
- Compact HD-SDI cameras

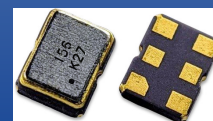
## Options and Part Identification [Note 1]



### Part Number Example:

AK2PAF1-156.2500      [(100) units in Bulk]  
 AK2PAF1-156.2500T      [(1k) units on Tape & Reel]  
 AK2PAF1-156.2500T3      [(3k) units on Tape & Reel]

Note 1: Contact Abracon for non-standard part number configurations and/or requests with carrier frequency callouts up to 5 & 6 digit accuracy after the decimal.



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## Electrical Characteristics

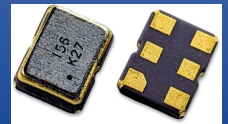
Parameters		Min.	Typ.	Max.	Unit	Notes
Frequency Range		100		200	MHz	
Standard Available Frequencies		100, 125, 148.5, 156.25, 200			MHz	Contact Abracon for availability of frequencies not listed
Supply Voltage ( $V_{dd}$ ) [Note 2]		2.97	3.3	3.63	V	Option "A"
		2.37	2.5	2.62		Option "B"
		1.71	1.8	1.89		Option "C"
Supply Current ( $I_{dd}$ )	LVPECL		30	50	mA	@ 200MHz; @ $V_{dd} = 3.3V$
	LVDS		10	15		@ 200MHz; @ $V_{dd} = 3.3V$
	HCSL		22	30		@ 200MHz; @ $V_{dd} = 3.3V$
Operating Temperature Range		-20		+70	°C	Option "D"
		-40		+85		Option "F"
Storage Temperature		-55		+150	°C	
Frequency Accuracy (Initial Set-Tolerance, as received stand-alone measured frequency) [Note 3] at time of shipment (Pre-Reflow) @ +25°C		-10	< ±5	+10	ppm	Relative to carrier frequency
Frequency Shift through Reflow		-2		+2	ppm	Relative to as received frequency
Frequency Stability over Operating Temperature Range		-25		+25	ppm	Option "D" (-20°C to +70°C)
		-30		+30		Option "F" (-40°C to +85°C)
First Year Aging		-3		3	ppm	Maximum first year aging ±2.00 ppm max. per year thereafter
Aging over 20 Year Product Life [Note 4]		-15		+15	ppm	
All-Inclusive Frequency Accuracy (Total Stability) over 20 Year Product Life [Note 5]		-52		+52	ppm	Option "D" (-20°C to +70°C)
		-57		+57		Option "F" (-40°C to +85°C)
Rise (Tr) / Fall (Tf) Time 20% to 80% $V_{peak\ to\ peak}$	LVPECL		0.3	0.6	ns	@ $V_{dd} = 3.3V, R_L = 50\Omega$
	LVDS		0.3	0.5		@ $V_{dd} = 3.3V, R_L = 100\Omega$
	HCSL		0.3	0.6		@ $V_{dd} = 3.3V, R_L = 50\Omega\ to\ GND$
Duty Cycle		45		55	%	
Start-up Time			< 2	5.0	ms	

Note 2: Supply voltage ( $V_{dd}$ ) = 1.8V option not available with LVPECL output

Note 3: Relative to initial measured frequency @ +25°C, pre-reflow

Note 4: Relative to post-reflow frequency

Note 5: Includes post reflow frequency accuracy, temperature stability, load pulling, power supply variation, and 20-year aging



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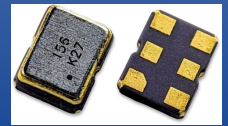
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## Electrical Characteristics Cont.

Parameters		Min.	Typ.	Max.	Unit	Notes
Differential Output High Voltage ( $V_{OH}$ ) Output Low Voltage ( $V_{OL}$ )	LVPECL	$V_{OH}$	$V_{dd}-1.03$		$V_{dd}-0.88$	V $R_L=50\Omega$ to $V_{dd}-2.0V$ $R_L=100\Omega$ between both outputs $R_L=50\Omega$ to ground on each output
		$V_{OL}$	$V_{dd}-1.85$		$V_{dd}-1.60$	
	LVDS	$V_{OH}$		1.40	1.60	
		$V_{OL}$	0.90	1.10		
	HCSL	$V_{OH}$	0.40	0.74	0.85	
		$V_{OL}$	-0.15	0.00	0.15	
Output Voltage Swing		0.50			V	LVPECL
		0.25	0.35	0.45		LVDS
		0.50				HCSL
Output Enable & Disable Control		$0.7*(V_{dd})$			V	Output Enable or No Connect
				$0.3*(V_{dd})$		Output Disable (High Impedance)
Output Enable Time			< 2.00	5.00	ms	
Output Disable Time				0.2	$\mu s$	
Output Disable Current Consumption				< 10	$\mu A$	$OE \leq 0.3V$
RMS Phase Jitter (12kHz to 20MHz from Carrier)			< 200	500	fsec	Vdd, RF output type and Carrier frequency dependent
			< 150	200		@ 156.25MHz



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## Phase Noise Test Setup

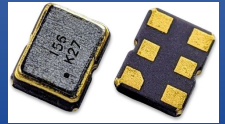
- Keysight E5052B Signal Source Analyzer
- Integration Bandwidth = 12kHz to 20MHz
- Spurious Activity (entire plot trace) = Not omitted (Normalized in dBc/Hz)
- Specified Spur Omission Function = Not enabled
- IF Gain = 20dB
- Correlation = 5
- Average = 3

Typical Values measured at 25°C ± 3°C

Frequency (MHz)	100.00MHz									156.25MHz	
V <sub>DD</sub>	1.8V			2.5V			3.3V			1.8V	2.5V
RF Output	LVDS	HCSL	LVDS	HCSL	LVPECL	LVDS	HCSL	LVPECL	LVDS		
rms Phase Jitter (fsec) 12kHz-20MHz	385.27	147.12	207.96	117.86	131.63	255.13	195.68	123.73	139.49	107.18	
Phase Noise (dBc/Hz)	100Hz	-104.49	-86.91	-80.88	-75.50	-99.17	-87.89	-105.15	-102.40	-93.43	-93.21
	1kHz	-125.64	-120.54	-115.99	-115.89	-129.38	-120.80	-132.38	-132.55	-123.45	-125.31
	10kHz	-134.97	-144.63	-140.15	-147.34	-145.94	-143.61	-144.58	-146.61	-136.98	-139.61
	100kHz	-140.45	-152.42	-149.52	-457.05	-153.02	-146.87	-150.96	-152.79	-140.93	-149.12
	1MHz	-147.69	-155.94	-153.49	-153.53	-156.87	-148.30	-150.70	-156.98	-150.53	-154.70
	10MHz	-149.67	-157.06	-153.53	-159.42	-157.87	-153.04	-154.78	-158.59	-155.31	-156.40

Note 6: Guaranteed by characterization; rms Phase Jitter specifications are inclusive of any spurs  
 Note 7: Phase jitter measured with Keysight E5052B Signal Source Analyzer at 25°C±3°C

# ClearClock™ | Ultra-Low Jitter, Fixed-Frequency Miniature Clock Oscillator



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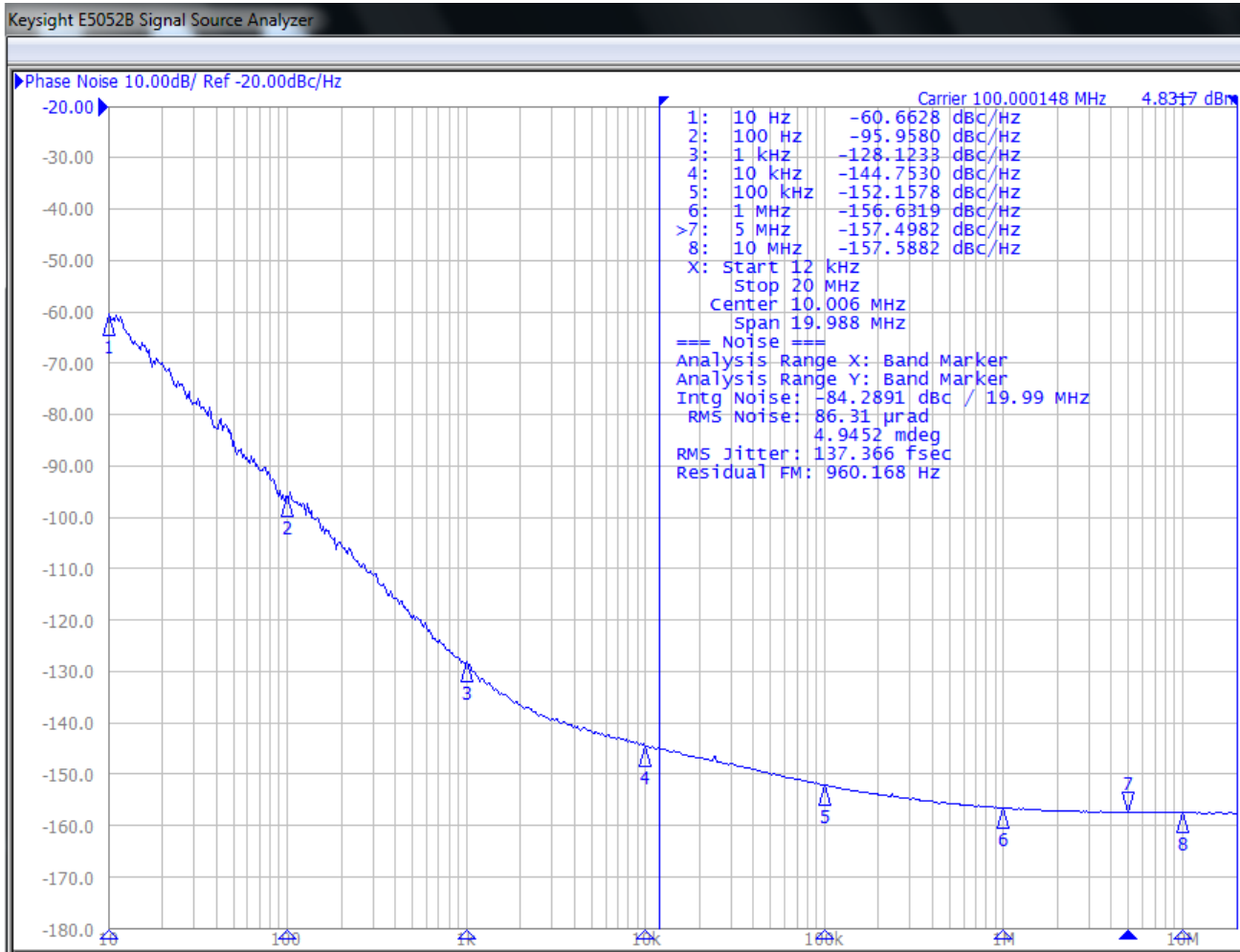
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## Representative Phase Noise Plots @ +25°C [Note 8]

F= 100.00MHz |  $V_{dd}$ =2.50V | LVPECL  
RMS Phase Jitter = 137 fsec



Note 8: Contact Abracon for phase noise plots at alternative supply voltage (Vdd) & differential output formats



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Phone: 512-371-6159 | Fax: 512-351-8858  
For terms and conditions of sales, please visit:  
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REVISED: 09.06.2019

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ISO9001-2015  
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# ClearClock™ | Ultra-Low Jitter, Fixed-Frequency Miniature Clock Oscillator



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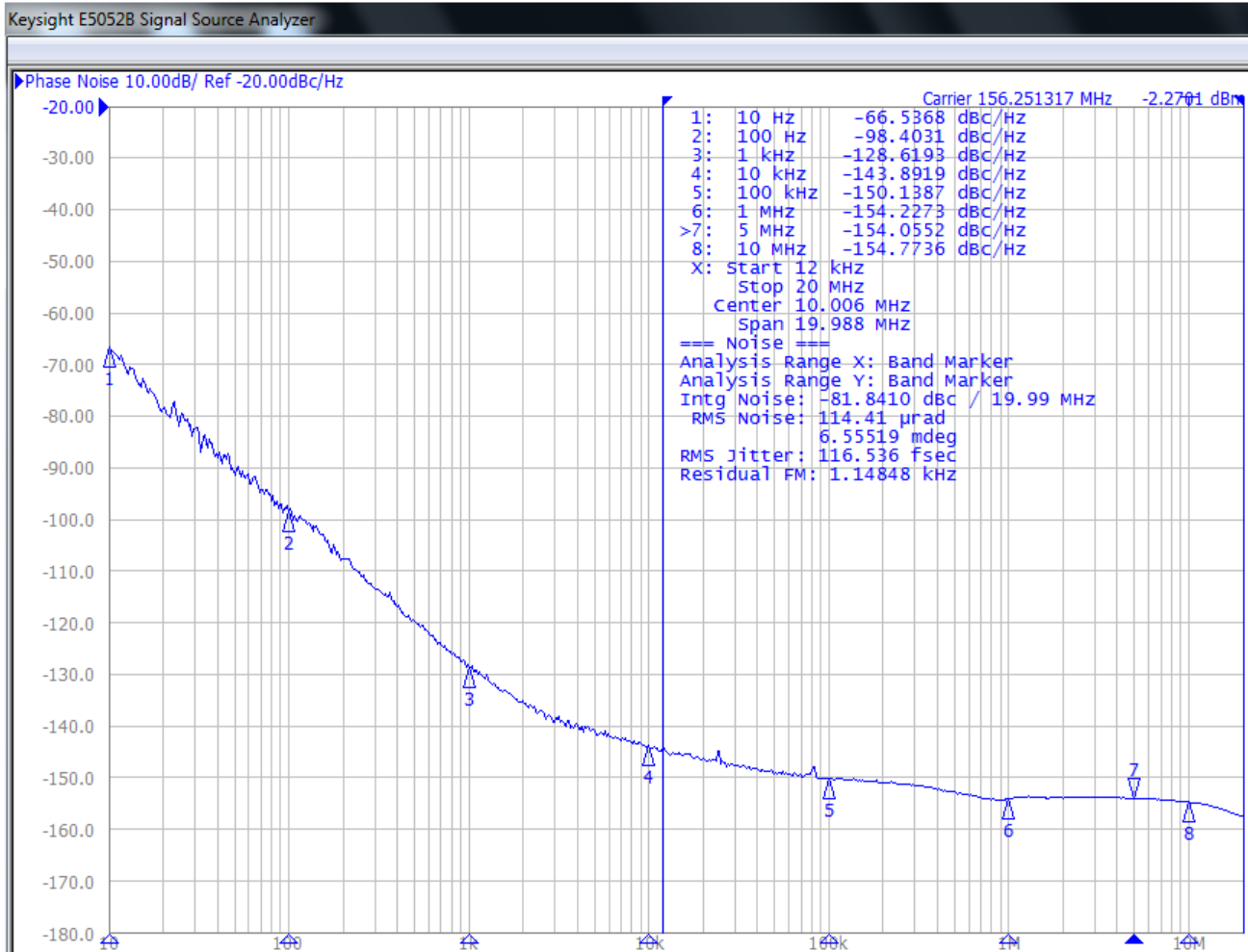
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## Representative Phase Noise Plots @ +25°C [Note 8]

F= 156.2500MHz |  $V_{dd}$ =2.50V | LVDS  
RMS Phase Jitter = 117 fsec



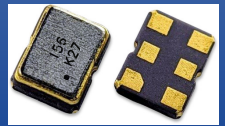
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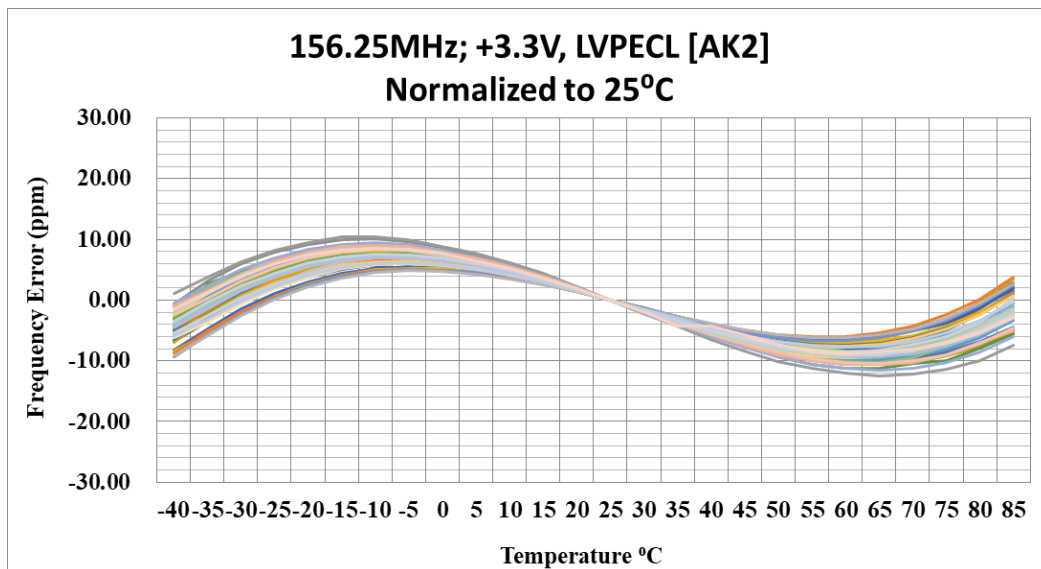
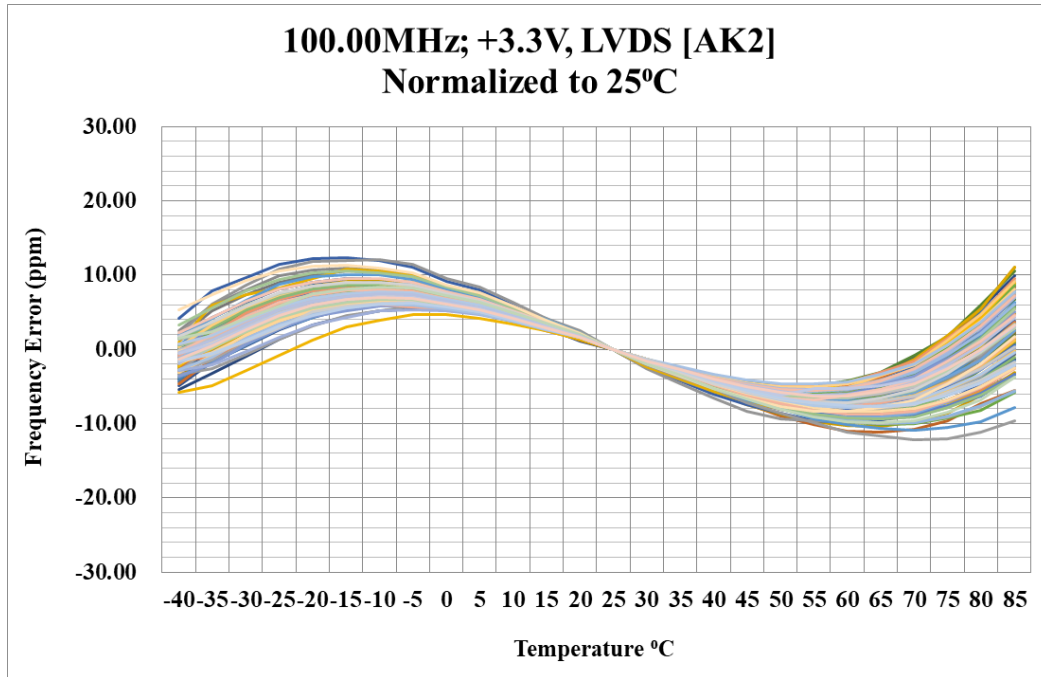


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Typical Frequency vs. Temperature Characteristics





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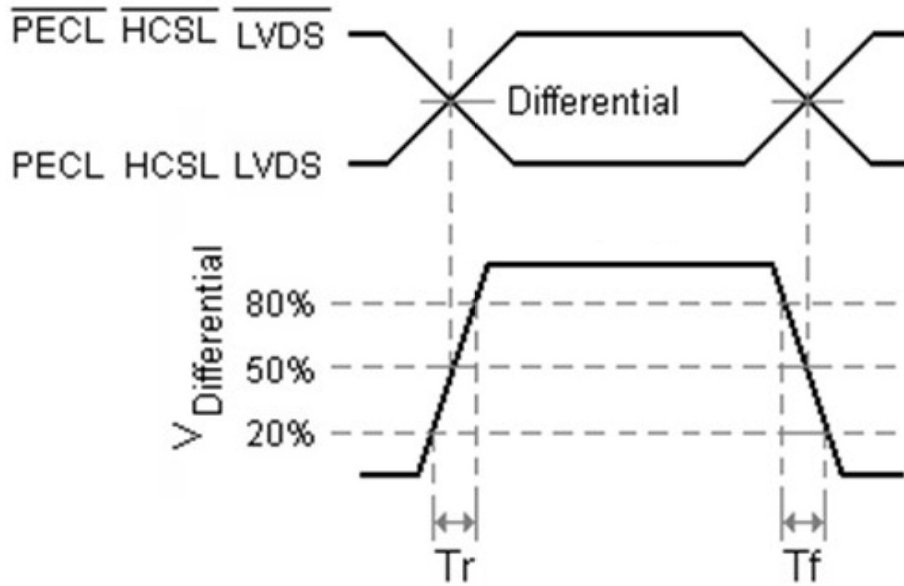
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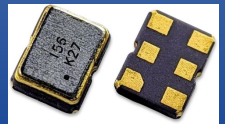


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### Differential Output Waveform

#### LVPECL, LVDS and HCSL Output Waveforms





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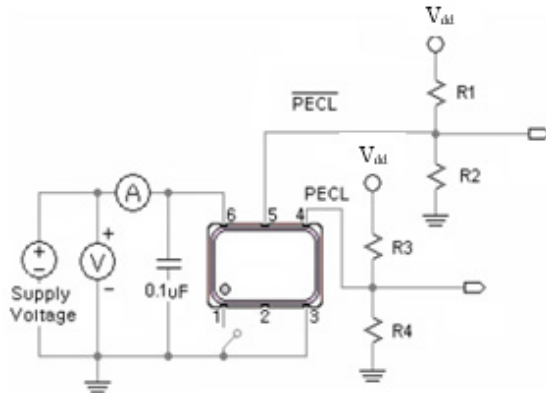
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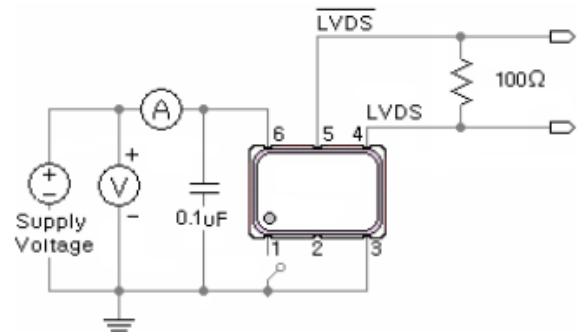
## Recommended Test Circuit <sup>[Note 9]</sup>

### LVPECL

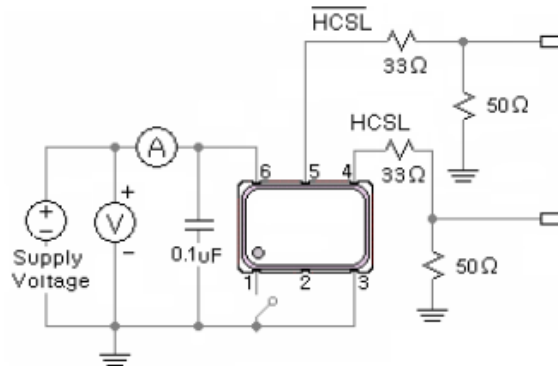


V<sub>dd</sub> = 3.3V: R<sub>1</sub>=R<sub>3</sub>=127Ω; R<sub>2</sub>=R<sub>4</sub>=82.5Ω  
V<sub>dd</sub> = 2.5V: R<sub>1</sub>=R<sub>3</sub>=250Ω; R<sub>2</sub>=R<sub>4</sub>=62.5Ω

### LVDS



### HCSL



Note 9: Recommended test circuit images are representative of when the OE Function is located on Pin 1; when the OE Function is located on Pin 2, then Pin 1=No Connect & Pin 2=OE or No Connect.



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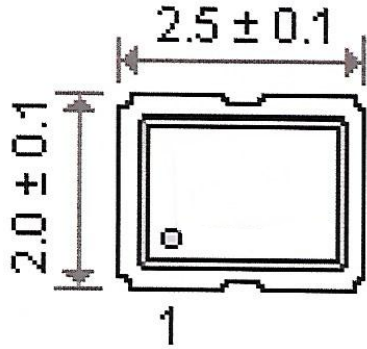
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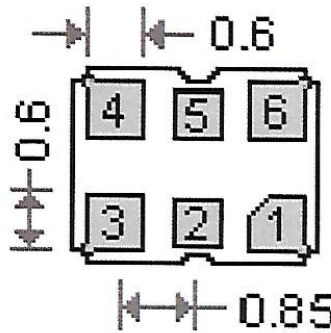
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**Mechanical Dimensions**

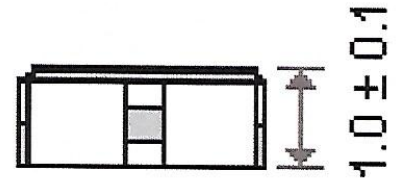
Top View



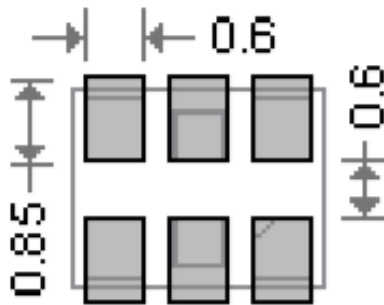
Bottom View



Side View

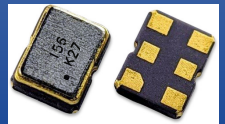


Recommended Land Pattern



Case 1 Pin #1= Enable/Disable Function where OE is Active HIGH		Case 2 Pin #2= Enable/Disable Function where OE is Active HIGH	
Pin	Description	Pin	Description
# 1	Output Enable = Logic High, "1", V <sub>dd</sub>	# 1	No Connect
	Output Disable = Logic Low, "0", GND	# 2	Output Enable = Logic High, "1", V <sub>dd</sub>
# 2	No Connect		Output Enable = Logic Low, "0", GND
# 3	GND	# 3	GND
# 4	Output	# 4	Output
# 5	Complementary output	# 5	Complementary output
# 6	Supply Voltage (V <sub>dd</sub> )	# 6	Supply Voltage (V <sub>dd</sub> )

Dimensions: [mm]



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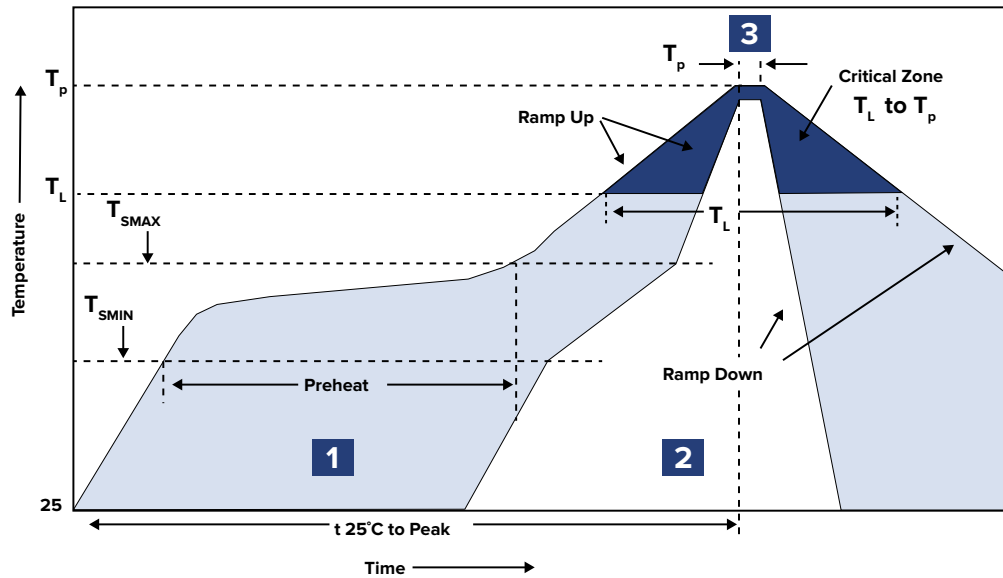


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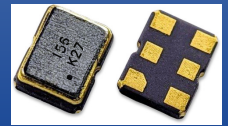


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Recommended Reflow Profile



Zone	Description	Temperature	Time
1	Preheat / Soak	$T_{SMIN} \sim T_{SMAX}$ 150°C ~ 220°C	80 ~ 140 sec.
2	Reflow	$T_L$ 220°C	60 sec.
3	Peak heat	$T_P$ 260°C±5°C	~10 sec.



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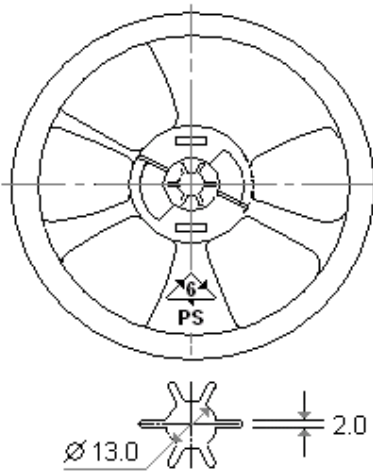
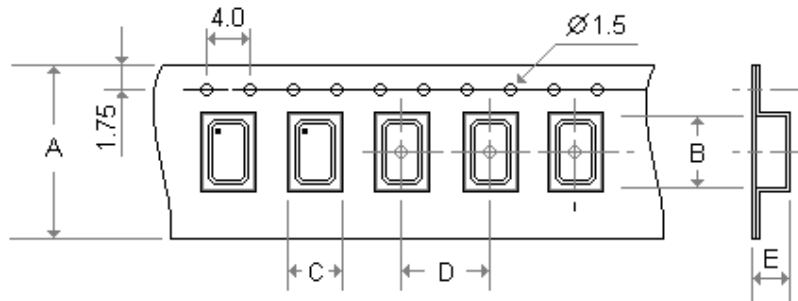
## Packaging

Blank = Bulk (MOQ=100 units)

T = Tape & Reel 1,000 units/reel

T3 = Tape & Reel 3,000 units/reel

Feeding (PULL) Direction →



Dimensions : ( Unit : mm )

A	B	C	D	E
8.0	2.7	2.2	4.0	1.2

F	G	H
180.0	9.0	12.0

- (10) sprocket hold pitch cumulative tolerance is  $\pm 0.10$  mm
- “E” measured from a place on the inside bottom of the pocket to the top surface of the carrier

Dimensions: mm

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