

MOSFET

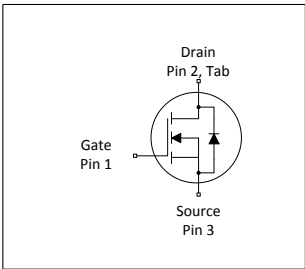
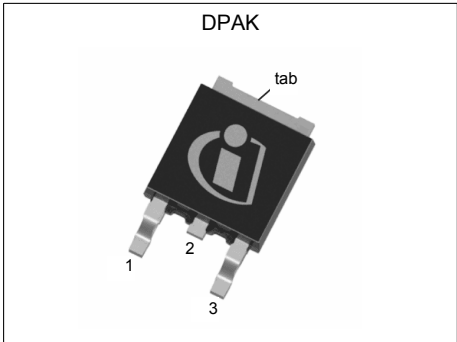
StrongIRFET™ 2 Power-Transistor

Features

- Optimized for a wide range of applications
- N-Channel, normal level
- 100% avalanche tested
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

Product validation

Qualified according to JEDEC Standard



RoHS

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	80	V
$R_{DS(on),max}$	5.5	$m\Omega$
I_D	98	A
Q_{oss}	44	nC
Q_G	36	nC

Type / Ordering Code	Package	Marking	Related Links
IPD055N08NF2S	PG-TO252-3	055N08NS	-

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1 Maximum ratings

at $T_A=25\text{ °C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	98 70 57 17	A	$V_{GS}=10\text{ V}$, $T_C=25\text{ °C}$ $V_{GS}=10\text{ V}$, $T_C=100\text{ °C}$ $V_{GS}=6\text{ V}$, $T_C=100\text{ °C}$ $V_{GS}=10\text{ V}$, $T_A=25\text{ °C}$, $R_{thJA}=50\text{ °C/W}^{2)}$
Pulsed drain current ³⁾	$I_{D,pulse}$	-	-	392	A	$T_C=25\text{ °C}$
Avalanche energy, single pulse ⁴⁾	E_{AS}	-	-	54	mJ	$I_D=90\text{ A}$, $R_{GS}=25\text{ }\Omega$
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	107 3.0	W	$T_C=25\text{ °C}$ $T_A=25\text{ °C}$, $R_{thJA}=50\text{ °C/W}^{2)}$
Operating and storage temperature	T_j , T_{stg}	-55	-	175	°C	-

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	1.4	°C/W	-
Thermal resistance, junction - ambient, 6 cm ² cooling area ²⁾	R_{thJA}	-	-	50	°C/W	-
Thermal resistance, junction - ambient, minimal footprint	R_{thJA}	-	-	75	°C/W	-

¹⁾ Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

²⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

³⁾ See Diagram 3 for more detailed information

⁴⁾ See Diagram 13 for more detailed information

3 Electrical characteristics

at $T_j=25\text{ °C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	80	-	-	V	$V_{GS}=0\text{ V}$, $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	2.2	3.0	3.8	V	$V_{DS}=V_{GS}$, $I_D=55\text{ }\mu\text{A}$
Zero gate voltage drain current	I_{DSS}	-	0.1 10	1 100	μA	$V_{DS}=80\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$ $V_{DS}=80\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=125\text{ °C}$
Gate-source leakage current	I_{GSS}	-	10	100	nA	$V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	4.7 6.1	5.5 8.1	m Ω	$V_{GS}=10\text{ V}$, $I_D=60\text{ A}$ $V_{GS}=6\text{ V}$, $I_D=30\text{ A}$
Gate resistance	R_G	-	1.3	-	Ω	-
Transconductance ¹⁾	g_{fs}	46	-	-	S	$ V_{DS} \geq 2 I_D /R_{DS(on)max}$, $I_D=60\text{ A}$

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	2500	-	pF	$V_{GS}=0\text{ V}$, $V_{DS}=40\text{ V}$, $f=1\text{ MHz}$
Output capacitance	C_{oss}	-	420	-	pF	$V_{GS}=0\text{ V}$, $V_{DS}=40\text{ V}$, $f=1\text{ MHz}$
Reverse transfer capacitance	C_{rss}	-	20	-	pF	$V_{GS}=0\text{ V}$, $V_{DS}=40\text{ V}$, $f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	-	14	-	ns	$V_{DD}=40\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=60\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Rise time	t_r	-	37	-	ns	$V_{DD}=40\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=60\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	-	21	-	ns	$V_{DD}=40\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=60\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Fall time	t_f	-	7	-	ns	$V_{DD}=40\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=60\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$

Table 6 Gate charge characteristics²⁾

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	12.3	-	nC	$V_{DD}=40\text{ V}$, $I_D=60\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate charge at threshold	$Q_{g(th)}$	-	7.5	-	nC	$V_{DD}=40\text{ V}$, $I_D=60\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate to drain charge	Q_{gd}	-	8	-	nC	$V_{DD}=40\text{ V}$, $I_D=60\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Switching charge	Q_{sw}	-	13	-	nC	$V_{DD}=40\text{ V}$, $I_D=60\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total ¹⁾	Q_g	-	36	54	nC	$V_{DD}=40\text{ V}$, $I_D=60\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate plateau voltage	$V_{plateau}$	-	5	-	V	$V_{DD}=40\text{ V}$, $I_D=60\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Output charge	Q_{oss}	-	44	-	nC	$V_{DS}=40\text{ V}$, $V_{GS}=0\text{ V}$

¹⁾ Defined by design. Not subject to production test.

²⁾ See "Gate charge waveforms" for parameter definition

Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	79	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	392	A	$T_C=25\text{ °C}$
Diode forward voltage	V_{SD}	-	0.93	1.2	V	$V_{GS}=0\text{ V}$, $I_F=60\text{ A}$, $T_j=25\text{ °C}$
Reverse recovery time	t_{rr}	-	30	-	ns	$V_R=40\text{ V}$, $I_F=60\text{ A}$, $di_F/dt=500\text{ A}/\mu\text{s}$
Reverse recovery charge	Q_{rr}	-	154	-	nC	$V_R=40\text{ V}$, $I_F=60\text{ A}$, $di_F/dt=500\text{ A}/\mu\text{s}$

4 Electrical characteristics diagrams

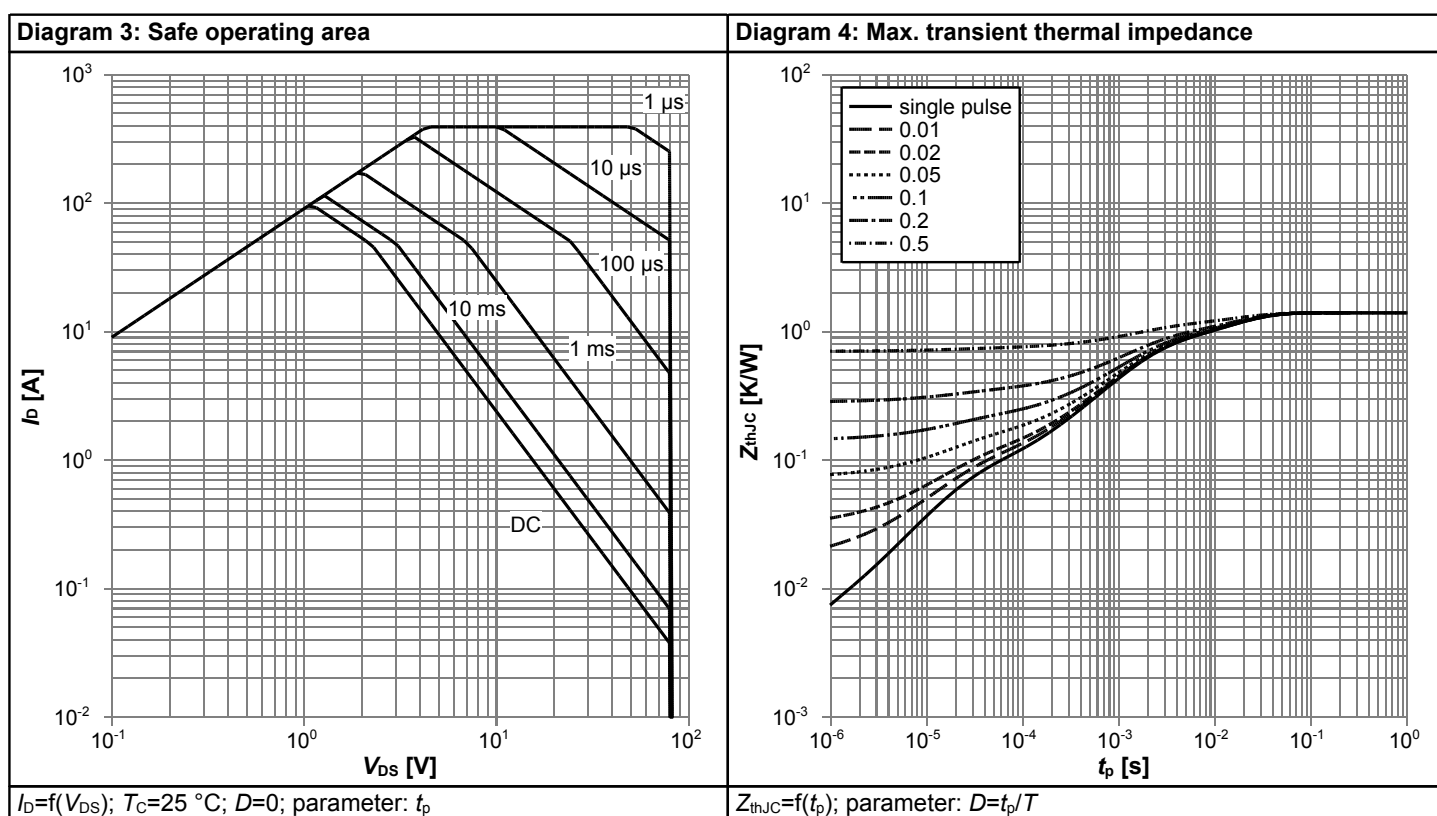
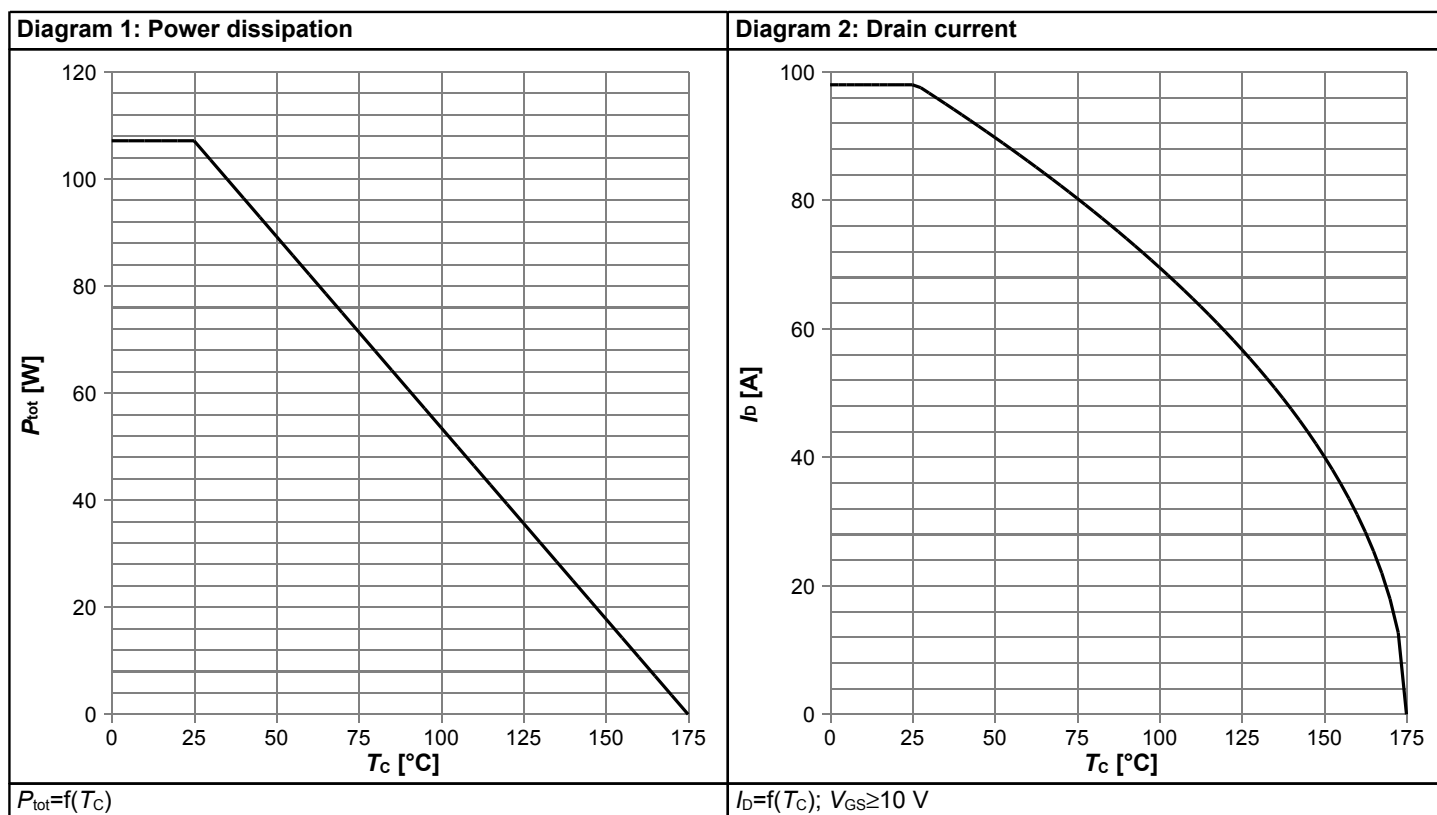
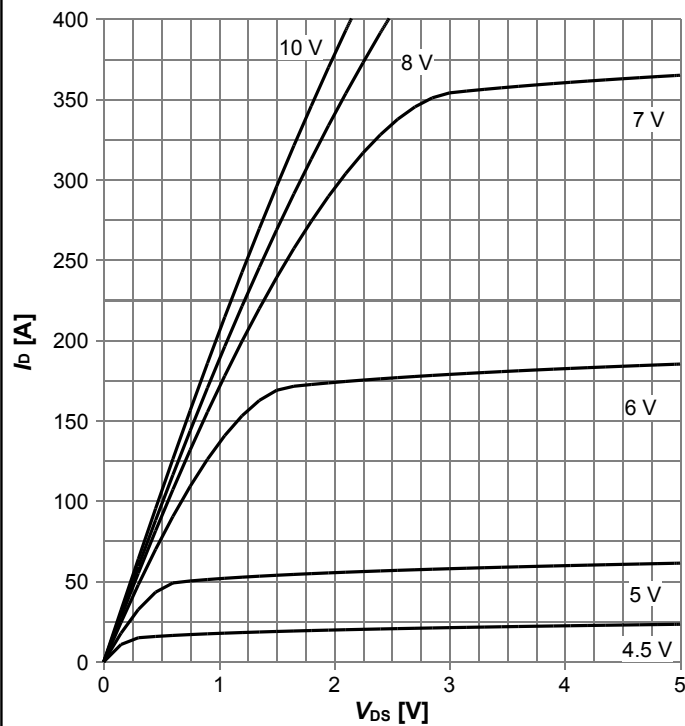
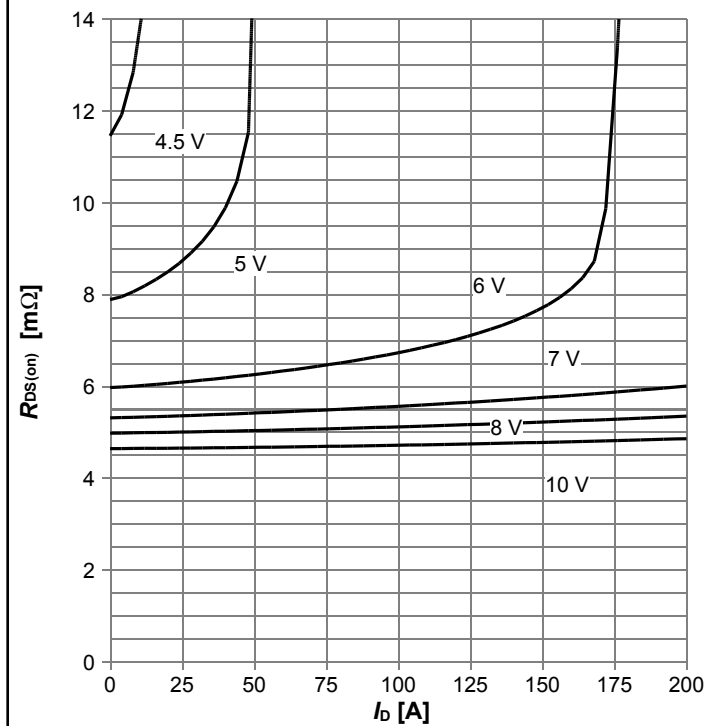


Diagram 5: Typ. output characteristics



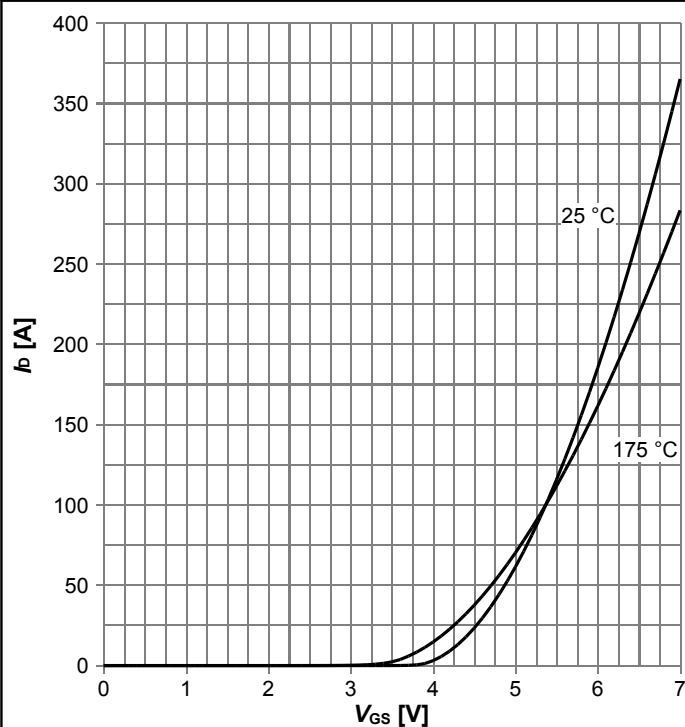
$I_D = f(V_{DS})$, $T_j = 25^\circ\text{C}$; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



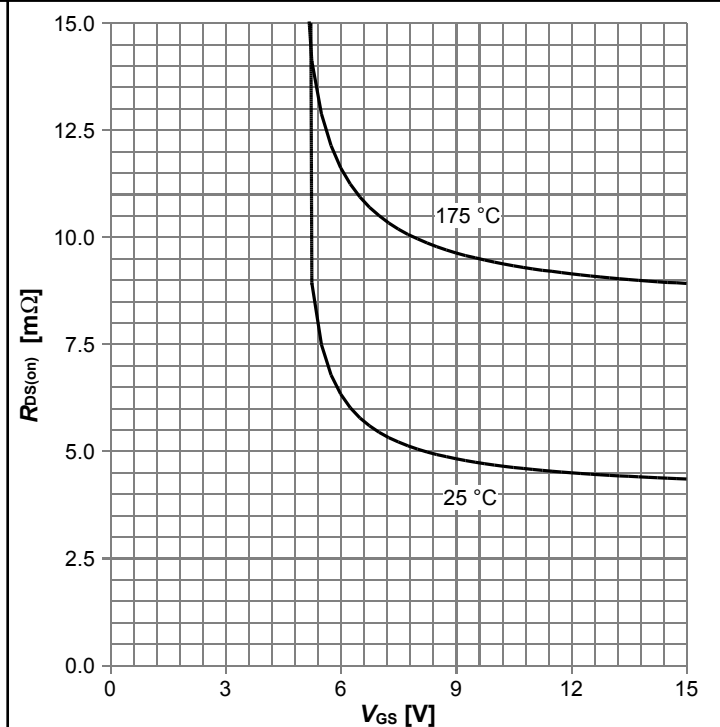
$R_{DS(on)} = f(I_D)$, $T_j = 25^\circ\text{C}$; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



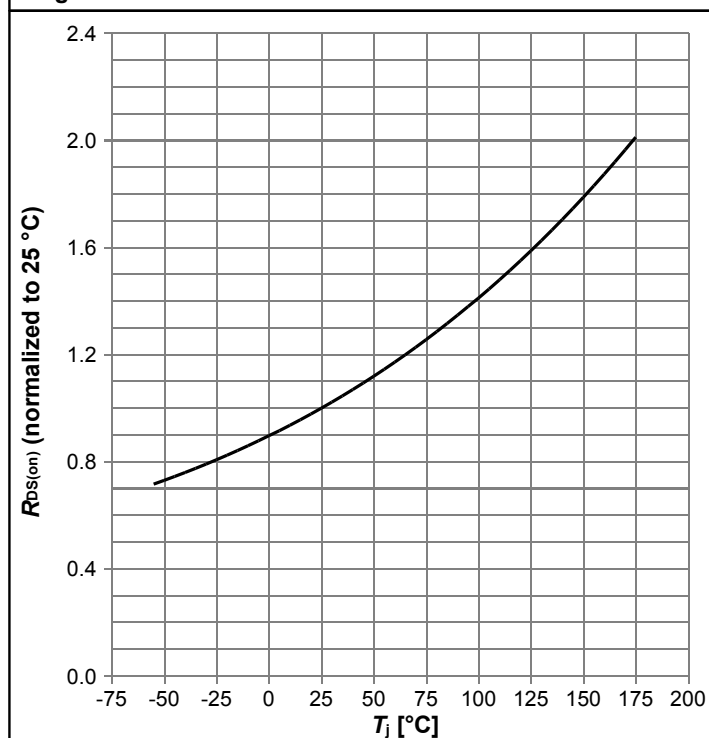
$I_D = f(V_{GS})$, $|V_{DS}| > 2 \cdot I_D / R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. drain-source on resistance



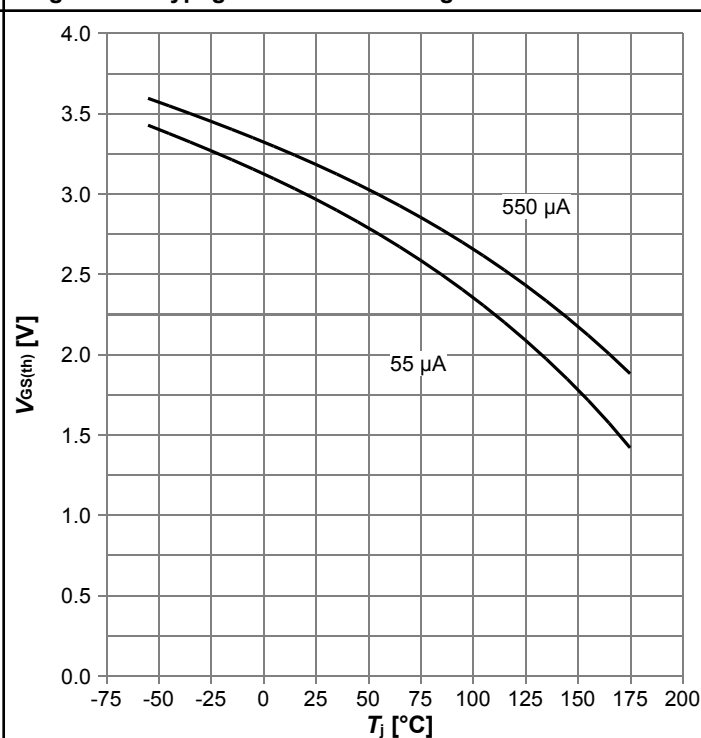
$R_{DS(on)} = f(V_{GS})$, $I_D = 60$ A; parameter: T_j

Diagram 9: Normalized drain-source on resistance



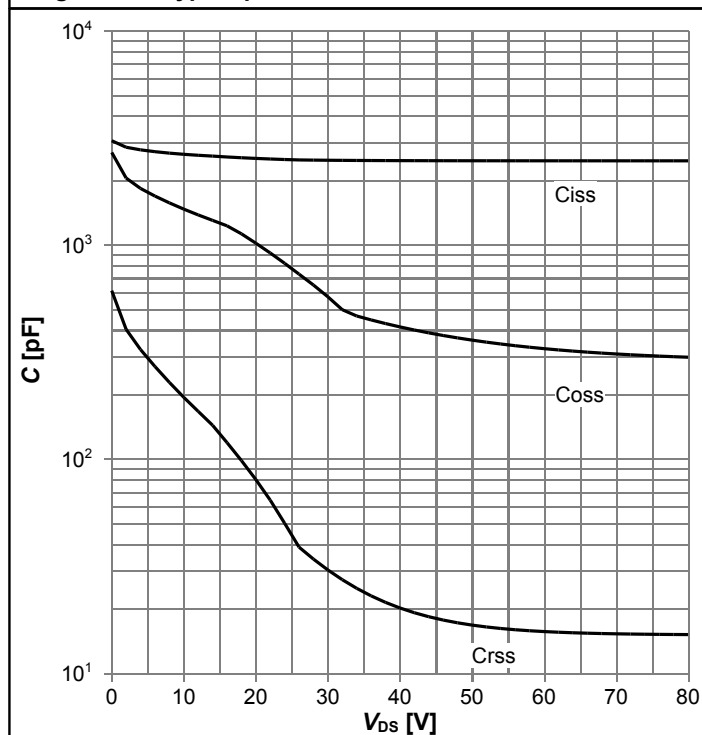
$R_{DS(on)}=f(T_j)$, $I_D=60$ A, $V_{GS}=10$ V

Diagram 10: Typ. gate threshold voltage



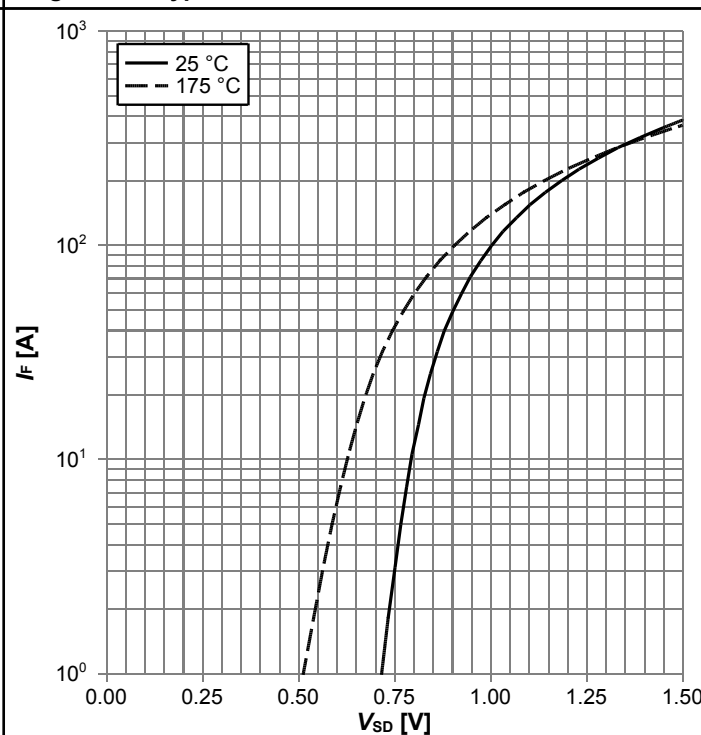
$V_{GS(th)}=f(T_j)$, $V_{GS}=V_{DS}$; parameter: I_D

Diagram 11: Typ. capacitances



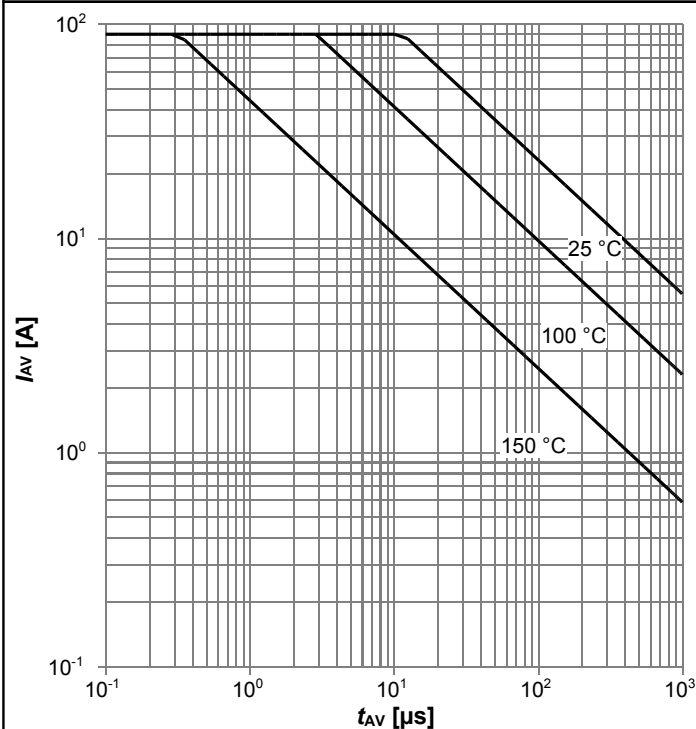
$C=f(V_{DS})$; $V_{GS}=0$ V; $f=1$ MHz

Diagram 12: Typ. forward characteristics of reverse diode



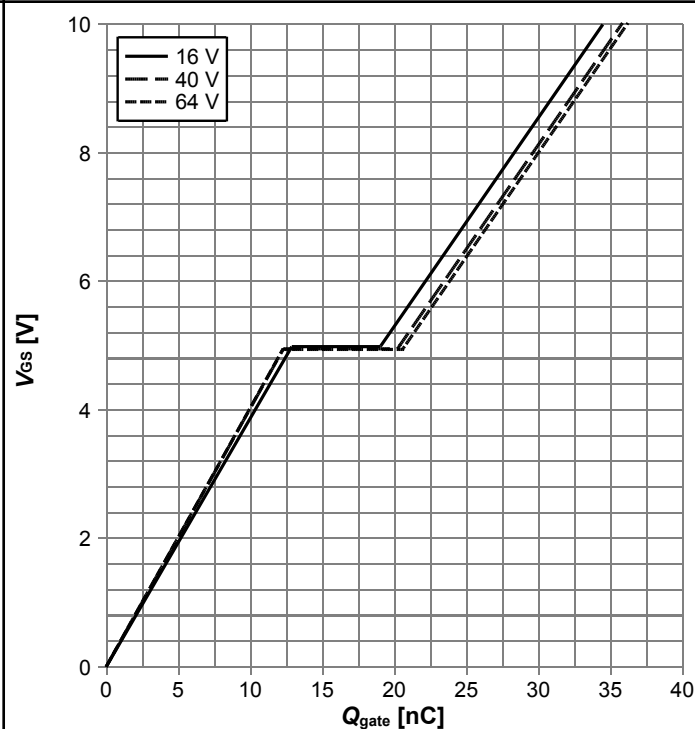
$I_F=f(V_{SD})$; parameter: T_j

Diagram 13: Avalanche characteristics



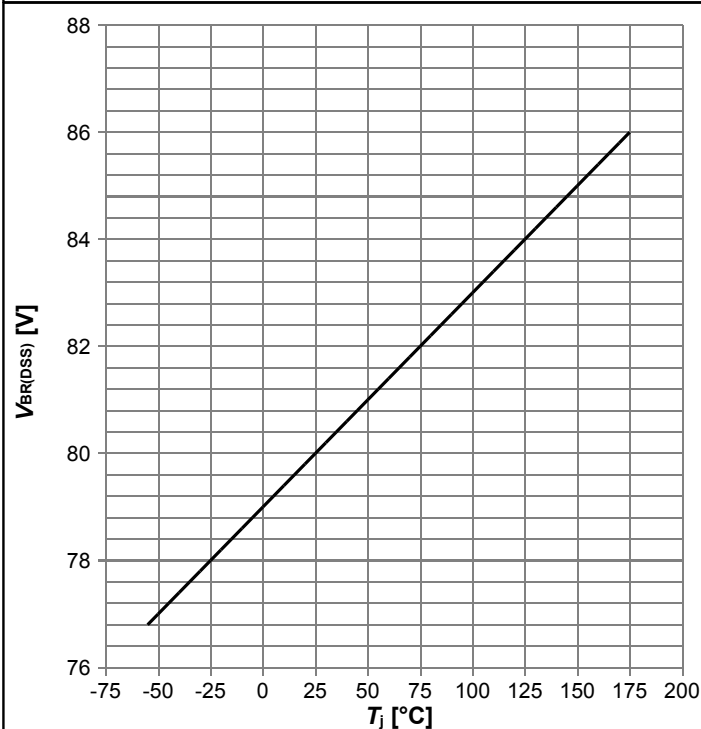
$I_{AS}=f(t_{AV})$; $R_{GS}=25\ \Omega$; parameter: $T_{j,start}$

Diagram 14: Typ. gate charge



$V_{GS}=f(Q_{gate})$, $I_D=60\text{ A}$ pulsed, $T_j=25\text{ °C}$; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage

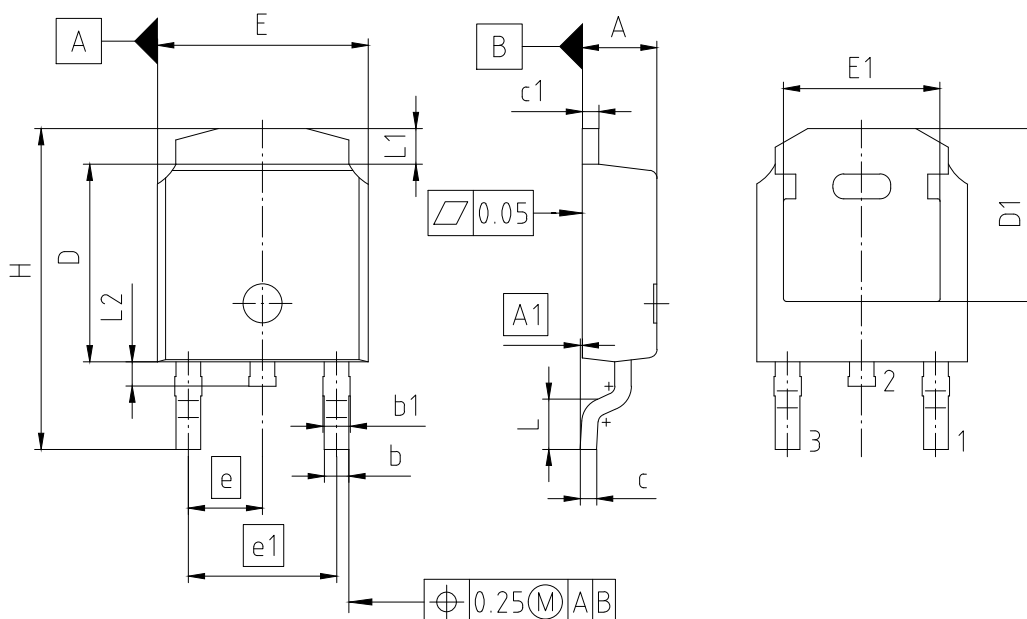


$V_{BR(DSS)}=f(T_j)$; $I_D=1\text{ mA}$

Diagram Gate charge waveforms



5 Package Outlines



PACKAGE - GROUP NUMBER: PG-TO252-3-U01		
DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	2.18	2.39
A1	0.00	0.13
b	0.64	0.89
b1	0.76	1.14
c	0.46	0.61
c1	0.40	0.89
D	5.97	6.22
D1	5.21	---
E	6.35	6.73
E1	4.32	---
e	2.29	
e1	4.58	
N	3	
H	9.40	10.41
L	1.40	1.78
L1	0.89	1.27
L2	0.50	1.02

Figure 1 Outline PG-TO252-3, dimensions in mm

Revision History

IPD055N08NF2S

Revision: 2022-10-10, Rev. 2.2

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2022-02-08	Release of final version
2.1	2022-05-24	Update Diagram 15
2.2	2022-10-10	Update package outline drawing

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