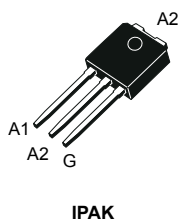


4 A - Triac in IPAK package



Features

- 4 A Triac
- $V_{DRM} / V_{RRM} = 600 \text{ V}$ and $V_{DSM} / V_{RSM} = 750 \text{ V}$
- 125 °C maximum junction temperature T_j
- IPAK package
- 4 quadrants triacs with $I_{GT} = 25 \text{ mA}$
- Halogen-free molding, lead-free plating
- ECOPACK2 compliant

Applications

- Actuators
- Heating elements
- Inrush current limiting circuits

Description

The Z0410MH series is 4 A Triac housed in compact through-hole IPAK package. This 4 quadrants device is suited to home appliances or power tools and industrial systems and drives loads up to 4 A.

Product status link

[Z0410MH](#)

Product summary

$I_{T(RMS)}$	4 A
V_{DSM}/V_{RSM}	750 V
I_{GT}	25 mA
$T_j \text{ max.}$	125 °C

1 Characteristics

Table 1. Absolute maximum ratings (limiting values)

Symbol	Parameter		Value	Unit
$I_{T(RMS)}$	RMS on-state current (full sine wave)	$T_c = 107\text{ °C}$	4	A
I_{TSM}	Non repetitive surge peak on-state current (full cycle, T_j initial = 25 °C)	$t = 16.7\text{ ms}$	16	A
		$t = 20\text{ ms}$	15	
I^2t	I^2t value for fusing	$t_p = 10\text{ ms}$	1.5	A ² s
di/dt	Critical rate of rise of on-state current, $I_G = 2 \times I_{GT}$, $t_r \leq 100\text{ ns}$, $f = 120\text{ Hz}$	$T_j = 125\text{ °C}$	50	A/ μ s
V_{DRM}/V_{RRM}	Repetitive peak off-state voltage	$T_j = 125\text{ °C}$	600	V
V_{DSM}/V_{RSM}	Non Repetitive peak off-state voltage, 10 ms		750	V
I_{GM}	Maximum peak gate current	$t_p = 20\text{ }\mu\text{s}$, $T_j = 125\text{ °C}$	1.2	A
P_{GM}	Maximum gate power dissipation		0.5	W
T_{stg}	Storage temperature range		-40 to +125	°C
T_j	Operating junction temperature range		-40 to +125	°C
T_L	Maximum lead temperature for soldering during 10 s		260	°C

Table 2. Electrical characteristics ($T_j = 25\text{ °C}$, unless otherwise specified)

Symbol	Test conditions		Value	Unit
$I_{GT}^{(1)}$	$V_D = 12\text{ V}$, $R_L = 33\text{ }\Omega$	Max.	25	mA
V_{GT}	$V_D = 12\text{ V}$, $R_L = 33\text{ }\Omega$	Max.	1.3	V
V_{GD}	$V_D = V_{DRM}$, $R_L = 3.3\text{ k}\Omega$	$T_j = 125\text{ °C}$ Min.	0.2	V
I_L	$I_G = 1.2 \times I_{GT}$	I-III-IV Max.	25	mA
		II Max.	50	mA
$I_H^{(2)}$	$I_T = 500\text{ mA}$, gate open	Max.	25	mA
$dV/dt^{(2)}$	$V_D = 67\% V_{DRM}$; $V_R = 67\% V_{RRM}$, gate open	$T_j = 110\text{ °C}$ Min.	200	V/ μ s
$(dV/dt)_c^{(2)}$	$(di/dt)_c = 1.8\text{ A/ms}$	$T_j = 110\text{ °C}$ Min.	5	V/ μ s

1. For both polarities of OUT pin referenced to COM pin.

2. For both polarities of A2 referenced to A1.

Table 3. Static characteristics

Symbol	Test conditions	T_j		Value	Unit
$V_{TM}^{(1)}$	$I_{TM} = 5.5\text{ A}$, $t_p = 380\text{ }\mu\text{s}$	25 °C	Max.	2	V
$V_{TO}^{(1)}$	Threshold voltage	125 °C	Max.	0.95	V
$R_D^{(1)}$	Dynamic resistance	125 °C	Max.	180	m Ω
I_{DRM}/I_{RRM}	$V_D = V_R = V_{DRM} = V_{RRM}$	25 °C	Max.	5	μ A
		125 °C		0.5	mA

1. For both polarities of A2 referenced to A1.

Table 4. Thermal resistance

Symbol	Parameter		Value	Unit
$R_{th(j-c)}$	Junction to case (AC)	Max.	3	°C/W
$R_{th(j-a)}$	Junction to ambient	Typ.	70	°C/W

1.1 Characteristics (curves)

Figure 1. Maximum power dissipation versus on-state RMS current (full cycle)

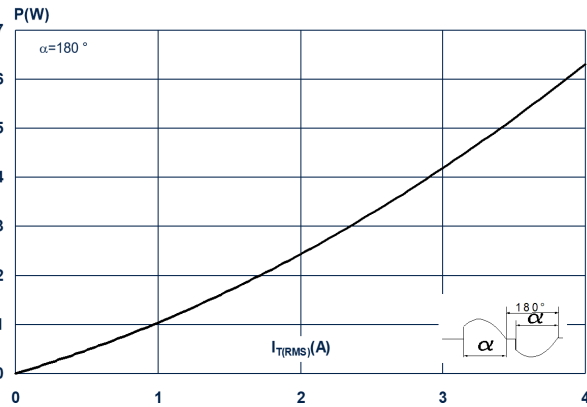


Figure 2. Average and DC on-state current versus case temperature

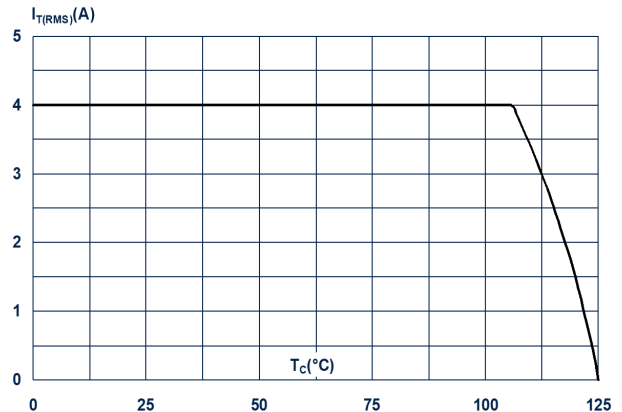


Figure 3. On-state RMS current versus ambient temperature (full cycle)

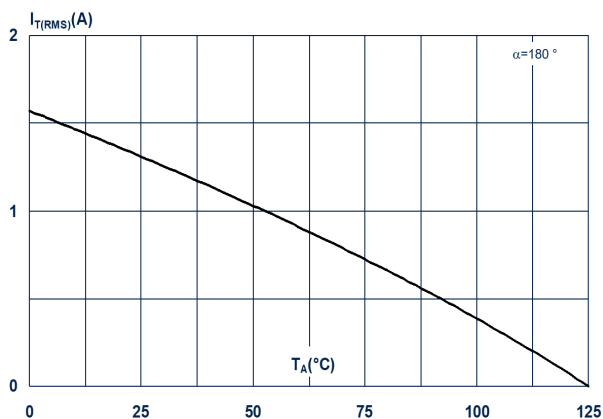


Figure 4. Relative variation of thermal impedance versus pulse duration

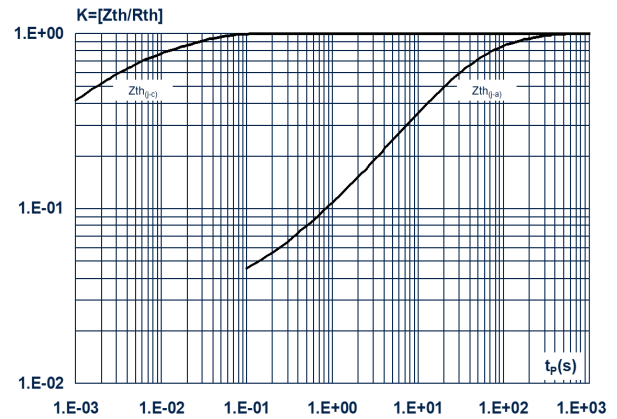


Figure 5. Relative variation of gate triggering current and voltage versus junction temperature (typical values)

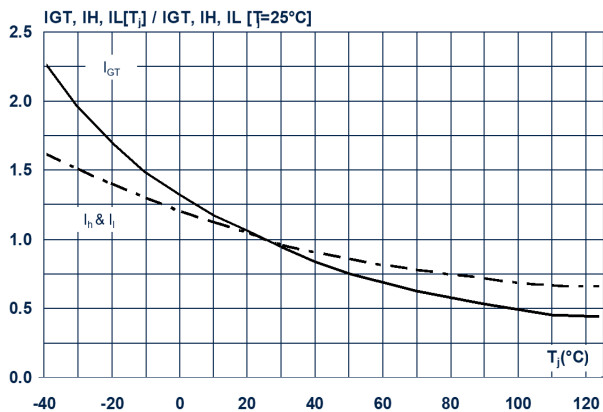


Figure 6. Surge peak on-state current versus number of cycles

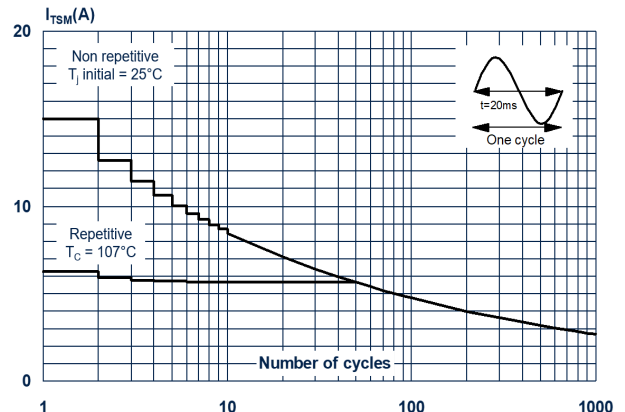


Figure 7. Non repetitive surge peak on-state current for a sinusoidal pulse with width $t_p < 10$ ms and corresponding value of I^2t

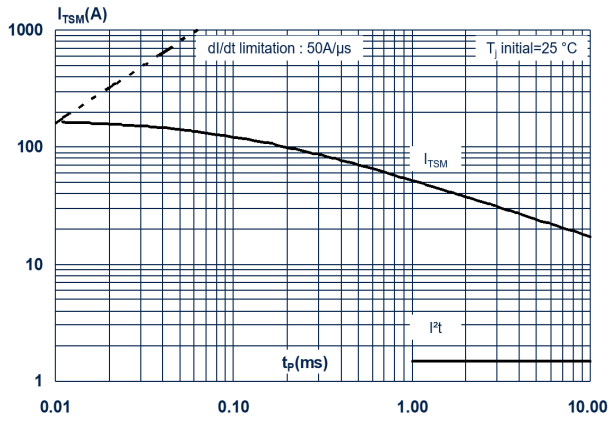


Figure 8. On-state characteristics (maximum values)

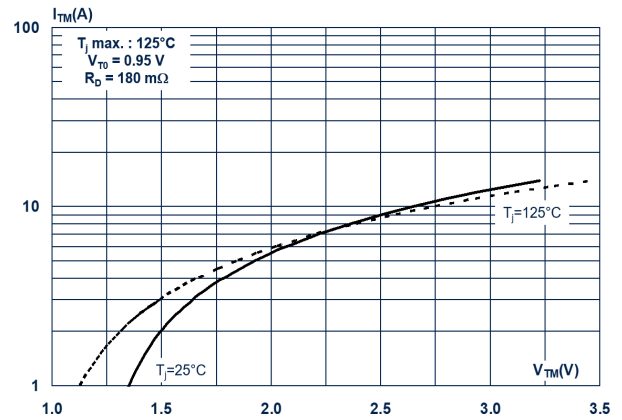


Figure 9. Relative variation of critical rate of decrease of main current versus $(dV/dt)_c$ (typical values)

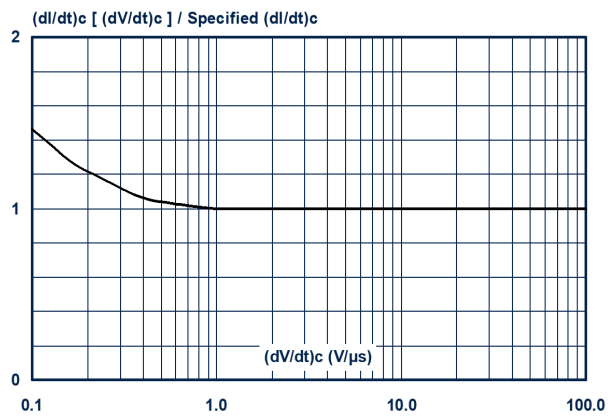


Figure 10. Relative variation of critical rate of decrease of main current versus junction temperature

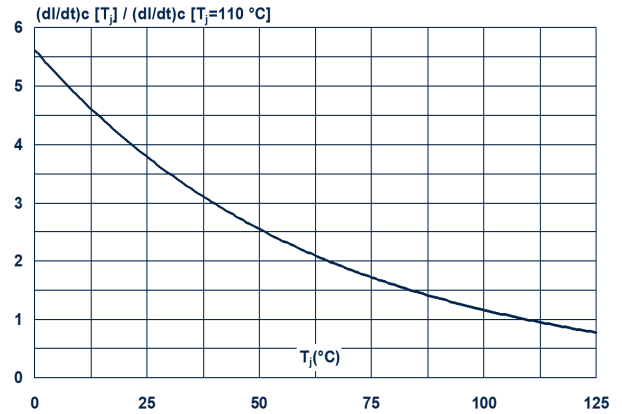
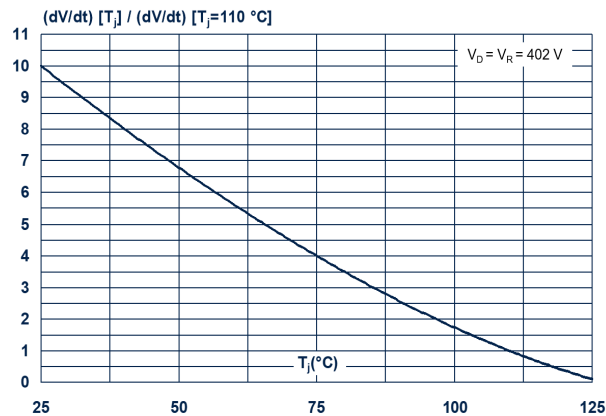


Figure 11. Relative variation of static dV/dt immunity versus junction temperature



2 Ordering information

Figure 12. Ordering information scheme

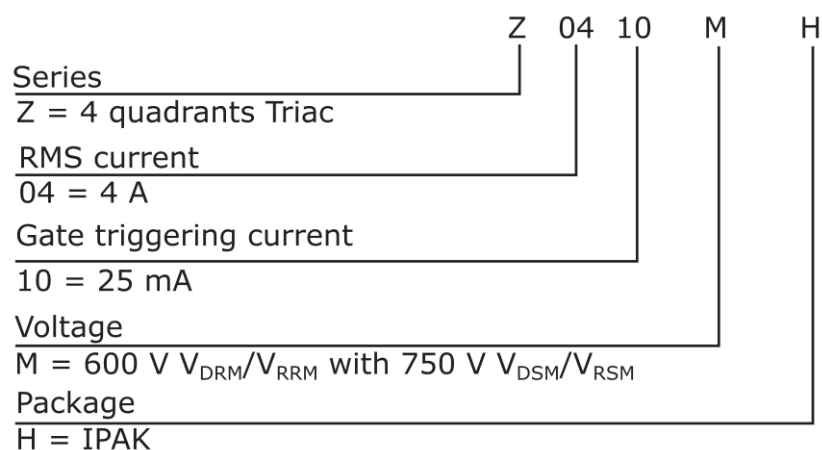


Table 5. Ordering information

Order code	Marking	Package	Weight	Base qty.	Delivery mode
Z0410MH	Z0410MH	IPAK	0.31 g	75	Tube

3 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

3.1 IPAK package information

- Molding compounded resin is halogen free and meets UL94 flammability standard, level V0
- Lead-free package leads plating

Figure 13. IPAK package outline

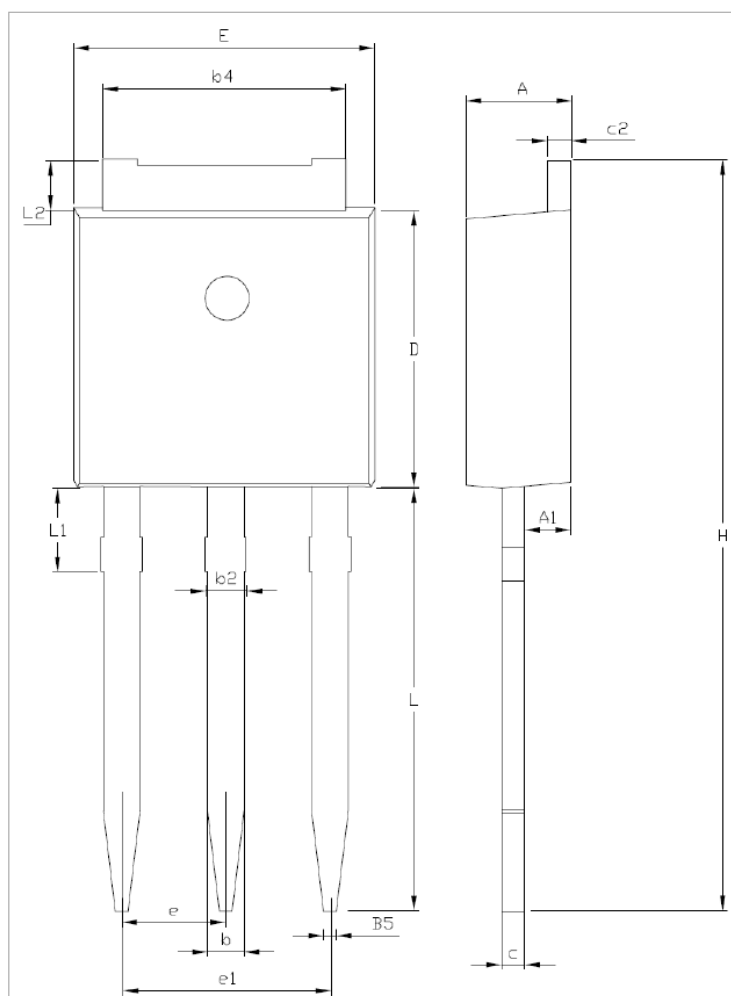


Table 6. IPAK package mechanical data

Ref.	Dimensions					
	MillimetersInches (for reference only)					
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.20		2.40	0.086		0.094
A1	0.90		1.10			0.035
b	0.64		0.90	0.025		0.035
b2			0.95			0.037
b4	5.20		5.43			
B5		0.30			0.012	
c	0.45		0.60			
c2	0.46		0.60			
D	6		6.20			
E	6.40		6.65	0.252		0.262
e		2.28			0.090	
e1	4.40		4.60	0.173		0.181
H		16.10			0.634	
L	9		9.60	0.354		0.377
L1	0.8		1.20	0.031		0.047
L2		0.80	1.25		0.031	0.049
V1		10°			10°	

Revision history

Table 7. Document revision history

Date	Revision	Changes
05-Sep-2022	1	Initial release.

IMPORTANT NOTICE – READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgment.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2022 STMicroelectronics – All rights reserved