



PSMN014-40HLD

N-channel 40 V, 13.6 mOhm, logic level MOSFET in LPAK56D using NextPowerS3 technology

26 September 2022

Product data sheet

1. General description

Dual logic level N-channel MOSFET in an LPAK56D (Dual Power-SO8) package using NextPowerS3 technology.

2. Features and benefits

- Dual MOSFET
- Repetitive avalanche rated
- High reliability LPAK56D package
- Copper-clip, solder die attach
- Qualified to 175 °C

3. Applications

- Brushless DC motor control
- DC-to-DC converters
- High-performance synchronous rectification
- High performance and high efficiency server power supply

4. Quick reference data

Table 1. Quick reference data

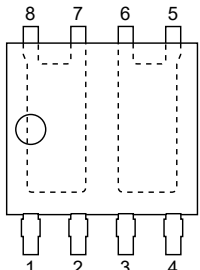
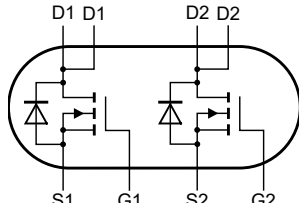
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V _{DS}	drain-source voltage	25 °C ≤ T _j ≤ 175 °C		-	-	40	V
I _D	drain current	V _{GS} = 10 V; T _{mb} = 25 °C; Fig. 2	[1]	-	-	42	A
P _{tot}	total power dissipation	T _{mb} = 25 °C; Fig. 1		-	-	46	W
T _j	junction temperature			-55	-	175	°C
Static characteristics FET1 and FET2							
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 10 A; T _j = 25 °C		7.9	11.4	13.6	mΩ
		V _{GS} = 10 V; I _D = 10 A; T _j = 105 °C		10.9	16	20.4	mΩ
Dynamic characteristics FET1 and FET2							
Q _{GD}	gate-drain charge	I _D = 10 A; V _{DS} = 32 V; V _{GS} = 5 V; T _j = 25 °C		-	1.8	4.2	nC
Q _{G(tot)}	total gate charge	I _D = 10 A; V _{DS} = 32 V; V _{GS} = 10 V; T _j = 25 °C		-	13	19.4	nC
Avalanche Ruggedness FET1 and FET2							
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I _D = 39.9 A; V _{sup} ≤ 40 V; R _{GS} = 50 Ω; V _{GS} = 10 V; T _{j(init)} = 25 °C; Fig. 4	[2] [3]	-	-	10.6	mJ

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Source-drain diode FET1 and FET2						
Q_r	recovered charge	$I_S = 10\text{ A}$; $di_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$; $V_{DS} = 20\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$	[4]	-	16.2	nC

- [1] 42A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.
 [2] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
 [3] Refer to application note AN10273 for further information.
 [4] Includes capacitive recovery

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source1	 LPAK56D; Dual LPAK (SOT1205)	 mbk725
2	G1	gate1		
3	S2	source2		
4	G2	gate2		
5	D2	drain2		
6	D2	drain2		
7	D1	drain1		
8	D1	drain1		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN014-40HLD	LPAK56D; Dual LPAK	plastic, single ended surface mounted package (LPAK56D); 8 leads	SOT1205

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN014-40HLD	14DS40H

8. Limiting values

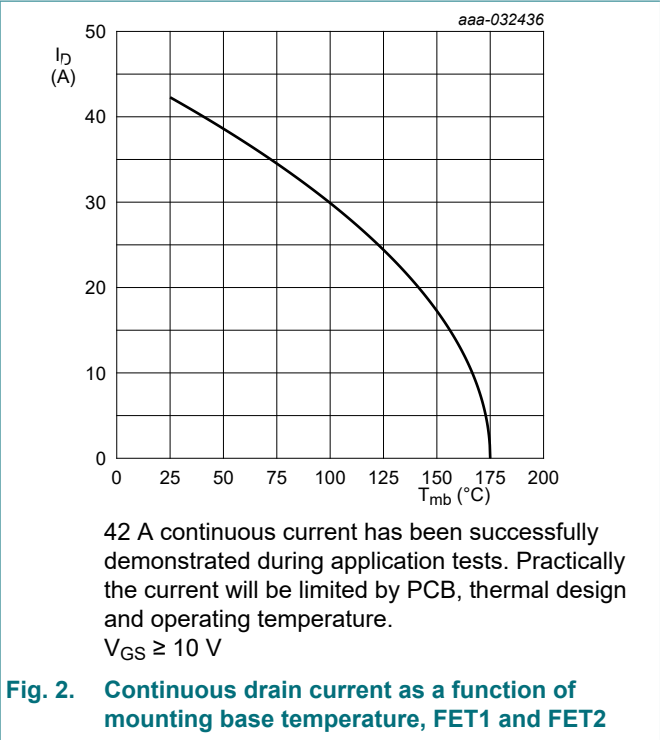
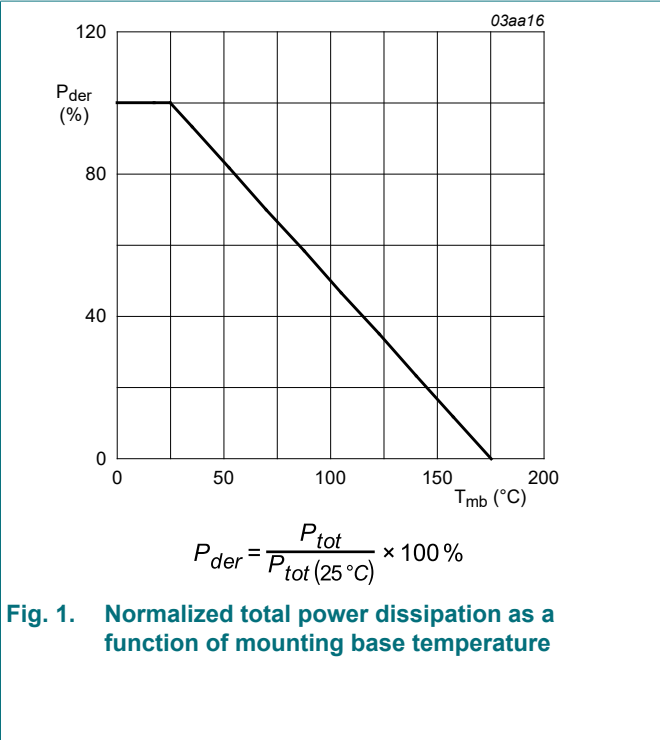
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$25\text{ }^\circ\text{C} \leq T_j \leq 175\text{ }^\circ\text{C}$	-	40	V
V_{GS}	gate-source voltage	DC; $T_j = 25\text{ }^\circ\text{C}$	-20	20	V
P_{tot}	total power dissipation	$T_{mb} = 25\text{ }^\circ\text{C}$; Fig. 1	-	46	W

Symbol	Parameter	Conditions		Min	Max	Unit
I _D	drain current	V _{GS} = 10 V; T _{mb} = 25 °C; Fig. 2	[1]	-	42	A
		V _{GS} = 10 V; T _{mb} = 100 °C; Fig. 2		-	30	A
I _{DM}	peak drain current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C; Fig. 3		-	169	A
T _{stg}	storage temperature			-55	175	°C
T _j	junction temperature			-55	175	°C
Source-drain diode FET1 and FET2						
I _S	source current	T _{mb} = 25 °C		-	42	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C		-	169	A
Avalanche Ruggedness FET1 and FET2						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I _D = 39.9 A; V _{sup} ≤ 40 V; R _{GS} = 50 Ω; V _{GS} = 10 V; T _{j(init)} = 25 °C; Fig. 4	[2] [3]	-	10.6	mJ
I _{AS}	non-repetitive avalanche current	V _{sup} = 40 V; V _{GS} = 10 V; T _{j(init)} = 25 °C; R _{GS} = 50 Ω; Fig. 4	[4]	-	39.9	A

- [1] 42A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.
- [2] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
- [3] Refer to application note AN10273 for further information.
- [4] Protected by 100% test



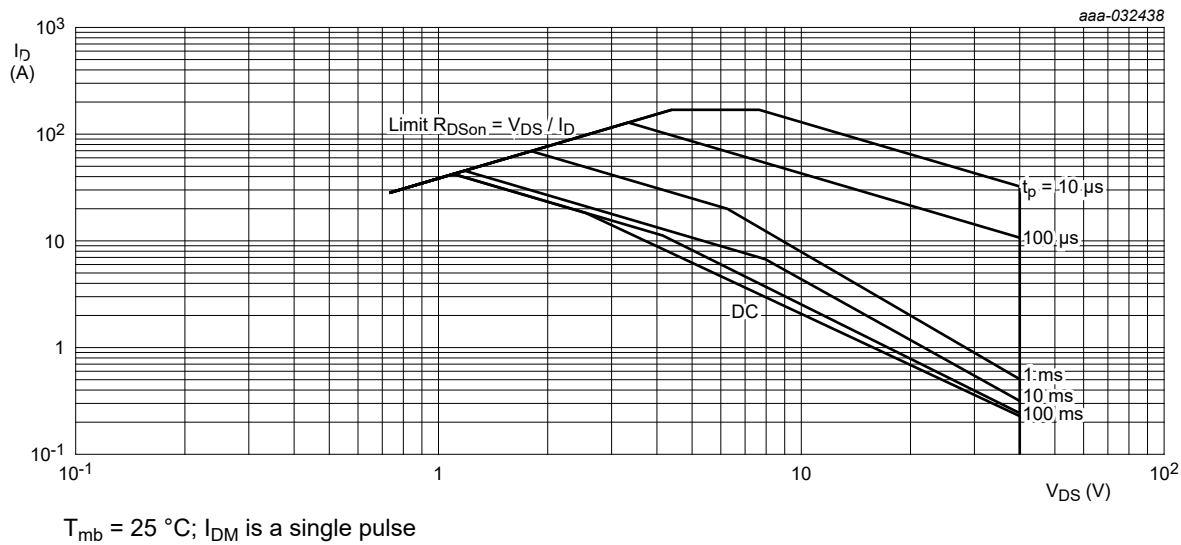


Fig. 3. Safe operating area; continuous and peak drain current as a function of drain-source voltage, FET1 and FET2

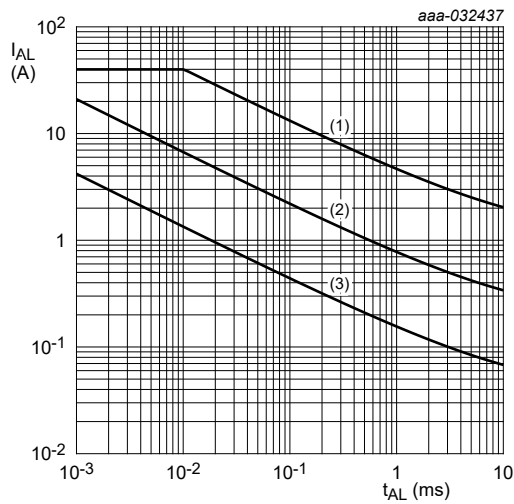
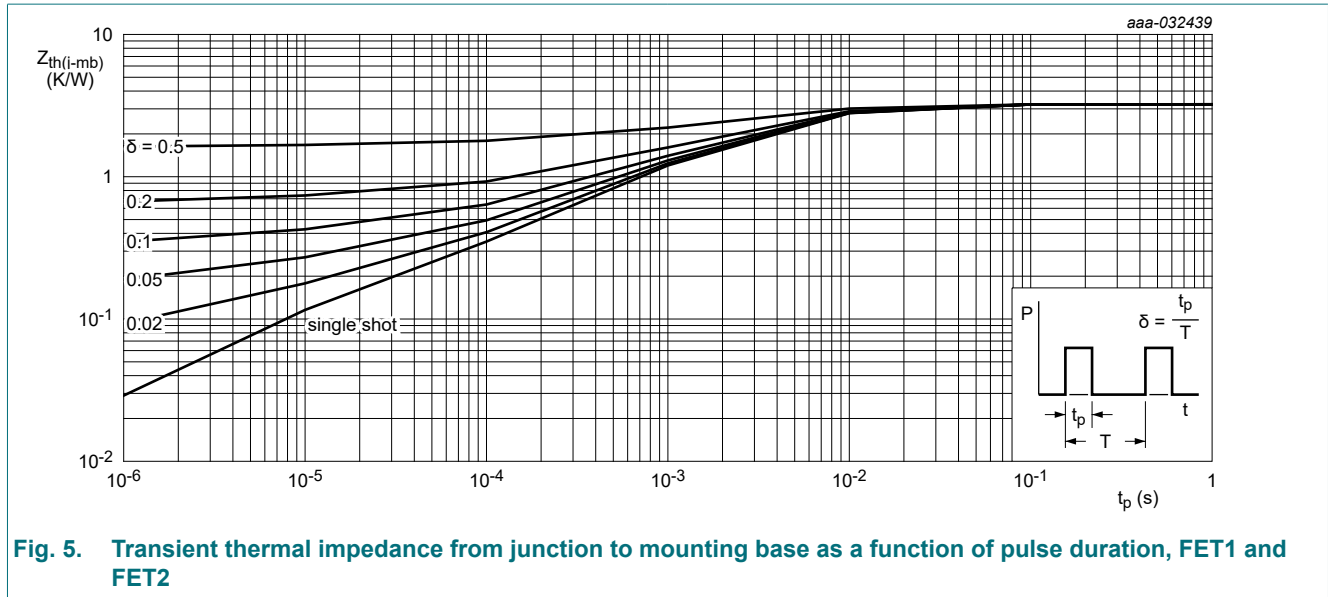


Fig. 4. Avalanche rating; avalanche current as a function of avalanche time, FET1 and FET2

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	3	3.23	K/W



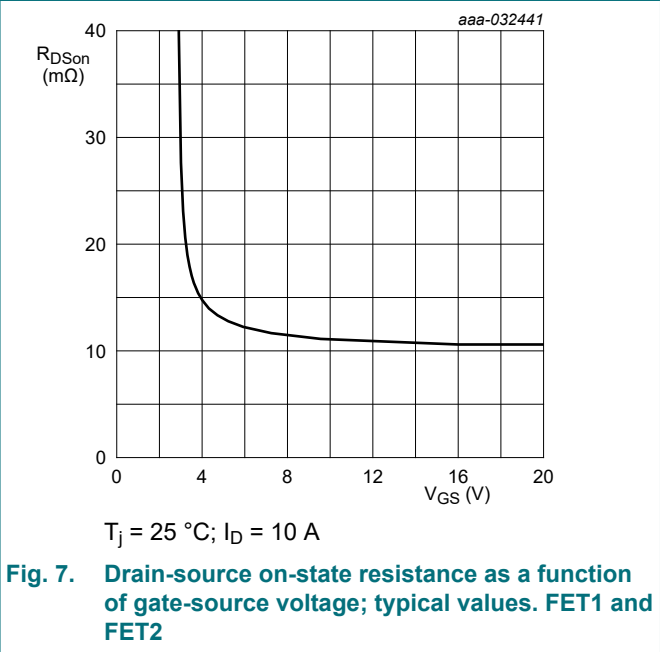
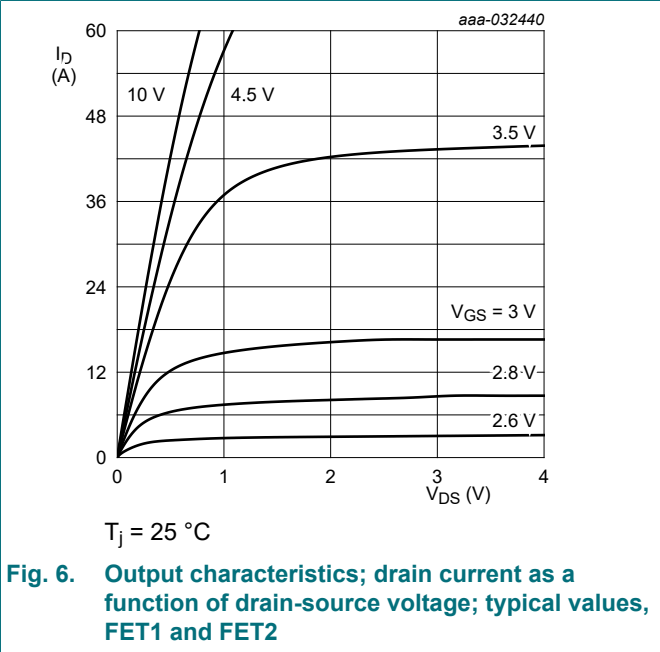
10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics FET1 and FET2						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A$; $V_{GS} = 0 V$; $T_J = 25 ^\circ C$	40	43	-	V
		$I_D = 250 \mu A$; $V_{GS} = 0 V$; $T_J = -40 ^\circ C$	-	40.5	-	V
		$I_D = 250 \mu A$; $V_{GS} = 0 V$; $T_J = -55 ^\circ C$	36	40	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 mA$; $V_{DS}=V_{GS}$; $T_J = 25 ^\circ C$; Fig. 9 ; Fig. 10	1.5	1.85	2.2	V
		$I_D = 1 mA$; $V_{DS}=V_{GS}$; $T_J = 175 ^\circ C$; Fig. 10	0.7	-	-	V
		$I_D = 1 mA$; $V_{DS}=V_{GS}$; $T_J = -55 ^\circ C$; Fig. 10	-	-	2.6	V
I_{DSS}	drain leakage current	$V_{DS} = 40 V$; $V_{GS} = 0 V$; $T_J = 25 ^\circ C$	-	0.01	5	μA
		$V_{DS} = 16 V$; $V_{GS} = 0 V$; $T_J = 125 ^\circ C$	-	0.14	10	μA
		$V_{DS} = 40 V$; $V_{GS} = 0 V$; $T_J = 175 ^\circ C$	-	26	500	μA
I_{GSS}	gate leakage current	$V_{GS} = -10 V$; $V_{DS} = 0 V$; $T_J = 25 ^\circ C$	-	2	100	nA
		$V_{GS} = 16 V$; $V_{DS} = 0 V$; $T_J = 25 ^\circ C$	-	2	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 V$; $I_D = 10 A$; $T_J = 25 ^\circ C$	7.9	11.4	13.6	m Ω
		$V_{GS} = 10 V$; $I_D = 10 A$; $T_J = 105 ^\circ C$	10.9	16	20.4	m Ω
		$V_{GS} = 10 V$; $I_D = 10 A$; $T_J = 125 ^\circ C$	12	17.4	21.9	m Ω
		$V_{GS} = 10 V$; $I_D = 10 A$; $T_J = 175 ^\circ C$	14.5	20.9	26.4	m Ω
		$V_{GS} = 4.5 V$; $I_D = 10 A$; $T_J = 25 ^\circ C$	9.8	14.1	16.9	m Ω
		$V_{GS} = 4.5 V$; $I_D = 10 A$; $T_J = 105 ^\circ C$	13.5	20	25.4	m Ω
		$V_{GS} = 4.5 V$; $I_D = 10 A$; $T_J = 125 ^\circ C$	14.8	21.6	27.2	m Ω
		$V_{GS} = 4.5 V$; $I_D = 10 A$; $T_J = 175 ^\circ C$	18	26.6	32.8	m Ω
R_G	gate resistance	$f = 1 MHz$; $T_J = 25 ^\circ C$	0.7	1.8	4.2	Ω

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Dynamic characteristics FET1 and FET2							
Q _{G(tot)}	total gate charge	I _D = 10 A; V _{DS} = 32 V; V _{GS} = 10 V; T _J = 25 °C		-	13	19.4	nC
		I _D = 10 A; V _{DS} = 32 V; V _{GS} = 5 V; T _J = 25 °C		-	6.8	10.2	nC
Q _{GS}	gate-source charge			-	2.3	3.8	nC
Q _{GD}	gate-drain charge			-	1.8	4.2	nC
C _{iss}	input capacitance	V _{DS} = 25 V; V _{GS} = 0 V; f = 1 MHz; T _J = 25 °C; Fig. 11		-	848	1160	pF
C _{oss}	output capacitance			-	280	420	pF
C _{rss}	reverse transfer capacitance			-	39	84	pF
t _{d(on)}	turn-on delay time	V _{DS} = 32 V; R _L = 3.2 Ω; V _{GS} = 5 V; R _{G(ext)} = 5 Ω; T _J = 25 °C		-	6.5	-	ns
t _r	rise time			-	9.7	-	ns
t _{d(off)}	turn-off delay time			-	10.1	-	ns
t _f	fall time			-	7.8	-	ns
Source-drain diode FET1 and FET2							
V _{SD}	source-drain voltage	I _S = 10 A; V _{GS} = 0 V; T _J = 25 °C; Fig. 12		-	0.81	1	V
t _{rr}	reverse recovery time	I _S = 10 A; dI _S /dt = -100 A/μs; V _{GS} = 0 V; V _{DS} = 20 V; T _J = 25 °C		-	21.5	-	ns
Q _r	recovered charge		[1]	-	16.2	-	nC

[1] Includes capacitive recovery



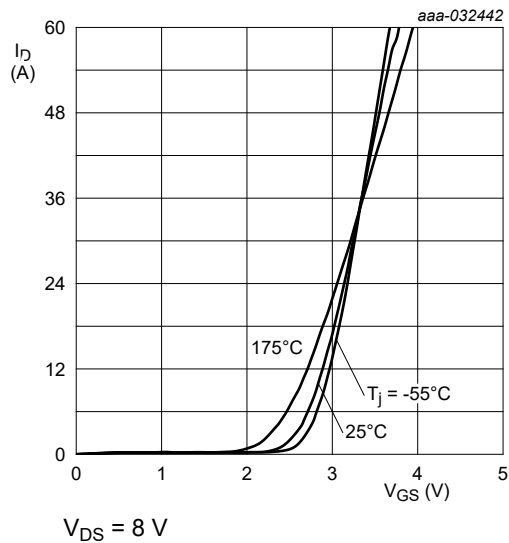


Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values, FET1 and FET2

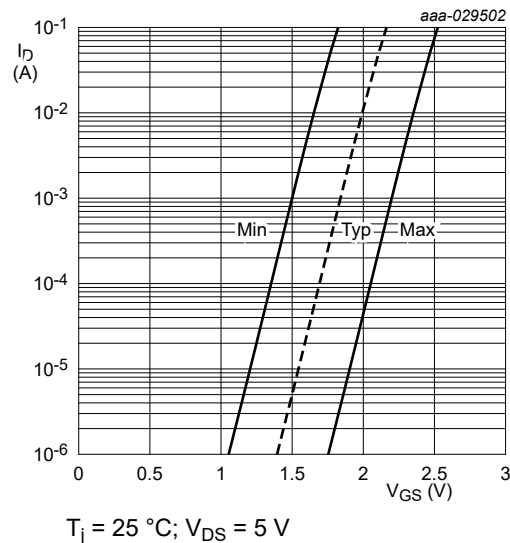


Fig. 9. Sub-threshold drain current as a function of gate-source voltage, FET1 and FET2

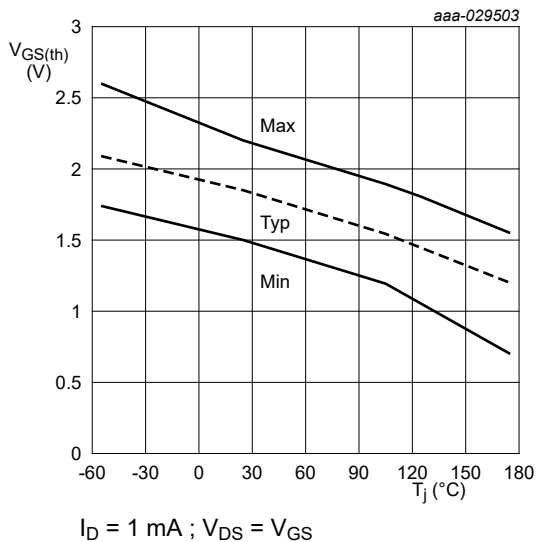


Fig. 10. Gate-source threshold voltage as a function of junction temperature, FET1 and FET2

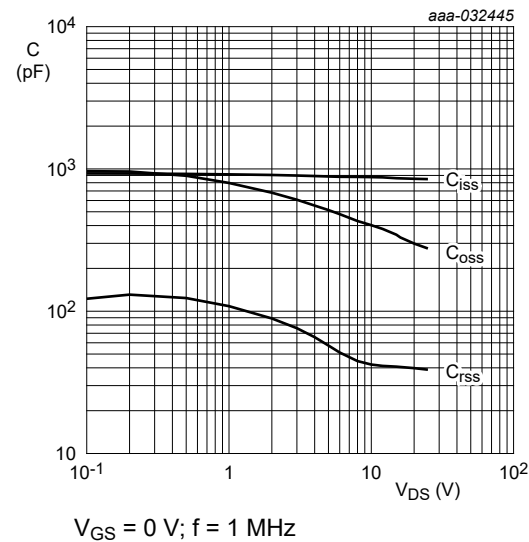
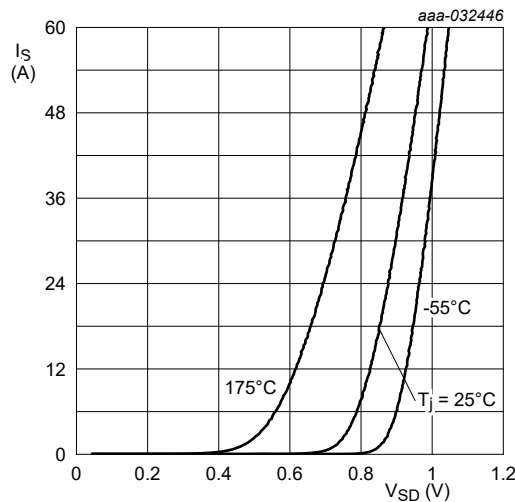


Fig. 11. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values, FET1 and FET2



$V_{GS} = 0\text{ V}$

Fig. 12. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values FET1 and FET2

11. Package outline

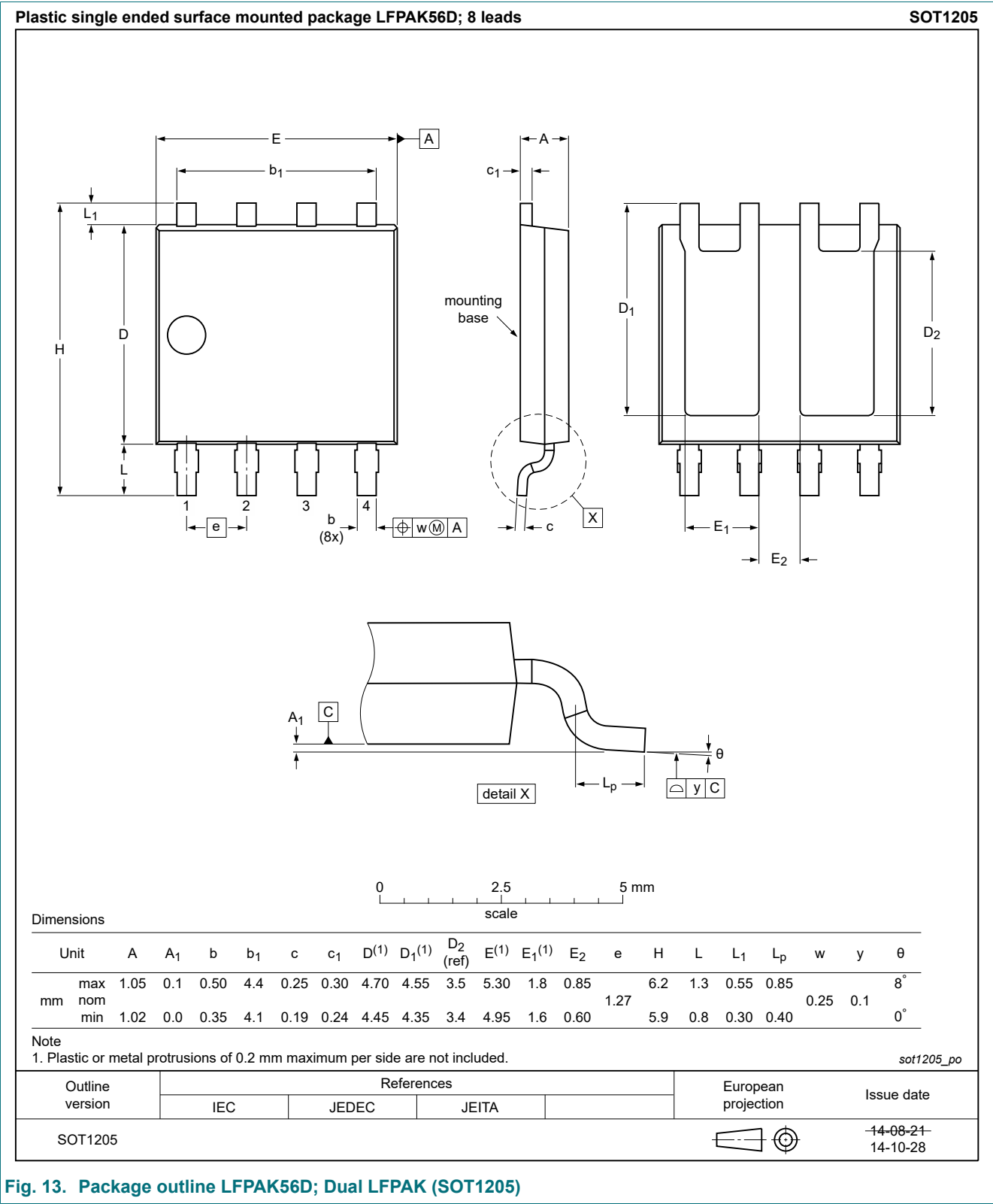


Fig. 13. Package outline LPAK56D; Dual LPAK (SOT1205)

12. Soldering

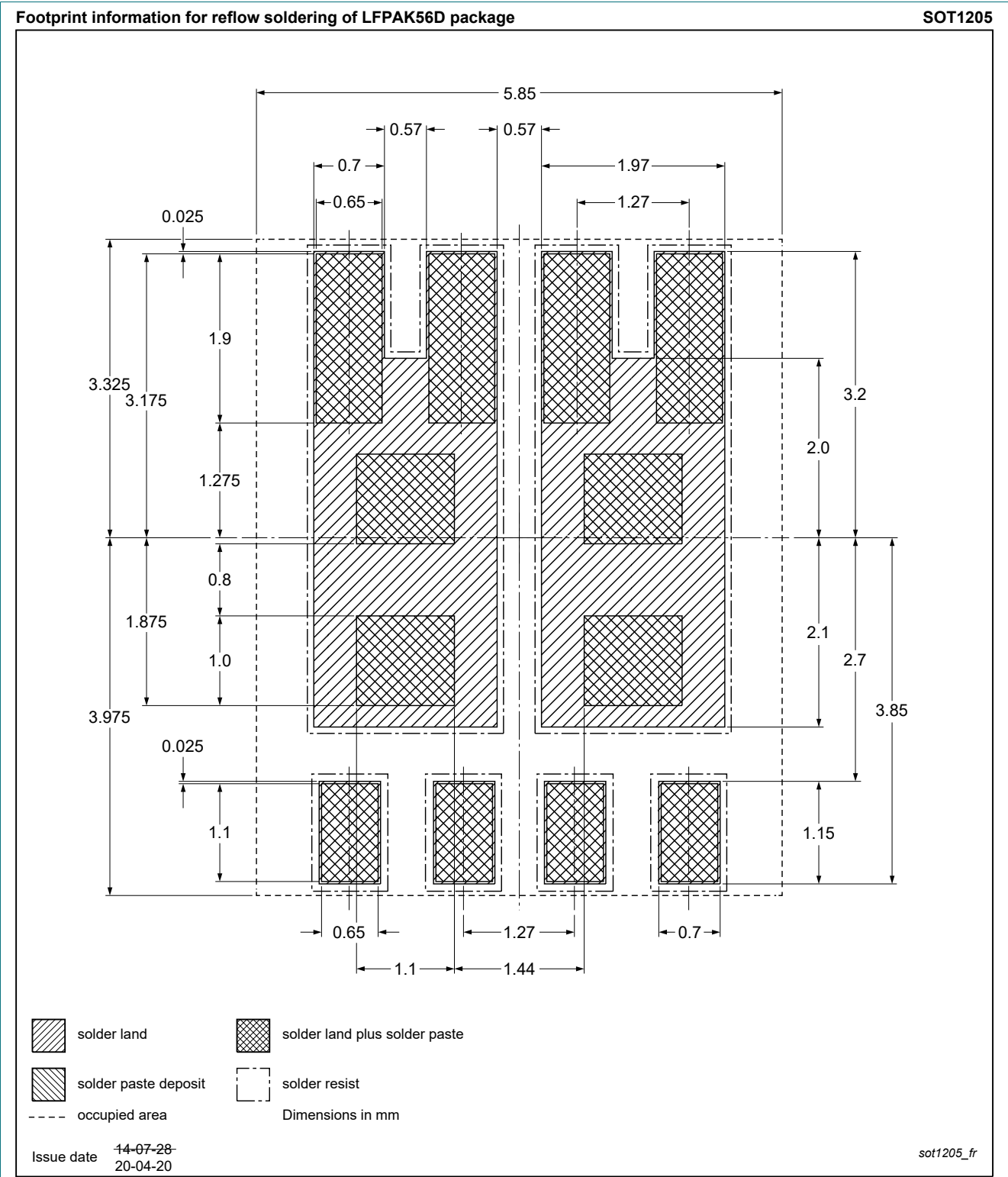


Fig. 14. Reflow soldering footprint for LPAK56D; Dual LPAK (SOT1205)

13. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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