



# PSMN014-60HS

N-channel 60 V, 14 mOhm, standard level MOSFET in LPAK56D using TrenchMOS technology

26 September 2022

Product data sheet

## 1. General description

Dual standard level N-channel MOSFET in an LPAK56D (Dual Power-SO8) package using TrenchMOS technology.

## 2. Features and benefits

- Dual MOSFET
- Repetitive avalanche rated
- High reliability LPAK56D package
- Copper-clip, solder die attach
- Qualified to 175 °C

## 3. Applications

- Brushless DC motor control
- DC-to-DC converters
- High-performance synchronous rectification
- High performance and high efficiency server power supply

## 4. Quick reference data

Table 1. Quick reference data

| Table 7. Quick reference data         |                                              |                                                                                                                                                  |         |     |      |      |      |
|---------------------------------------|----------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------|---------|-----|------|------|------|
| Symbol                                | Parameter                                    | Conditions                                                                                                                                       |         | Min | Typ  | Max  | Unit |
| V <sub>DS</sub>                       | drain-source voltage                         | 25 °C ≤ T <sub>j</sub> ≤ 175 °C                                                                                                                  |         | -   | -    | 60   | V    |
| I <sub>D</sub>                        | drain current                                | V <sub>GS</sub> = 10 V; T <sub>mb</sub> = 25 °C; <a href="#">Fig. 2</a>                                                                          | [1]     | -   | -    | 30   | A    |
| P <sub>tot</sub>                      | total power dissipation                      | T <sub>mb</sub> = 25 °C; <a href="#">Fig. 1</a>                                                                                                  |         | -   | -    | 53   | W    |
| T <sub>j</sub>                        | junction temperature                         |                                                                                                                                                  |         | -55 | -    | 175  | °C   |
| Static characteristics FET1 and FET2  |                                              |                                                                                                                                                  |         |     |      |      |      |
| R <sub>DSon</sub>                     | drain-source on-state resistance             | V <sub>GS</sub> = 10 V; I <sub>D</sub> = 10 A; T <sub>j</sub> = 25 °C; <a href="#">Fig. 11</a>                                                   |         | -   | 11.3 | 14   | mΩ   |
|                                       |                                              | V <sub>GS</sub> = 10 V; I <sub>D</sub> = 10 A; T <sub>j</sub> = 175 °C; <a href="#">Fig. 11</a> ; <a href="#">Fig. 12</a>                        |         | -   | 25.3 | 31.4 | mΩ   |
| Dynamic characteristics FET1 and FET2 |                                              |                                                                                                                                                  |         |     |      |      |      |
| Q <sub>GD</sub>                       | gate-drain charge                            | I <sub>D</sub> = 10 A; V <sub>DS</sub> = 48 V; V <sub>GS</sub> = 20 V; T <sub>j</sub> = 25 °C; <a href="#">Fig. 13</a> ; <a href="#">Fig. 14</a> |         | -   | 8.1  | -    | nC   |
| Q <sub>G(tot)</sub>                   | total gate charge                            | I <sub>D</sub> = 10 A; V <sub>DS</sub> = 48 V; V <sub>GS</sub> = 10 V; T <sub>j</sub> = 25 °C; <a href="#">Fig. 13</a> ; <a href="#">Fig. 14</a> |         | -   | 23.6 | -    | nC   |
| Avalanche ruggedness FET1 and FET2    |                                              |                                                                                                                                                  |         |     |      |      |      |
| E <sub>DS(AL)S</sub>                  | non-repetitive drain-source avalanche energy | I <sub>D</sub> = 30 A; V <sub>sup</sub> ≤ 60 V; V <sub>GS</sub> = 10 V; T <sub>j(init)</sub> = 25 °C; <a href="#">Fig. 4</a>                     | [2] [3] | -   | -    | 55   | mJ   |

N-channel 60 V, 14 mOhm, standard level MOSFET in LFAK56D using TrenchMOS technology

| Symbol                                  | Parameter        | Conditions                                                                                                                                      | Min | Typ  | Max | Unit |
|-----------------------------------------|------------------|-------------------------------------------------------------------------------------------------------------------------------------------------|-----|------|-----|------|
| <b>Source-drain diode FET1 and FET2</b> |                  |                                                                                                                                                 |     |      |     |      |
| $Q_r$                                   | recovered charge | $I_S = 10\text{ A}$ ; $dI_S/dt = -100\text{ A}/\mu\text{s}$ ; $V_{GS} = 0\text{ V}$ ; $V_{DS} = 30\text{ V}$ ; $T_j = 25\text{ }^\circ\text{C}$ | -   | 24.6 | -   | nC   |

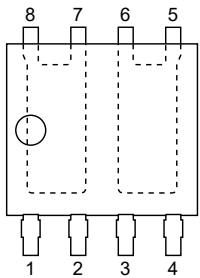
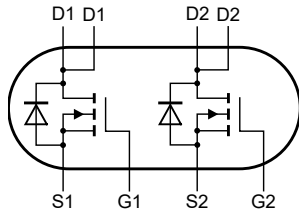
[1] Continuous current is limited by package

[2] Refer to application note AN10273 for further information

[3] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C

## 5. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description | Simplified outline                                                                                                               | Graphic symbol                                                                                    |
|-----|--------|-------------|----------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------|
| 1   | S1     | source1     |  <p><b>LFAK56D; Dual<br/>LFAK (SOT1205)</b></p> |  <p>mbk725</p> |
| 2   | G1     | gate1       |                                                                                                                                  |                                                                                                   |
| 3   | S2     | source2     |                                                                                                                                  |                                                                                                   |
| 4   | G2     | gate2       |                                                                                                                                  |                                                                                                   |
| 5   | D2     | drain2      |                                                                                                                                  |                                                                                                   |
| 6   | D2     | drain2      |                                                                                                                                  |                                                                                                   |
| 7   | D1     | drain1      |                                                                                                                                  |                                                                                                   |
| 8   | D1     | drain1      |                                                                                                                                  |                                                                                                   |

## 6. Ordering information

Table 3. Ordering information

| Type number  | Package               |                                                                  |         |
|--------------|-----------------------|------------------------------------------------------------------|---------|
|              | Name                  | Description                                                      | Version |
| PSMN014-60HS | LFAK56D;<br>Dual LFAK | plastic, single ended surface mounted package (LFAK56D); 8 leads | SOT1205 |

## 7. Marking

Table 4. Marking codes

| Type number  | Marking code |
|--------------|--------------|
| PSMN014-60HS | 14RS60H      |

## 8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

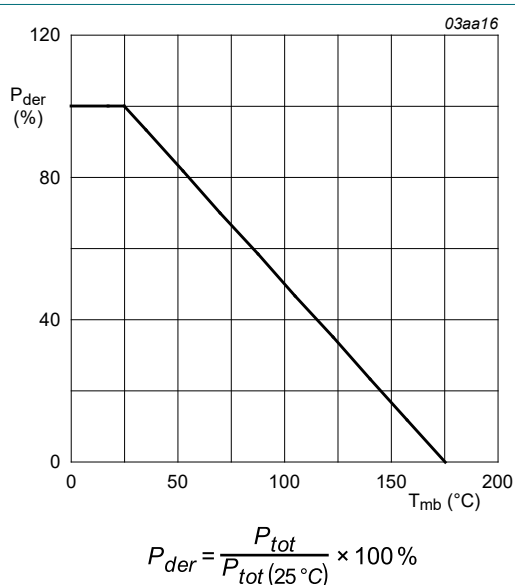
| Symbol    | Parameter               | Conditions                                                             | Min | Max | Unit |
|-----------|-------------------------|------------------------------------------------------------------------|-----|-----|------|
| $V_{DS}$  | drain-source voltage    | $25\text{ }^\circ\text{C} \leq T_j \leq 175\text{ }^\circ\text{C}$     | -   | 60  | V    |
| $V_{DGR}$ | drain-gate voltage      | $R_{GS} = 20\text{ k}\Omega$                                           | -   | 60  | V    |
| $V_{GS}$  | gate-source voltage     | DC; $T_j \leq 175\text{ }^\circ\text{C}$                               | -20 | 20  | V    |
| $P_{tot}$ | total power dissipation | $T_{mb} = 25\text{ }^\circ\text{C}$ ; Fig. 1                           | -   | 53  | W    |
| $I_D$     | drain current           | $V_{GS} = 10\text{ V}$ ; $T_{mb} = 25\text{ }^\circ\text{C}$ ; Fig. 2  | [1] | 30  | A    |
|           |                         | $V_{GS} = 10\text{ V}$ ; $T_{mb} = 100\text{ }^\circ\text{C}$ ; Fig. 2 | -   | 29  | A    |

| Symbol                                    | Parameter                                    | Conditions                                                                                 |         | Min | Max | Unit       |
|-------------------------------------------|----------------------------------------------|--------------------------------------------------------------------------------------------|---------|-----|-----|------------|
| $I_{DM}$                                  | peak drain current                           | pulsed; $t_p \leq 10 \mu s$ ; $T_{mb} = 25^\circ C$ ; Fig. 3                               |         | -   | 164 | A          |
| $T_{stg}$                                 | storage temperature                          |                                                                                            |         | -55 | 175 | $^\circ C$ |
| $T_j$                                     | junction temperature                         |                                                                                            |         | -55 | 175 | $^\circ C$ |
| <b>Source-drain diode FET1 and FET2</b>   |                                              |                                                                                            |         |     |     |            |
| $I_S$                                     | source current                               | $T_{mb} = 25^\circ C$                                                                      | [1]     | -   | 30  | A          |
| $I_{SM}$                                  | peak source current                          | pulsed; $t_p \leq 10 \mu s$ ; $T_{mb} = 25^\circ C$                                        |         | -   | 164 | A          |
| <b>Avalanche ruggedness FET1 and FET2</b> |                                              |                                                                                            |         |     |     |            |
| $E_{DS(AL)S}$                             | non-repetitive drain-source avalanche energy | $I_D = 30 A$ ; $V_{sup} \leq 60 V$ ; $V_{GS} = 10 V$ ; $T_{j(init)} = 25^\circ C$ ; Fig. 4 | [2] [3] | -   | 55  | mJ         |

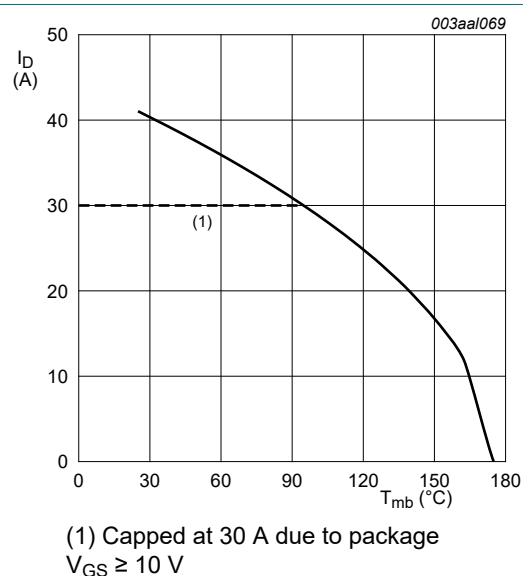
[1] Continuous current is limited by package

[2] Refer to application note AN10273 for further information

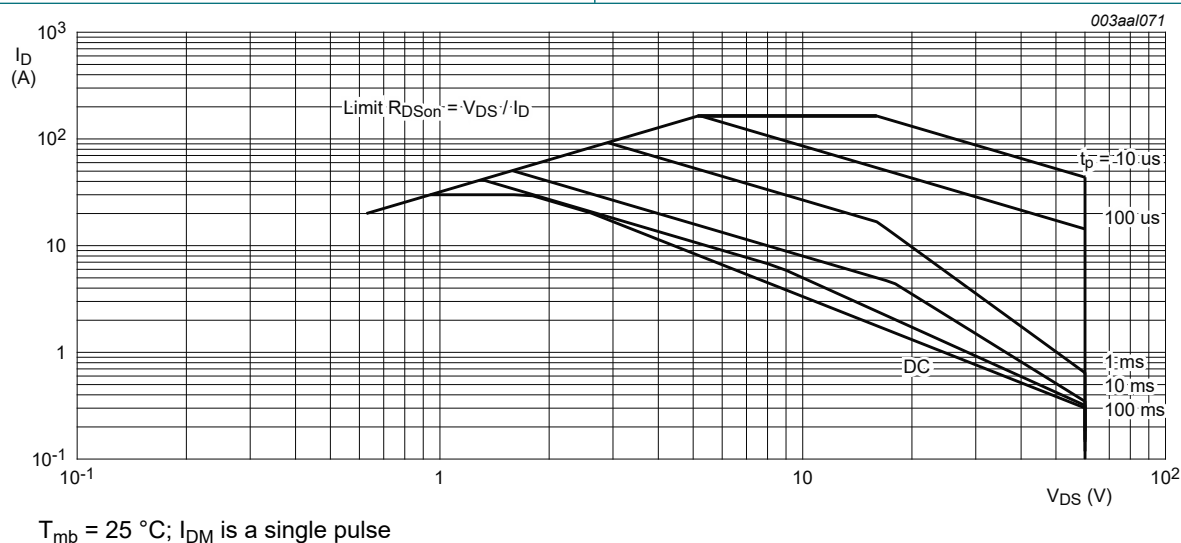
[3] Single-pulse avalanche rating limited by maximum junction temperature of  $175^\circ C$



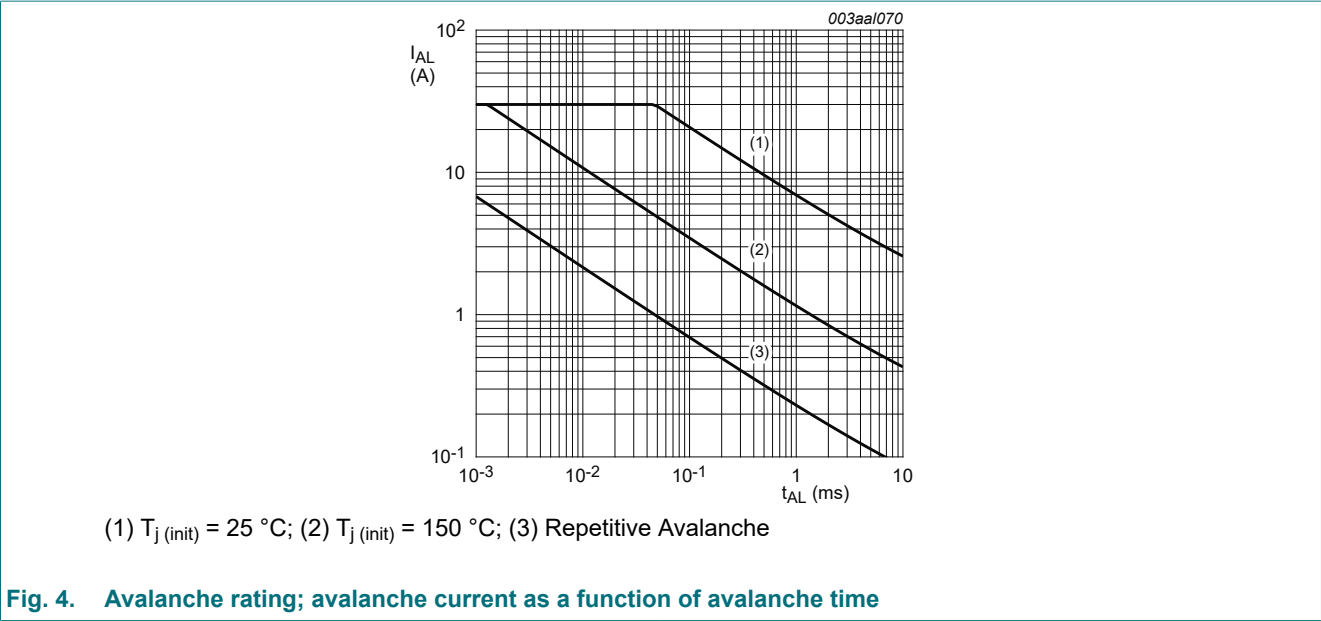
**Fig. 1. Normalized total power dissipation as a function of mounting base temperature**



**Fig. 2. Continuous drain current as a function of mounting base temperature**



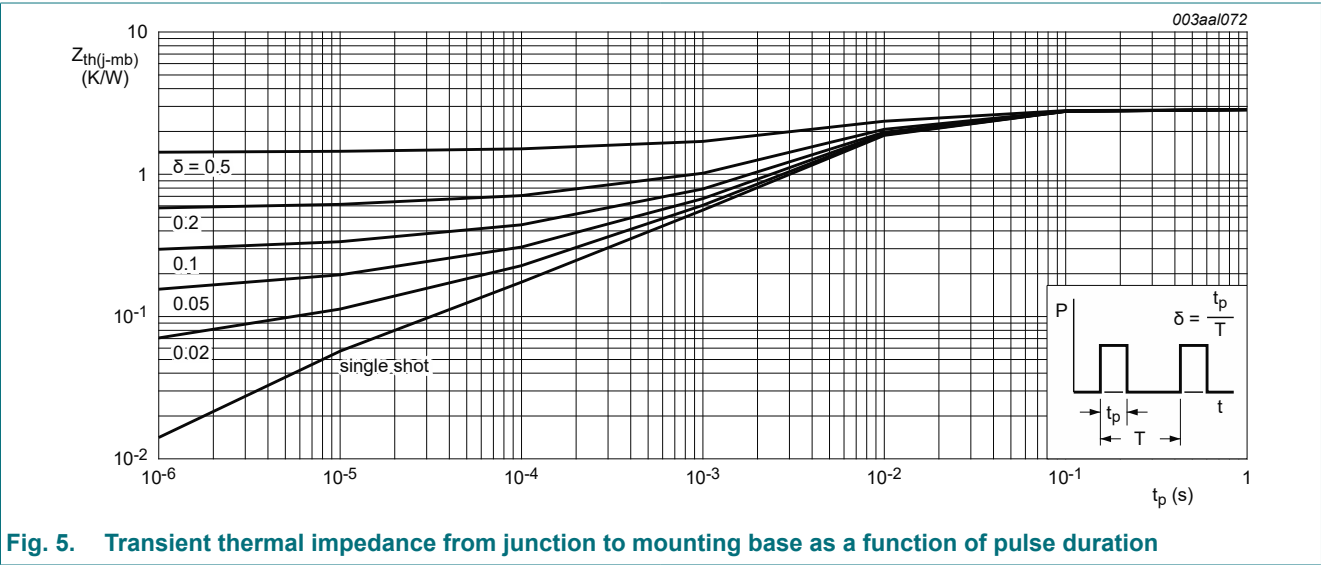
**Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage**



9. Thermal characteristics

Table 6. Thermal characteristics

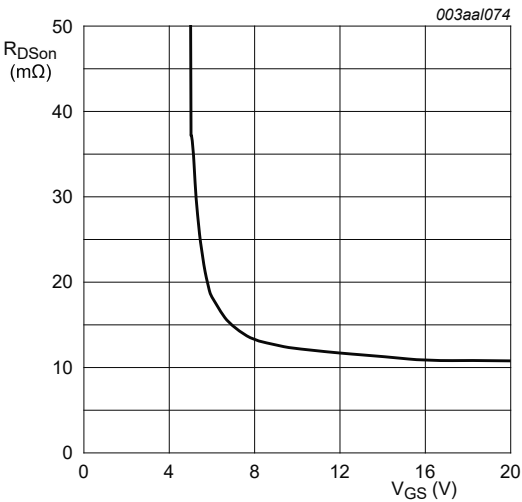
| Symbol         | Parameter                                         | Conditions                                            | Min | Typ | Max  | Unit |
|----------------|---------------------------------------------------|-------------------------------------------------------|-----|-----|------|------|
| $R_{th(j-mb)}$ | thermal resistance from junction to mounting base | <a href="#">Fig. 5</a>                                | -   | -   | 2.84 | K/W  |
| $R_{th(j-a)}$  | thermal resistance from junction to ambient       | Minimum footprint; mounted on a printed circuit board | -   | 95  | -    | K/W  |



## 10. Characteristics

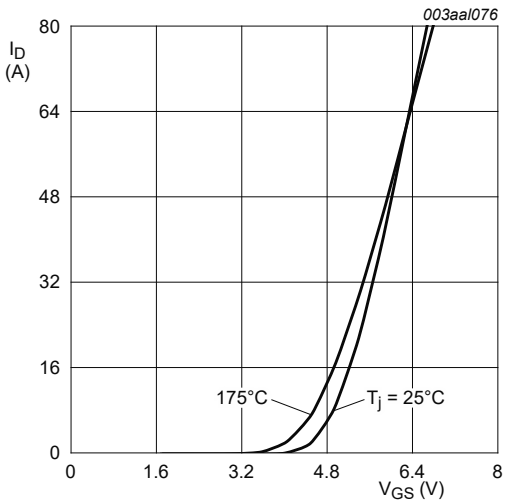
Table 7. Characteristics

| Symbol                                | Parameter                        | Conditions                                                                                                                                       |  | Min | Typ  | Max  | Unit |
|---------------------------------------|----------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------|--|-----|------|------|------|
| Static characteristics FET1 and FET2  |                                  |                                                                                                                                                  |  |     |      |      |      |
| V <sub>(BR)DSS</sub>                  | drain-source breakdown voltage   | I <sub>D</sub> = 250 μA; V <sub>GS</sub> = 0 V; T <sub>j</sub> = -55 °C                                                                          |  | 54  | -    | -    | V    |
|                                       |                                  | I <sub>D</sub> = 250 μA; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C                                                                           |  | 60  | -    | -    | V    |
| V <sub>GS(th)</sub>                   | gate-source threshold voltage    | I <sub>D</sub> = 1 mA; V <sub>DS</sub> =V <sub>GS</sub> ; T <sub>j</sub> = 25 °C; <a href="#">Fig. 9</a> ; <a href="#">Fig. 10</a>               |  | 2.4 | 3    | 4    | V    |
|                                       |                                  | I <sub>D</sub> = 1 mA; V <sub>DS</sub> =V <sub>GS</sub> ; T <sub>j</sub> = 175 °C; <a href="#">Fig. 9</a> ; <a href="#">Fig. 10</a>              |  | 1   | -    | -    | V    |
|                                       |                                  | I <sub>D</sub> = 1 mA; V <sub>DS</sub> =V <sub>GS</sub> ; T <sub>j</sub> = -55 °C; <a href="#">Fig. 9</a> ; <a href="#">Fig. 10</a>              |  | -   | -    | 4.5  | V    |
| I <sub>DSS</sub>                      | drain leakage current            | V <sub>DS</sub> = 60 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C                                                                            |  | -   | 0.02 | 1    | μA   |
|                                       |                                  | V <sub>DS</sub> = 60 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 175 °C                                                                           |  | -   | -    | 500  | μA   |
| I <sub>GSS</sub>                      | gate leakage current             | V <sub>GS</sub> = -20 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C                                                                           |  | -   | 2    | 100  | nA   |
|                                       |                                  | V <sub>GS</sub> = 20 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C                                                                            |  | -   | 2    | 100  | nA   |
| R <sub>DSon</sub>                     | drain-source on-state resistance | V <sub>GS</sub> = 10 V; I <sub>D</sub> = 10 A; T <sub>j</sub> = 25 °C; <a href="#">Fig. 11</a>                                                   |  | -   | 11.3 | 14   | mΩ   |
|                                       |                                  | V <sub>GS</sub> = 10 V; I <sub>D</sub> = 10 A; T <sub>j</sub> = 175 °C; <a href="#">Fig. 11</a> ; <a href="#">Fig. 12</a>                        |  | -   | 25.3 | 31.4 | mΩ   |
| Dynamic characteristics FET1 and FET2 |                                  |                                                                                                                                                  |  |     |      |      |      |
| Q <sub>G(tot)</sub>                   | total gate charge                | I <sub>D</sub> = 10 A; V <sub>DS</sub> = 48 V; V <sub>GS</sub> = 10 V; T <sub>j</sub> = 25 °C; <a href="#">Fig. 13</a> ; <a href="#">Fig. 14</a> |  | -   | 23.6 | -    | nC   |
| Q <sub>GS</sub>                       | gate-source charge               |                                                                                                                                                  |  | -   | 4.9  | -    | nC   |
| Q <sub>GD</sub>                       | gate-drain charge                | I <sub>D</sub> = 10 A; V <sub>DS</sub> = 48 V; V <sub>GS</sub> = 20 V; T <sub>j</sub> = 25 °C; <a href="#">Fig. 13</a> ; <a href="#">Fig. 14</a> |  | -   | 8.1  | -    | nC   |
| C <sub>iss</sub>                      | input capacitance                | V <sub>DS</sub> = 25 V; V <sub>GS</sub> = 0 V; f = 1 MHz; T <sub>j</sub> = 25 °C; <a href="#">Fig. 15</a>                                        |  | -   | 1183 | 1578 | pF   |
| C <sub>oss</sub>                      | output capacitance               |                                                                                                                                                  |  | -   | 167  | 200  | pF   |
| C <sub>rss</sub>                      | reverse transfer capacitance     |                                                                                                                                                  |  | -   | 113  | 158  | pF   |
| t <sub>d(on)</sub>                    | turn-on delay time               | V <sub>DS</sub> = 48 V; R <sub>L</sub> = 5 Ω; V <sub>GS</sub> = 10 V; R <sub>G(ext)</sub> = 5 Ω; T <sub>j</sub> = 25 °C                          |  | -   | 7.6  | -    | ns   |
| t <sub>r</sub>                        | rise time                        |                                                                                                                                                  |  | -   | 11.1 | -    | ns   |
| t <sub>d(off)</sub>                   | turn-off delay time              |                                                                                                                                                  |  | -   | 15.5 | -    | ns   |
| t <sub>f</sub>                        | fall time                        |                                                                                                                                                  |  | -   | 11   | -    | ns   |
| Source-drain diode FET1 and FET2      |                                  |                                                                                                                                                  |  |     |      |      |      |
| V <sub>SD</sub>                       | source-drain voltage             | I <sub>S</sub> = 10 A; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C; <a href="#">Fig. 16</a>                                                    |  | -   | 0.78 | 1.2  | V    |
| t <sub>rr</sub>                       | reverse recovery time            | I <sub>S</sub> = 10 A; dI <sub>S</sub> /dt = -100 A/μs; V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 30 V; T <sub>j</sub> = 25 °C                    |  | -   | 24.5 | -    | ns   |
| Q <sub>r</sub>                        | recovered charge                 |                                                                                                                                                  |  | -   | 24.6 | -    | nC   |



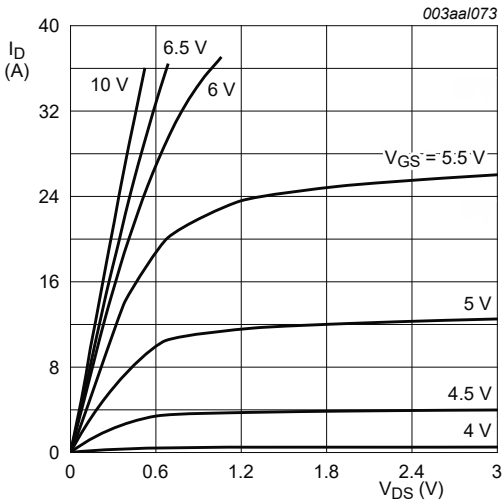
$T_J = 25\text{ }^{\circ}\text{C}$ ;  $I_D = 10\text{ A}$

Fig. 6. Drain-source on-state resistance as a function of gate-source voltage; typical values



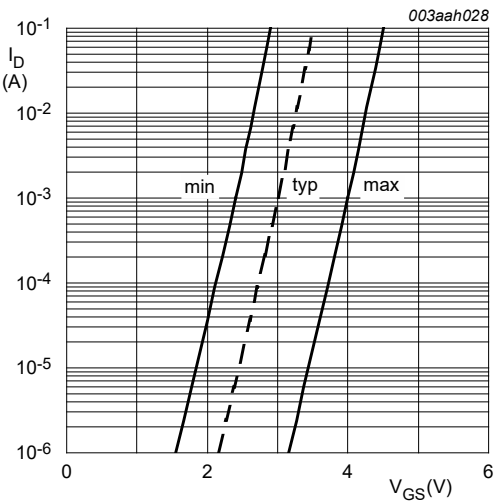
$V_{DS} = 10\text{ V}$

Fig. 7. Transfer characteristics; drain current as a function of gate-source voltage; typical values



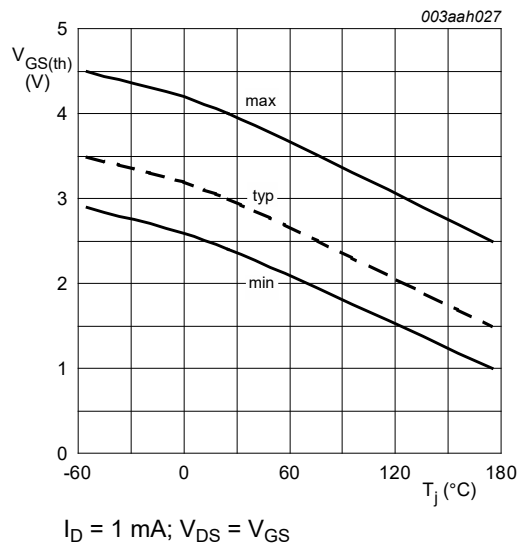
$T_J = 25\text{ }^{\circ}\text{C}$ ;  $t_p = 300\text{ }\mu\text{s}$

Fig. 8. Output characteristics; drain current as a function of drain-source voltage; typical values

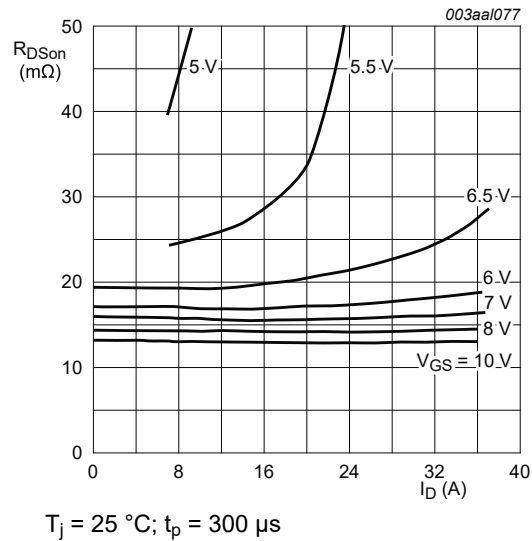


$T_J = 25\text{ }^{\circ}\text{C}$ ;  $V_{DS} = 5\text{ V}$

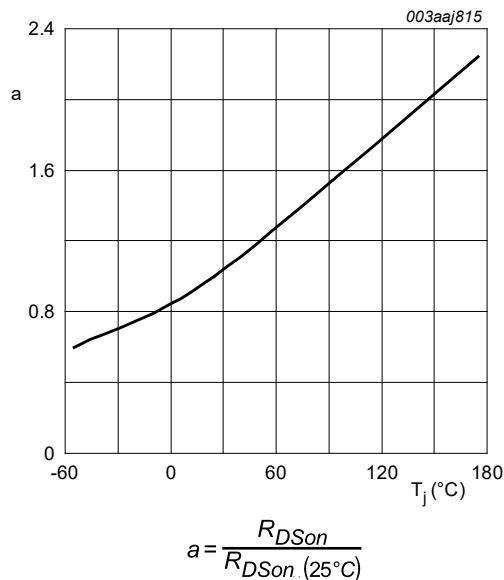
Fig. 9. Sub-threshold drain current as a function of gate-source voltage



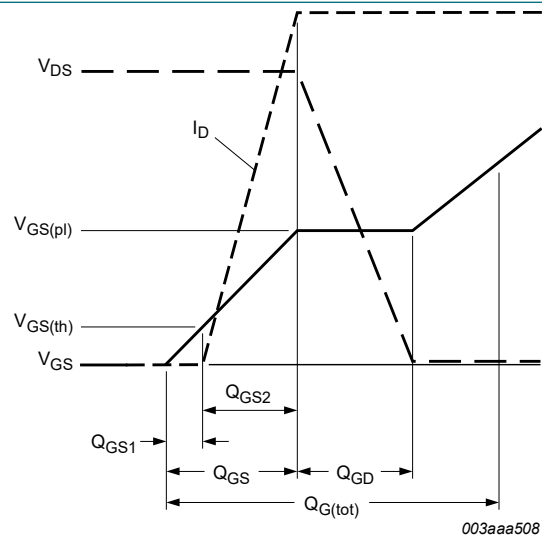
**Fig. 10.** Gate-source threshold voltage as a function of junction temperature



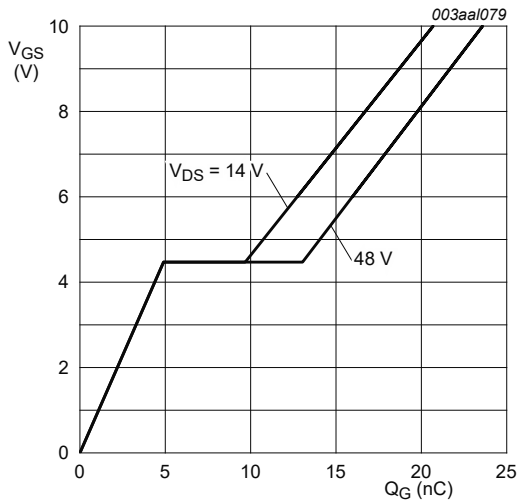
**Fig. 11.** Drain-source on-state resistance as a function of drain current; typical values



**Fig. 12.** Normalized drain-source on-state resistance factor as a function of junction temperature

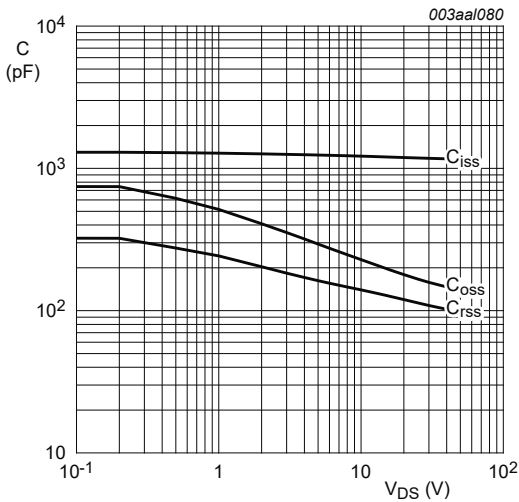


**Fig. 13.** Gate charge waveform definitions



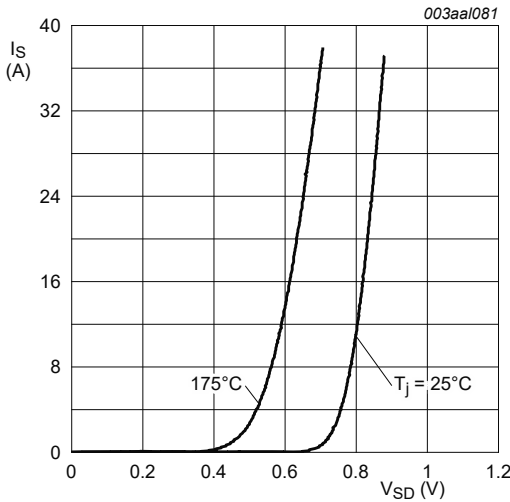
$T_j = 25\text{ }^{\circ}\text{C}$ ;  $I_D = 10\text{ A}$

Fig. 14. Gate-source voltage as a function of gate charge; typical values



$V_{GS} = 0\text{ V}$ ;  $f = 1\text{ MHz}$

Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$V_{GS} = 0\text{ V}$

Fig. 16. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values



11. Package outline

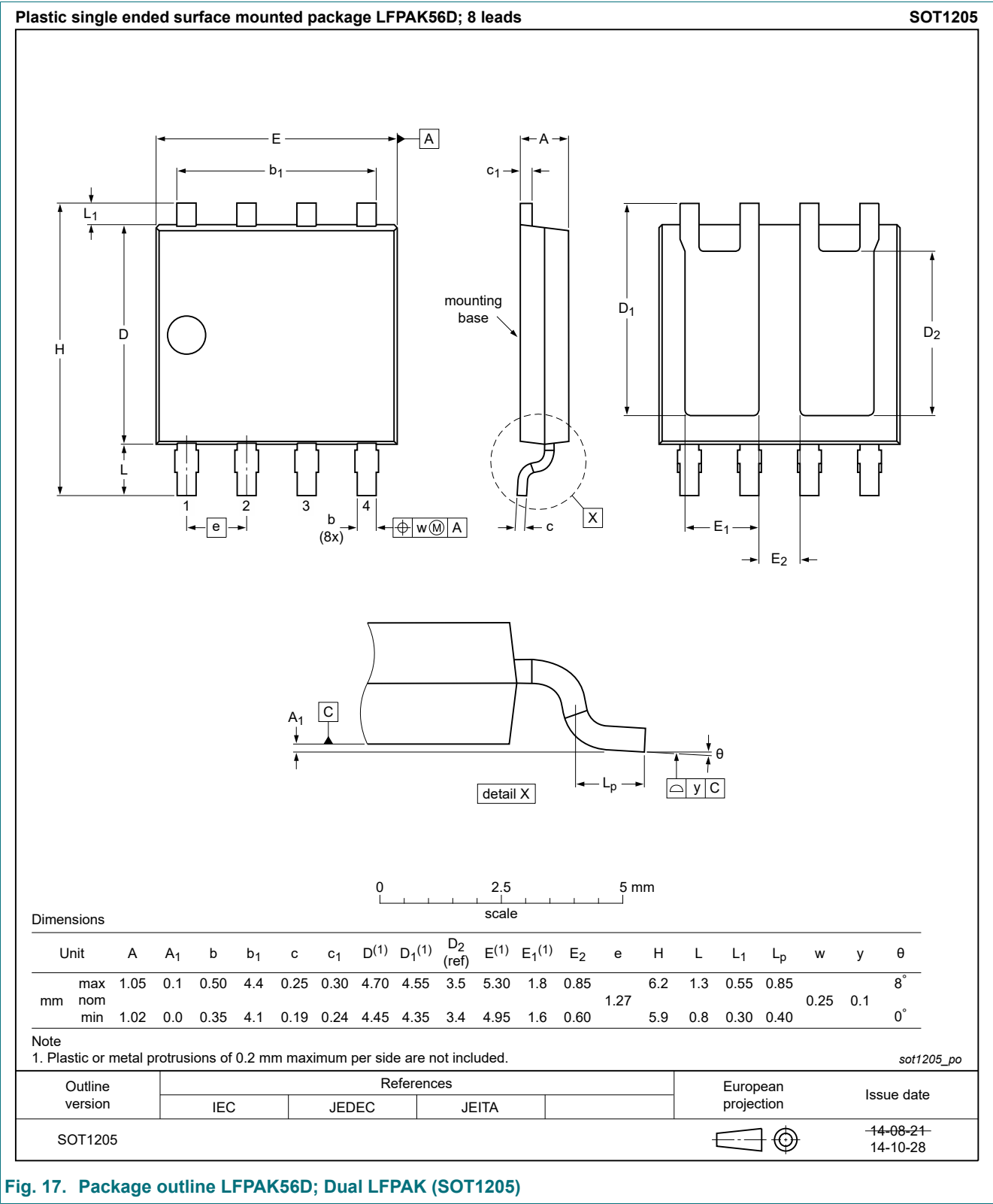


Fig. 17. Package outline LPAK56D; Dual LPAK (SOT1205)

12. Soldering

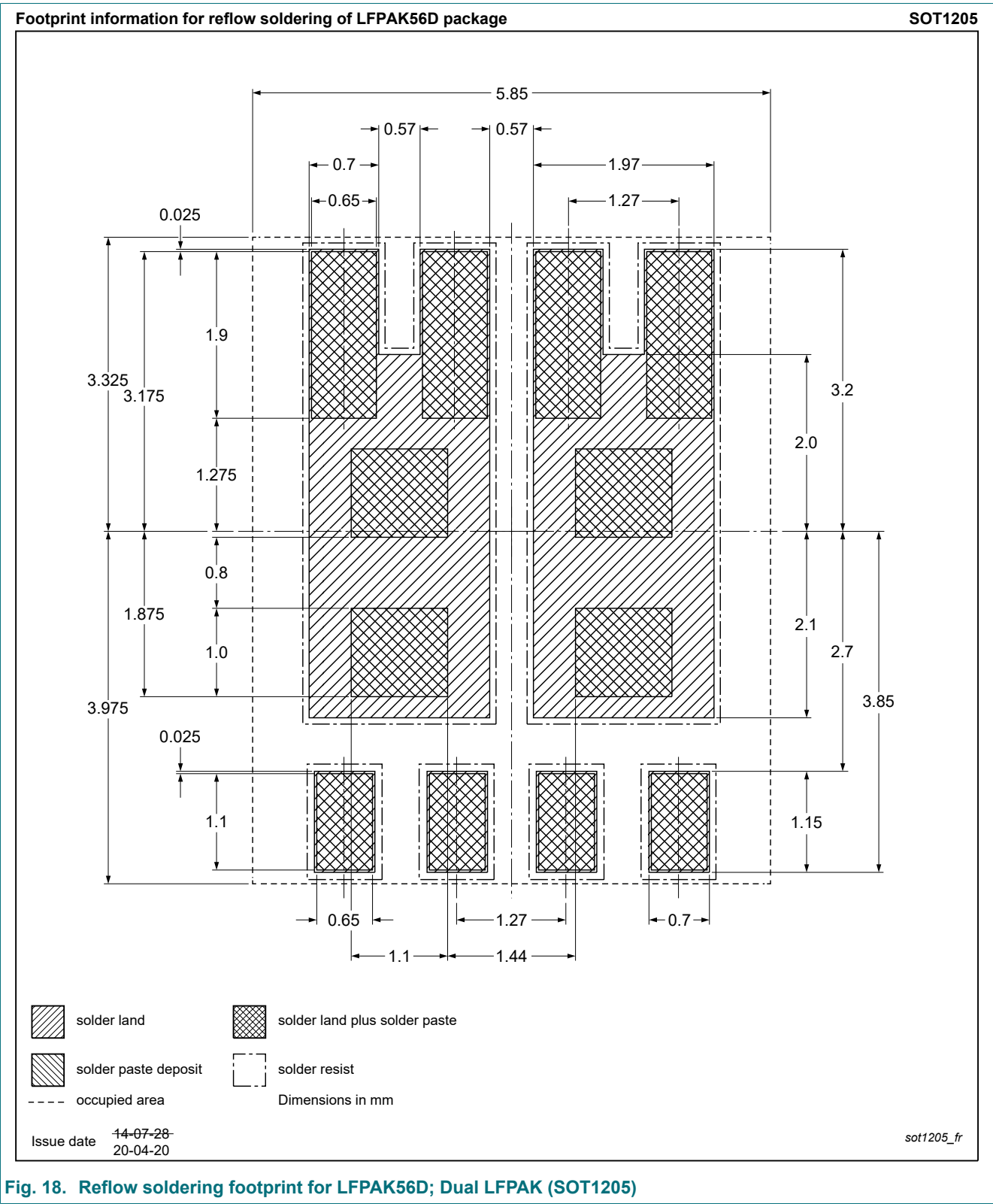


Fig. 18. Reflow soldering footprint for LPAK56D; Dual LPAK (SOT1205)

## 13. Legal information

### Data sheet status

| Document status<br>[1][2]      | Product status [3] | Definition                                                                            |
|--------------------------------|--------------------|---------------------------------------------------------------------------------------|
| Objective [short] data sheet   | Development        | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification      | This document contains data from the preliminary specification.                       |
| Product [short] data sheet     | Production         | This document contains the product specification.                                     |

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For sales office addresses, please send an email to: [salesaddresses@nexperia.com](mailto:salesaddresses@nexperia.com)

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