

Product Summary

$V_{(BR)DSS}$	$R_{DS(ON)}$ Max	I_D $T_A = +25^\circ\text{C}$
60V	40m Ω @ $V_{GS} = 10\text{V}$	5.0A
	55m Ω @ $V_{GS} = 4.5\text{V}$	4.4A

Description and Applications

This new generation MOSFET is designed to minimize the on-state resistance ($R_{DS(ON)}$), yet maintain superior switching performance, making it ideal for high efficiency power management applications.

- DC-DC Converters
- Power Management Functions
- Backlighting

Features and Benefits

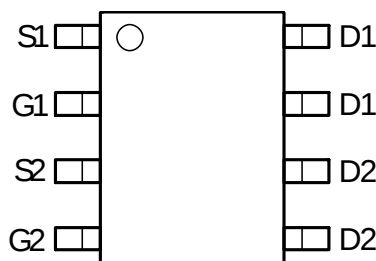
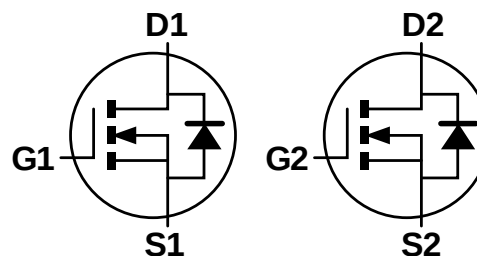
- Low Input Capacitance
- Low On-Resistance
- Fast Switching Speed
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **Qualified to AEC-Q101 Standards for High Reliability**
- **PPAP Capable (Note 4)**

Mechanical Data

- Case: SO-8
- Case Material: Molded Plastic, "Green" Molding Compound.
UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: See Diagram
- Terminals: Finish – Tin Finish Annealed over Copper Leadframe.
Solderable per MIL-STD-202, Method 208 
- Weight: 0.074 grams (Approximate)



Top View


 Top View
 Pin Configuration


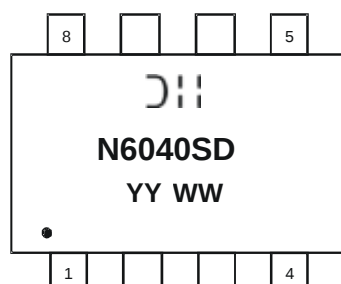
Equivalent Circuit

Ordering Information (Note 5)

Part Number	Case	Packaging
DMN6040SSDQ-13	SO-8	2,500/Tape & Reel

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
 2. See <http://www.diodes.com> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
 4. Automotive products are AEC-Q101 qualified and are PPAP capable. Refer to http://www.diodes.com/product_compliance_definitions.html
 5. For packaging details, go to our website at <http://www.diodes.com/products/packages.html>.

Marking Information



DII = Manufacturer's Marking
N6040SD = Product Type Marking Code
YYWW = Date Code Marking
 YY = Year (ex: 16 = 2016)
 WW = Week (01 – 53)

Maximum Ratings (@T_A = +25°C unless otherwise specified)

Characteristic			Symbol	Value	Units
Drain-Source Voltage			V _{DSS}	60	V
Gate-Source Voltage			V _{GSS}	±20	V
Continuous Drain Current (Note 7) V _{GS} = 10V	Steady State	T _A = +25°C T _A = +70°C	I _D	5.0 4.1	A
	t < 10s	T _A = +25°C T _A = +70°C	I _D	6.6 5.3	A
Maximum Body Diode Forward Current (Note 7)			I _S	2.5	A
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%)			I _{DM}	30	A
Pulsed Body Diode Forward Current (10µs pulse, duty cycle = 1%)			I _{SM}	30	A
Avalanche Current (Note 8) L = 0.1mH			I _{AS}	14.2	A
Avalanche Energy (Note 8) L = 0.1mH			E _{AS}	10	mJ

Thermal Characteristics (@T_A = +25°C unless otherwise specified)

Characteristic		Symbol	Value	Units
Total Power Dissipation (Note 6)	T _A = +25°C	P _D	1.3	W
	T _A = +70°C		0.8	
Thermal Resistance, Junction to Ambient (Note 6)	Steady State	R _{θJA}	102	°C/W
	t < 10s		61	
Total Power Dissipation (Note 7)	T _A = +25°C	P _D	1.7	W
	T _A = +70°C		1.1	
Thermal Resistance, Junction to Ambient (Note 7)	Steady State	R _{θJA}	75	°C/W
	t < 10s		50	
Thermal Resistance, Junction to Case (Note 7)		R _{θJC}	14.5	
Operating and Storage Temperature Range		T _J , T _{STG}	-55 to +150	°C

Electrical Characteristics (@T_A = 25°C unless otherwise specified)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 9)						
Drain-Source Breakdown Voltage	BV _{DSS}	60	—	—	V	V _{GS} = 0V, I _D = 250µA
Zero Gate Voltage Drain Current	I _{DSS}	—	—	100	nA	V _{DS} = 60V, V _{GS} = 0V
Gate-Source Leakage	I _{GSS}	—	—	±100	nA	V _{GS} = ±20V, V _{DS} = 0V
ON CHARACTERISTICS (Note 9)						
Gate Threshold Voltage	V _{GS(TH)}	1	—	3	V	V _{DS} = V _{GS} , I _D = 250µA
Static Drain-Source On-Resistance	R _{DS(ON)}	—	30	40	mΩ	V _{GS} = 10V, I _D = 4.5A
		—	35	55		V _{GS} = 4.5V, I _D = 3.5A
Forward Transfer Admittance	Y _{FS}	—	4.5	—	S	V _{DS} = 10V, I _D = 4.3A
Diode Forward Voltage	V _{SD}	—	0.7	1.2	V	V _{GS} = 0V, I _S = 1A
DYNAMIC CHARACTERISTICS (Note 10)						
Input Capacitance	C _{ISS}	—	1,287	—	pF	V _{DS} = 25V, V _{GS} = 0V f = 1.0MHz
Output Capacitance	C _{OSS}	—	57	—		
Reverse Transfer Capacitance	C _{RSS}	—	44	—		
Gate Resistance	R _G	—	1.2	—	Ω	V _{DS} = 0V, V _{GS} = 0V, f = 1.0MHz
Total Gate Charge (V _{GS} = 10V)	Q _G	—	22.4	—	nC	V _{DS} = 30V, I _D = 4.3A
Total Gate Charge (V _{GS} = 4.5V)	Q _G	—	10.4	—		
Gate-Source Charge	Q _{GS}	—	4.9	—		
Gate-Drain Charge	Q _{GD}	—	3.0	—		
Turn-On Delay Time	t _{D(ON)}	—	6.6	—	ns	V _{GS} = 10V, V _{DD} = 30V, R _G = 6Ω, I _D = 4.3A
Turn-On Rise Time	t _R	—	8.1	—		
Turn-Off Delay Time	t _{D(OFF)}	—	20.1	—		
Turn-Off Fall Time	t _F	—	4.0	—		
Body Diode Reverse Recovery Time	t _{RR}	—	18	—	ns	I _S = 4.3A, di/dt = 100A/µs
Body Diode Reverse Recovery Charge	Q _{RR}	—	11.9	—	nC	I _S = 4.3A, di/dt = 100A/µs

- Notes:
- Device mounted on FR-4 PC board, with minimum recommended pad layout, single sided.
 - Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1-inch square copper plate.
 - I_{AS} and E_{AS} rating are based on low frequency and duty cycles to keep T_J = +25°C.
 - Short duration pulse test used to minimize self-heating effect.
 - Guaranteed by design. Not subject to product testing.

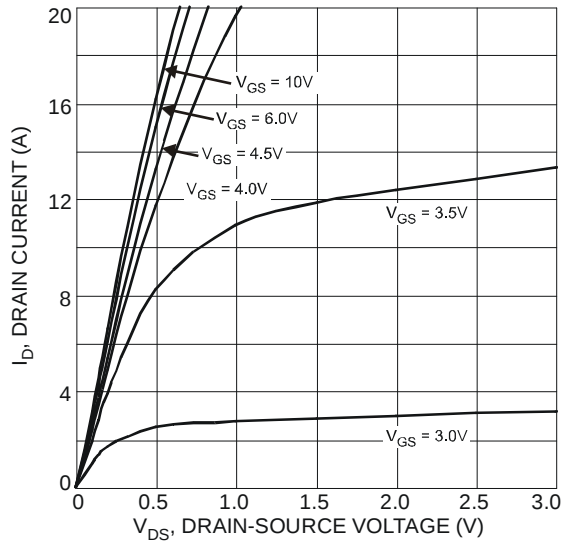


Fig. 1 Typical Output Characteristic

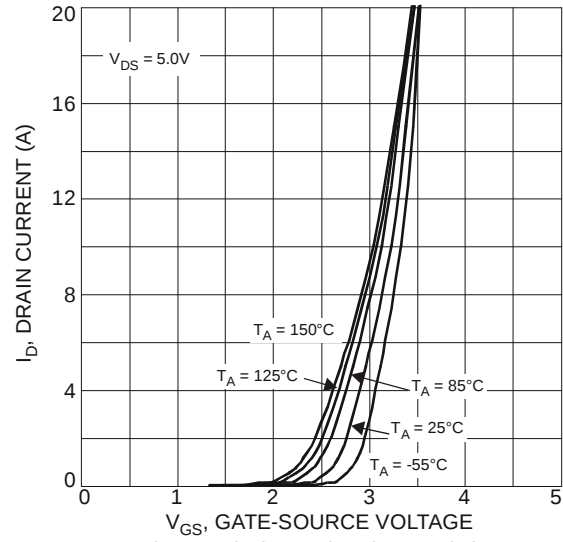


Fig. 2 Typical Transfer Characteristics

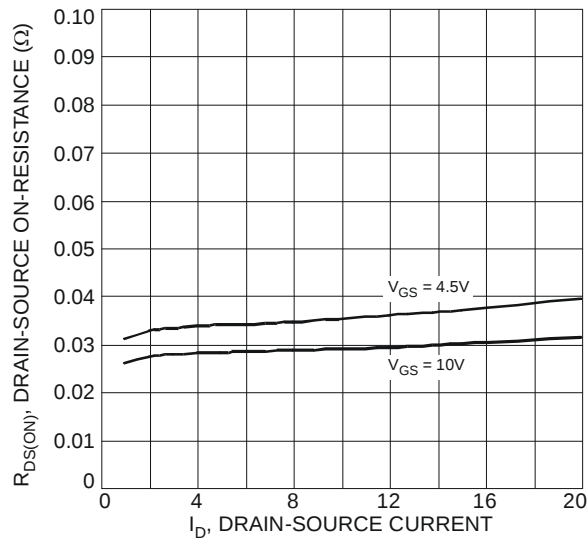


Fig. 3 Typical On-Resistance vs. Drain Current and Gate Voltage

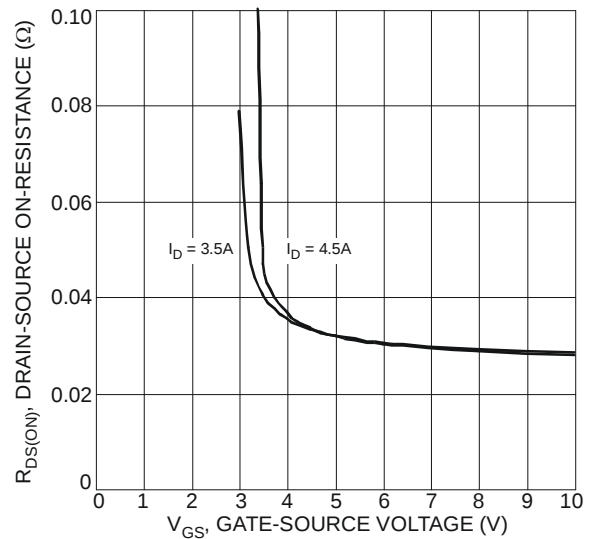


Fig. 4 Typical On-Resistance vs. Drain Current and Gate Voltage

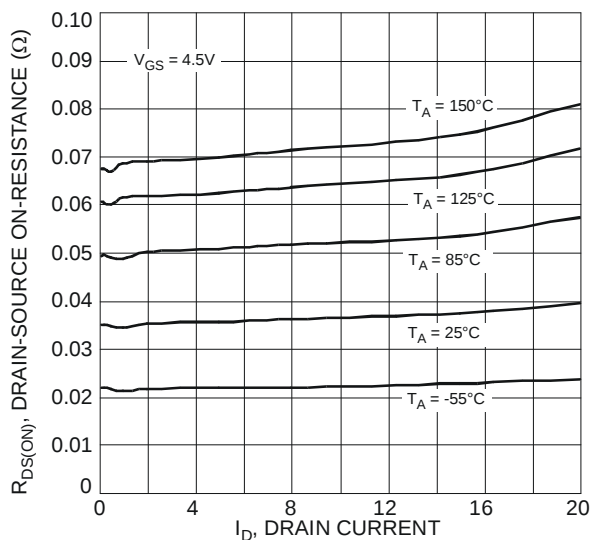


Fig. 5 Typical On-Resistance vs. Drain Current and Temperature

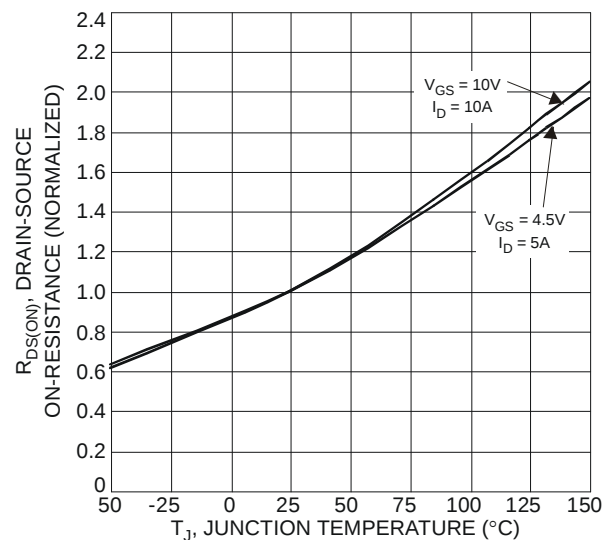


Fig. 6 On-Resistance Variation with Temperature

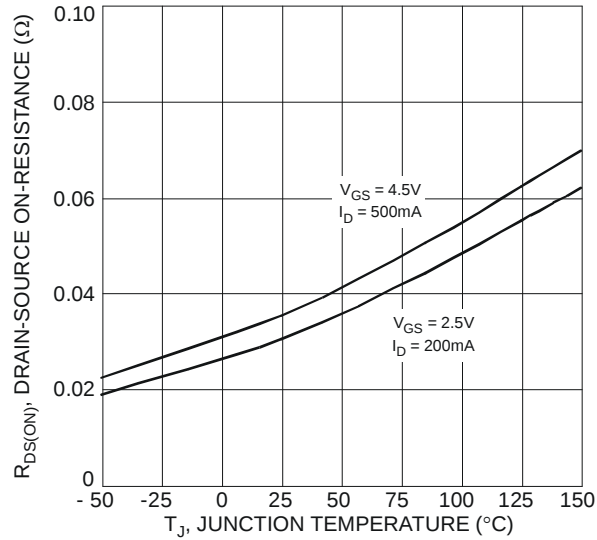


Fig. 7 On-Resistance Variation with Temperature

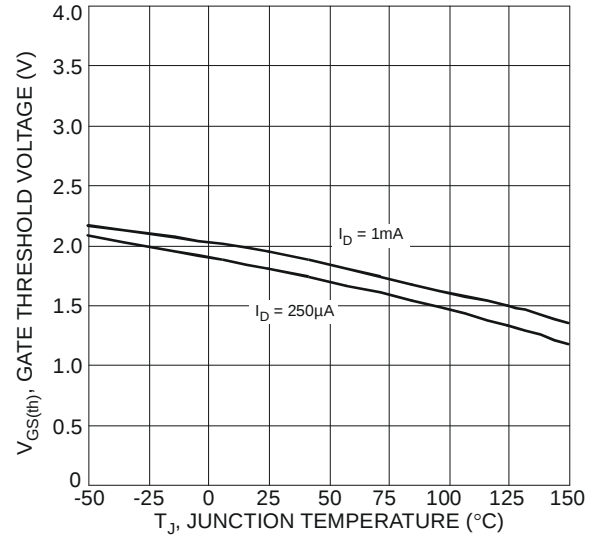


Fig. 8 Gate Threshold Variation vs. Ambient Temperature

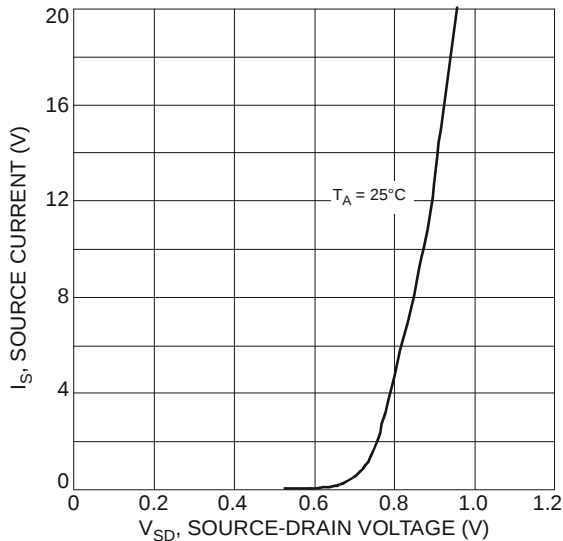


Fig. 9 Diode Forward Voltage vs. Current

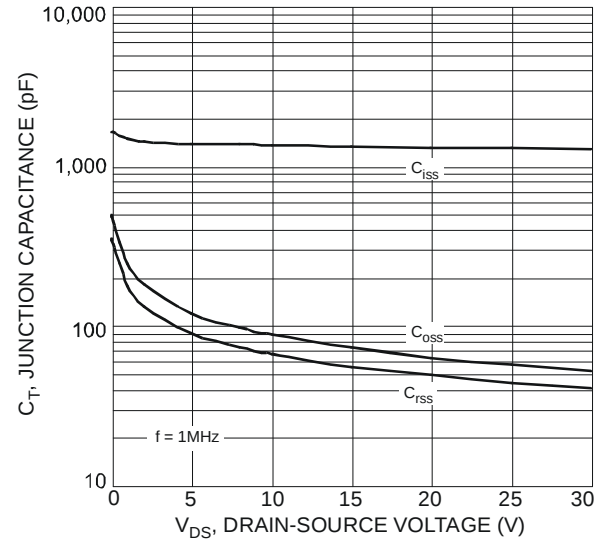


Fig. 10 Typical Junction Capacitance

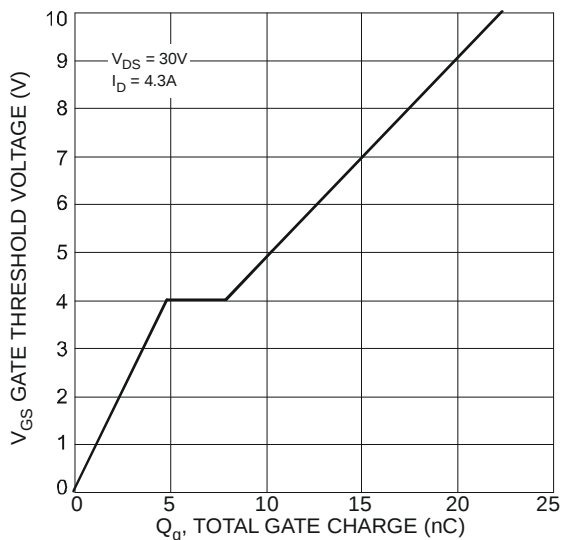


Fig. 11 Gate Charge

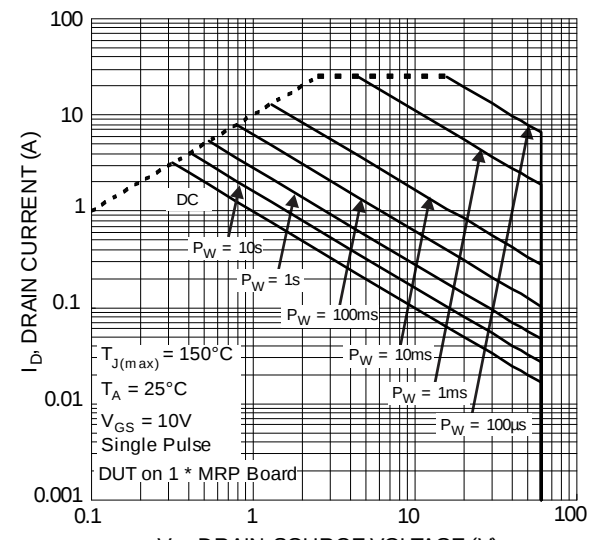
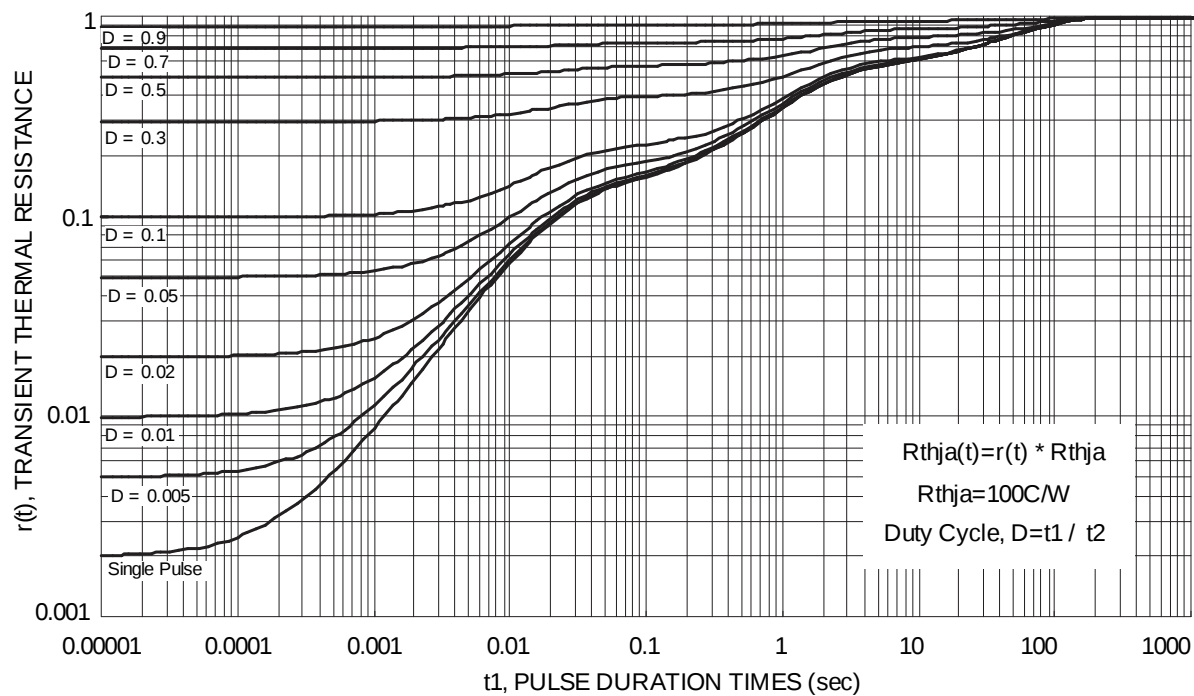
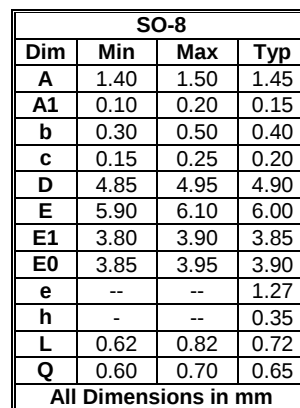


Figure 12 SOA, Safe Operation Area



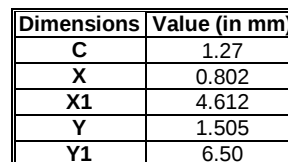
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