

**40V COMPLEMENTARY PAIR ENHANCEMENT MODE MOSFET**
**Product Summary**

Device	V <sub>(BR)DSS</sub>	R <sub>DS(on)</sub> max	I <sub>D</sub> max T <sub>A</sub> = +25°C (Note 7 & 9)
Q1	40V	25mΩ @ V <sub>GS</sub> = 10V	7.5A
		40mΩ @ V <sub>GS</sub> = 4.5V	6.2A
Q2	-40V	25mΩ @ V <sub>GS</sub> = -10V	-7.3A
		45mΩ @ V <sub>GS</sub> = -4.5V	-5.7A

**Description and Applications**

This MOSFET has been designed to ensure that R<sub>DS(on)</sub> of N and P channel FET are matched to minimize losses in both arms of the bridge. The DMC4040SSDQ is optimized for use in 3 phases brushless DC motor circuits (BLDC), CCFL backlighting.

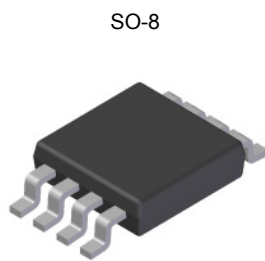
- 3 phases BLDC motor
- CCFL backlighting

**Features and Benefits**

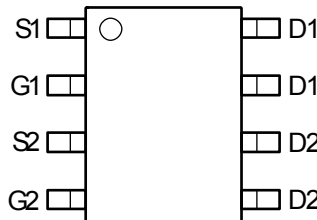
- Reduced Footprint with Two Discrete Devices in Single SO-8
- Low On-Resistance
- Fast Switching Speed
- Low Input/Output Leakage
- **Lead-Free Finish; RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **Qualified to AEC-Q101 Standards for High Reliability**
- **PPAP Available (Note 4)**

**Mechanical Data**

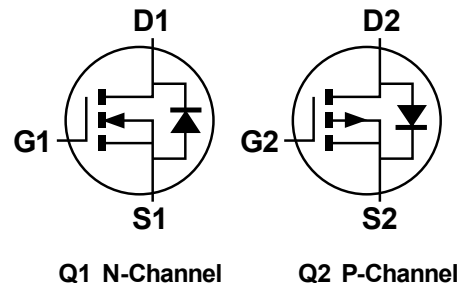
- Case: SO-8
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals Connections: See diagram below
- Terminals: Finish - Matte Tin annealed over Copper lead frame. Solderable per MIL-STD-202, Method 208
- Weight: 0.074 grams (approximate)

**NEW PRODUCT**


Top View



Top View

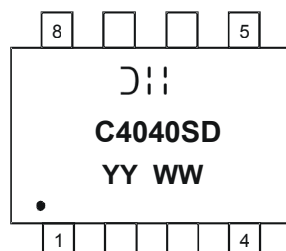


Equivalent Circuit

**Ordering Information** (Note 4 & 5)

Part Number	Compliance	Case	Packaging
DMC4040SSDQ-13	Automotive	SO-8	2,500/Tape & Reel

- Notes:
1. EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant. All applicable RoHS exemptions applied.
  2. See [http://www.diodes.com/quality/lead\\_free.html](http://www.diodes.com/quality/lead_free.html) for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
  3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
  4. Automotive products are AEC-Q101 qualified and are PPAP capable. Automotive, AEC-Q101 and standard products are electrically and thermally the same, except where specified. For more information, please refer to [http://www.diodes.com/quality/product\\_grade\\_definitions/](http://www.diodes.com/quality/product_grade_definitions/).
  5. For packaging details, go to our website at <http://www.diodes.com/products/packages.html>.

**Marking Information**


DII = Manufacturer's Marking  
 C4040SD = Product Type Marking Code  
 YYWW = Date Code Marking  
 YY = Year (ex: 13 = 2013)  
 WW = Week (01 - 53)

**Maximum Ratings** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic		Symbol	N-Channel - Q1	P-Channel - Q2	Units
Drain-Source Voltage		V <sub>DSS</sub>	40	-40	V
Gate-Source Voltage		V <sub>GSS</sub>	±20	±20	V
Continuous Drain Current	V <sub>GS</sub> = 10V	(Notes 7 & 9)	7.5	-7.5	A
		T <sub>A</sub> = +70°C (Notes 7 & 9)	5.8	-5.8	
		(Notes 6 & 9)	5.7	-5.7	
		(Notes 6 & 10)	6.8	-6.8	
Pulsed Drain Current	V <sub>GS</sub> = 10V	I <sub>DM</sub>	29.0	-29.0	A
Continuous Source Current (Body diode)		I <sub>S</sub>	3.0	-3.0	A
Pulsed Source Current (Body diode)		I <sub>SM</sub>	29.0	-29.0	A

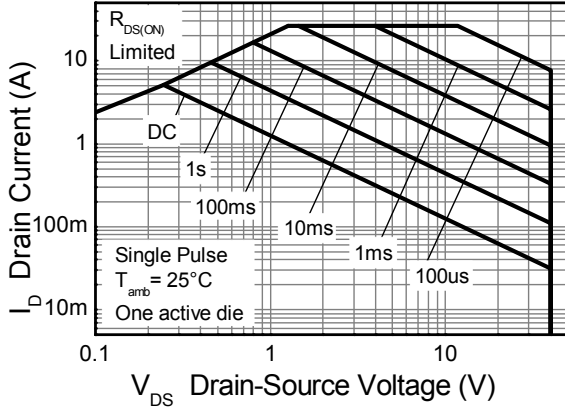
**Thermal Characteristics** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic		Symbol	N-Channel - Q1	P-Channel - Q2	Unit
Power Dissipation Linear Derating Factor	(Notes 6 & 9)	P <sub>D</sub>	1.25	W	mW/°C
			10		
	(Notes 6 & 10)		1.8		
			14.3		
Thermal Resistance, Junction to Ambient	(Notes 7 & 9)	R <sub>θJA</sub>	2.14	°C/W	
	(Notes 6 & 9)		17.2		
	(Notes 6 & 10)		100		
Thermal Resistance, Junction to Lead	(Notes 6 & 10)	R <sub>θJL</sub>	70	°C/W	
	(Notes 7 & 9)		58		
Operating and Storage Temperature Range		T <sub>J</sub> , T <sub>STG</sub>	-55 to +150		°C

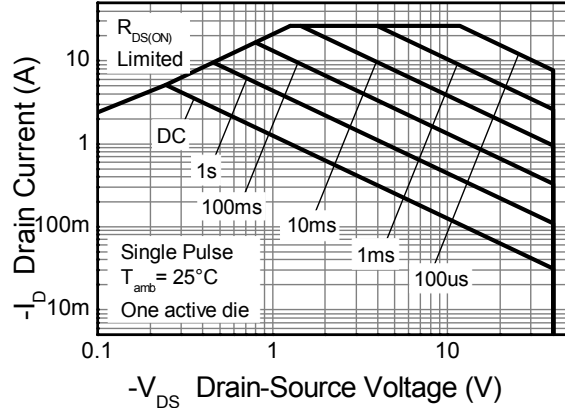
- Notes:
6. For a device surface mounted on 25mm x 25mm x 1.6mm FR4 PCB with high coverage of single sided 1oz copper, in still air conditions; the device is measured when operating in a steady-state condition.
  7. Same as note (6), except the device is measured at t ≤ 10 sec.
  8. Same as note (6), except the device is pulsed with D= 0.02 and pulse width 300 μs. The pulse current is limited by the maximum junction temperature.
  9. For a dual device with one active die.
  10. For a device with two active die running at equal power.
  11. Thermal resistance from junction to solder-point (at the end of the drain lead).

**Thermal Characteristics**

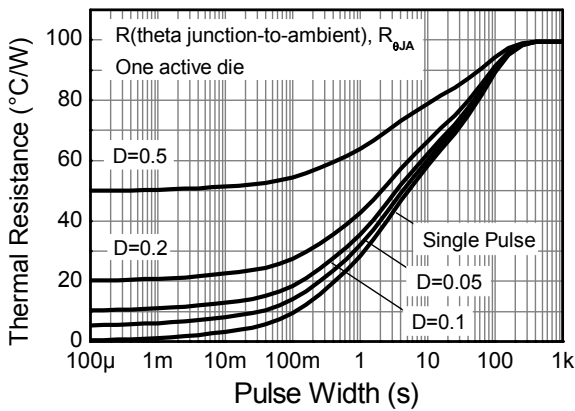
NEW PRODUCT



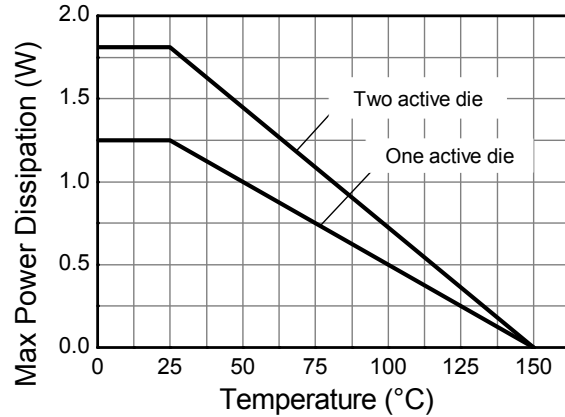
**N-channel Safe Operating Area**



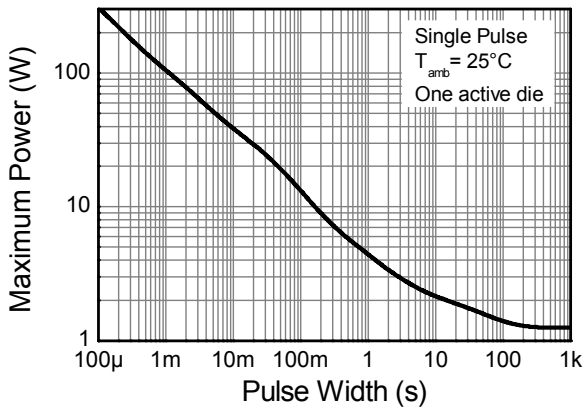
**P-channel Safe Operating Area**



**Transient Thermal Impedance**



**Derating Curve**



**Pulse Power Dissipation**

**Electrical Characteristics – Q1 N-Channel** (@ $T_A = +25^\circ\text{C}$ , unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
<b>OFF CHARACTERISTICS</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	40	—	—	V	$I_D = 250\mu\text{A}$ , $V_{GS} = 0\text{V}$
Zero Gate Voltage Drain Current	$I_{DSS}$	—	—	1.0	$\mu\text{A}$	$V_{DS} = 40\text{V}$ , $V_{GS} = 0\text{V}$
Gate-Source Leakage	$I_{GSS}$	—	—	$\pm 100$	nA	$V_{GS} = \pm 20\text{V}$ , $V_{DS} = 0\text{V}$
<b>ON CHARACTERISTICS</b>						
Gate Threshold Voltage	$V_{GS(th)}$	0.8	1.3	1.8	V	$I_D = 250\mu\text{A}$ , $V_{DS} = V_{GS}$
Static Drain-Source On-Resistance (Note 12)	$R_{DS(on)}$	—	0.013	0.025	$\Omega$	$V_{GS} = 10\text{V}$ , $I_D = 3\text{A}$
			0.028	0.040		$V_{GS} = 4.5\text{V}$ , $I_D = 3\text{A}$
Forward Transconductance (Notes 12 & 13)	$g_{fs}$	—	12.6	—	S	$V_{DS} = 5\text{V}$ , $I_D = 3\text{A}$
Diode Forward Voltage (Note 8)	$V_{SD}$	—	0.7	1.0	V	$I_S = 1\text{A}$ , $V_{GS} = 0\text{V}$
<b>DYNAMIC CHARACTERISTICS (Note 13)</b>						
Input Capacitance	$C_{iss}$	—	1790	—	pF	$V_{DS} = 20\text{V}$ , $V_{GS} = 0\text{V}$ $F = 1\text{MHz}$
Output Capacitance	$C_{oss}$	—	160	—	pF	
Reverse Transfer Capacitance	$C_{rss}$	—	120	—	pF	
Gate Resistance	$R_g$	—	1.03	—	$\Omega$	$V_{DS} = 0\text{V}$ , $V_{GS} = 0\text{V}$ , $f = 1\text{MHz}$
Total Gate Charge (Note 14)	$Q_g$	—	16.0	—	nC	$V_{GS} = 4.5\text{V}$
Total Gate Charge (Note 14)	$Q_g$	—	37.6	—	nC	$V_{GS} = 10\text{V}$ $V_{DS} = 20\text{V}$ $I_D = 3\text{A}$
Gate-Source Charge (Note 14)	$Q_{gs}$	—	7.8	—	nC	
Gate-Drain Charge (Note 14)	$Q_{gd}$	—	6.6	—	nC	$V_{DD} = 20\text{V}$ , $V_{GS} = 10\text{V}$ $I_D = 3\text{A}$
Turn-On Delay Time (Note 14)	$t_{D(on)}$	—	8.1	—	ns	
Turn-On Rise Time (Note 14)	$t_r$	—	15.1	—	ns	
Turn-Off Delay Time (Note 14)	$t_{D(off)}$	—	24.3	—	ns	
Turn-Off Fall Time (Note 14)	$t_f$	—	5.3	—	ns	

Notes: 12. Measured under pulsed conditions. Pulse width  $\leq 300\mu\text{s}$ ; duty cycle  $\leq 2\%$   
 13. For design aid only, not subject to production testing.  
 14. Switching characteristics are independent of operating junction temperatures.

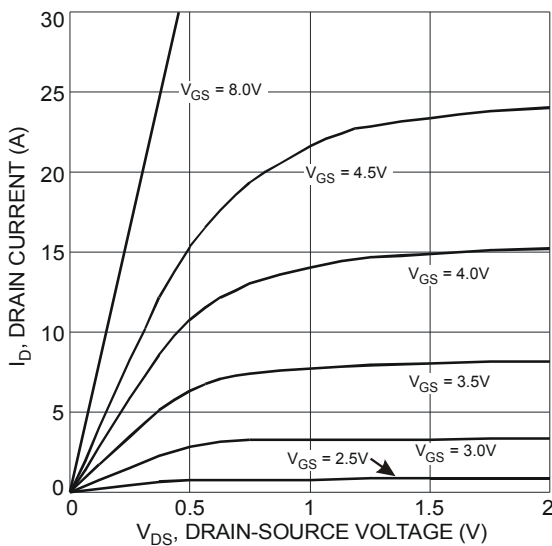
**Typical Characteristics – Q1 N-Channel**


Fig. 1 Typical Output Characteristic

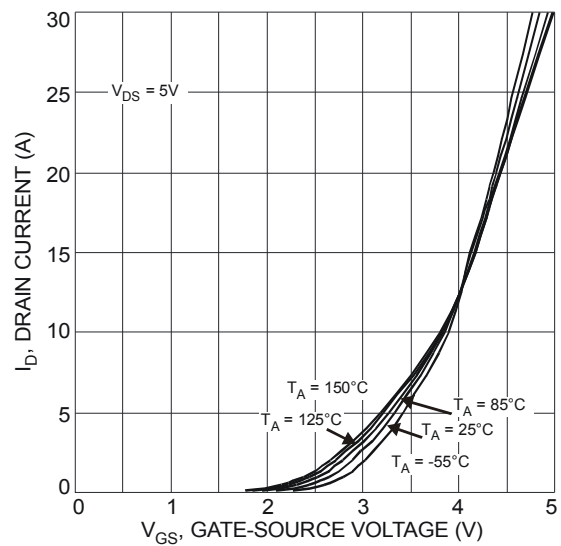


Fig. 2 Typical Transfer Characteristic

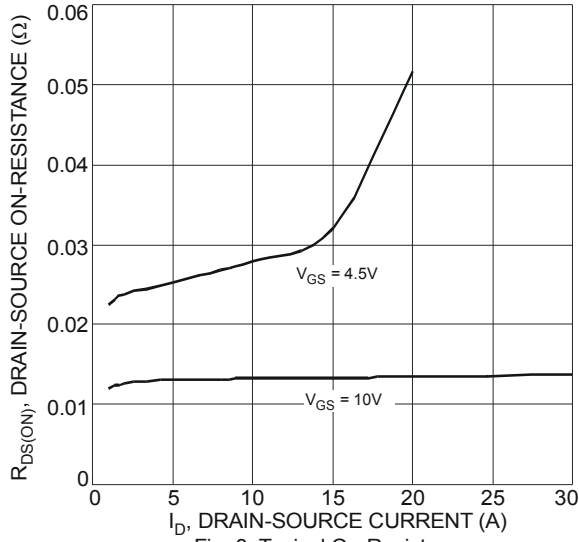


Fig. 3 Typical On-Resistance vs. Drain Current and Gate Voltage

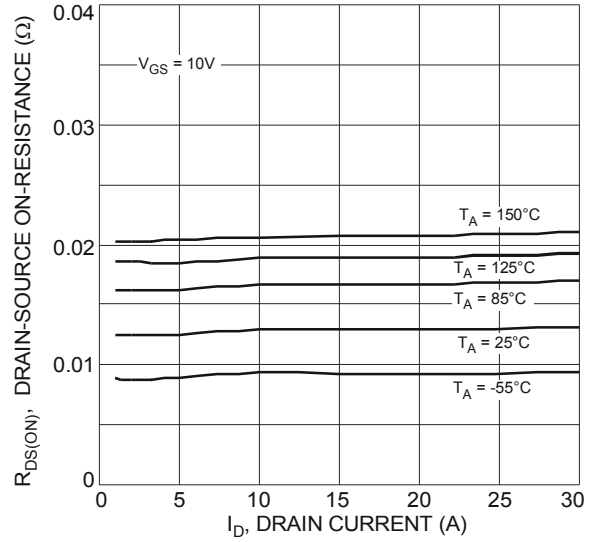


Fig. 4 Typical On-Resistance vs. Drain Current and Temperature

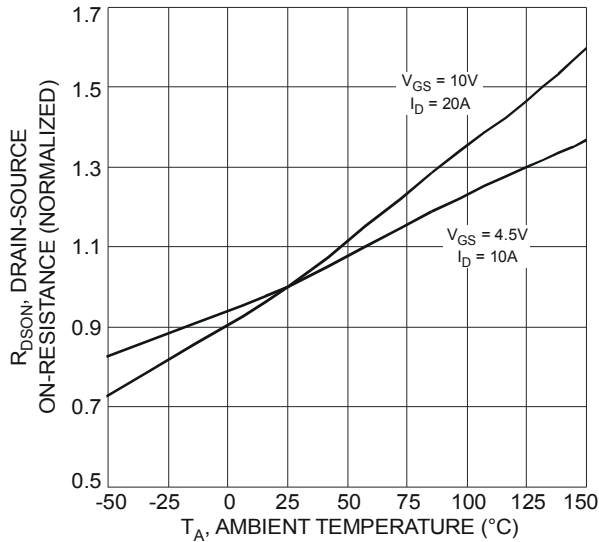


Fig. 5 On-Resistance Variation with Temperature

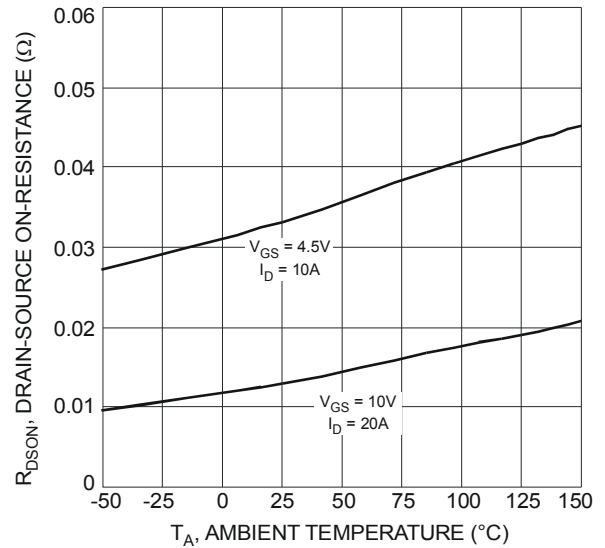


Fig. 6 On-Resistance Variation with Temperature

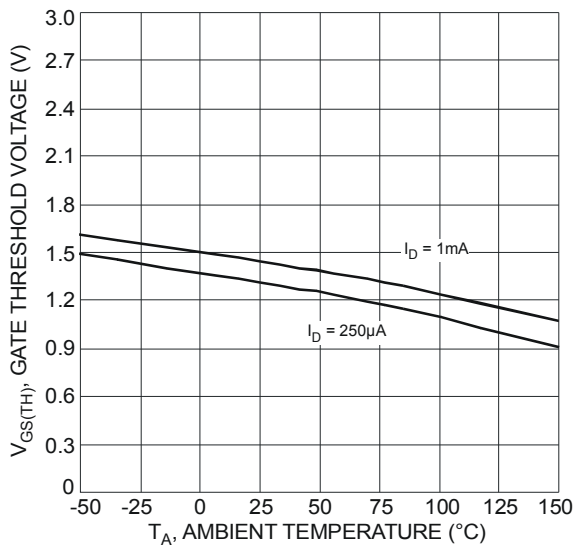


Fig. 7 Gate Threshold Variation vs. Ambient Temperature

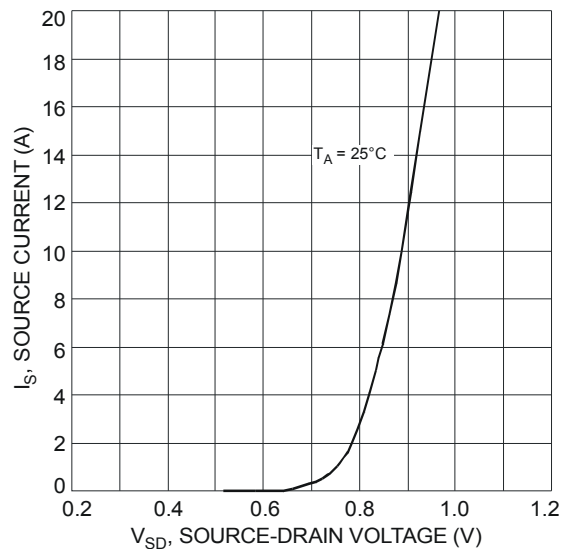


Fig. 8 Diode Forward Voltage vs. Current

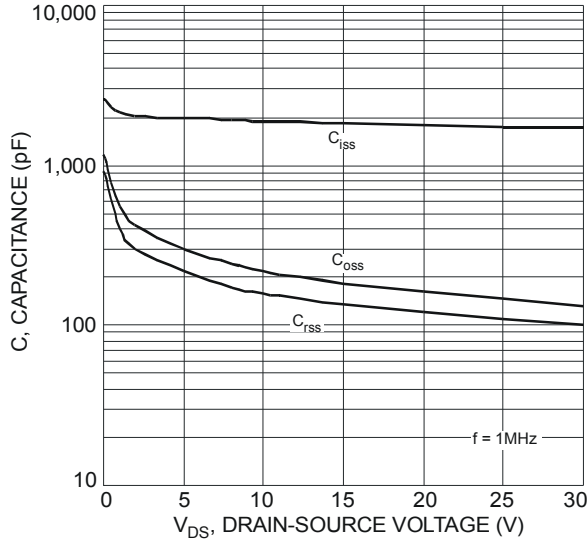


Fig. 9 Typical Total Capacitance

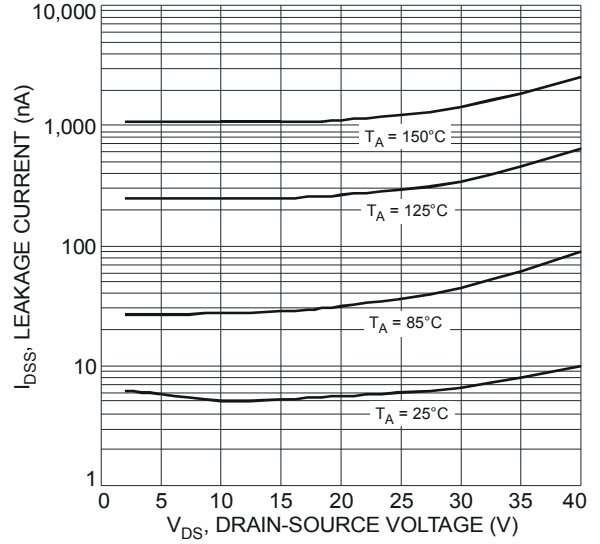


Fig. 10 Typical Leakage Current vs. Drain-Source Voltage

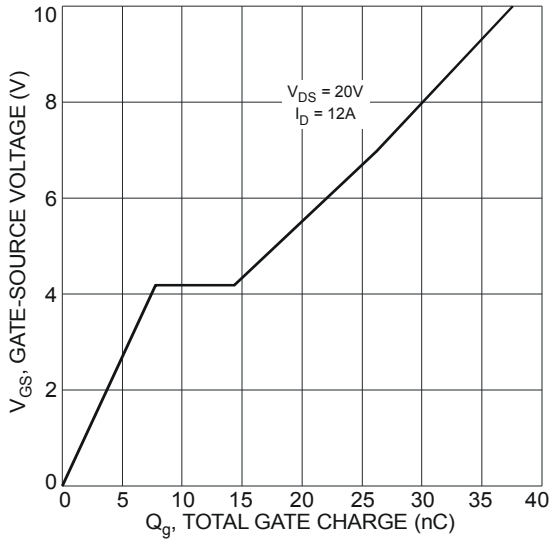


Fig. 11 Gate-Charge Characteristics

**Electrical Characteristics – Q2 P-Channel** (@ $T_A = +25^\circ\text{C}$ , unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
<b>OFF CHARACTERISTICS</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	-40	—	—	V	$I_D = -250\mu\text{A}$ , $V_{GS} = 0\text{V}$
Zero Gate Voltage Drain Current	$I_{DSS}$	—	—	-1.0	$\mu\text{A}$	$V_{DS} = -40\text{V}$ , $V_{GS} = 0\text{V}$
Gate-Source Leakage	$I_{GSS}$	—	—	$\pm 100$	nA	$V_{GS} = \pm 20\text{V}$ , $V_{DS} = 0\text{V}$
<b>ON CHARACTERISTICS</b>						
Gate Threshold Voltage	$V_{GS(th)}$	-0.8	-1.3	-1.8	V	$I_D = -250\mu\text{A}$ , $V_{DS} = V_{GS}$
Static Drain-Source On-Resistance (Note 15)	$R_{DS(on)}$	—	0.018	0.025	$\Omega$	$V_{GS} = -10\text{V}$ , $I_D = -3\text{A}$
			0.030	0.045		$V_{GS} = -4.5\text{V}$ , $I_D = -3\text{A}$
Forward Transconductance (Notes 15 & 16)	$g_{fs}$	—	16.6	—	S	$V_{DS} = -5\text{V}$ , $I_D = -3\text{A}$
Diode Forward Voltage (Note 15)	$V_{SD}$	—	-0.7	-1.0	V	$I_S = -1\text{A}$ , $V_{GS} = 0\text{V}$
<b>DYNAMIC CHARACTERISTICS (Note 16)</b>						
Input Capacitance	$C_{iss}$	—	1643	—	pF	$V_{DS} = -20\text{V}$ , $V_{GS} = 0\text{V}$ $F = 1\text{MHz}$
Output Capacitance	$C_{oss}$	—	179	—	pF	
Reverse Transfer Capacitance	$C_{rss}$	—	128	—	pF	$V_{DS} = 0\text{V}$ , $V_{GS} = 0\text{V}$ , $f = 1\text{MHz}$
Gate Resistance	$R_g$	—	6.43	—	$\Omega$	
Total Gate Charge (Note 17)	$Q_g$	—	14.0	—	nC	$V_{GS} = -4.5\text{V}$
Total Gate Charge (Note 17)	$Q_g$	—	33.7	—	nC	
Gate-Source Charge (Note 17)	$Q_{gs}$	—	5.5	—	nC	$V_{GS} = -10\text{V}$
Gate-Drain Charge (Note 17)	$Q_{gd}$	—	7.3	—	nC	
Turn-On Delay Time (Note 17)	$t_{D(on)}$	—	6.9	—	ns	$V_{DD} = -20\text{V}$ , $V_{GS} = -10\text{V}$ $I_D = -3\text{A}$
Turn-On Rise Time (Note 17)	$t_r$	—	14.7	—	ns	
Turn-Off Delay Time (Note 17)	$t_{D(off)}$	—	53.7	—	ns	
Turn-Off Fall Time (Note 17)	$t_f$	—	30.9	—	ns	

Notes: 15. Measured under pulsed conditions. Pulse width  $\leq 300\mu\text{s}$ ; duty cycle  $\leq 2\%$   
 16. For design aid only, not subject to production testing.  
 17. Switching characteristics are independent of operating junction temperatures

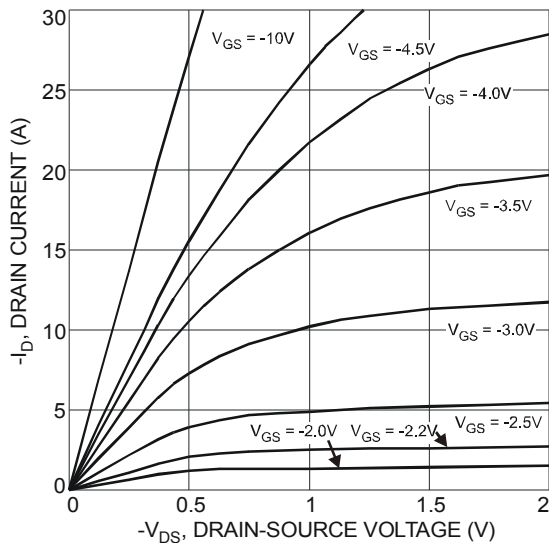
**Typical Characteristics – Q2 P-Channel**


Fig. 13 Typical Output Characteristic

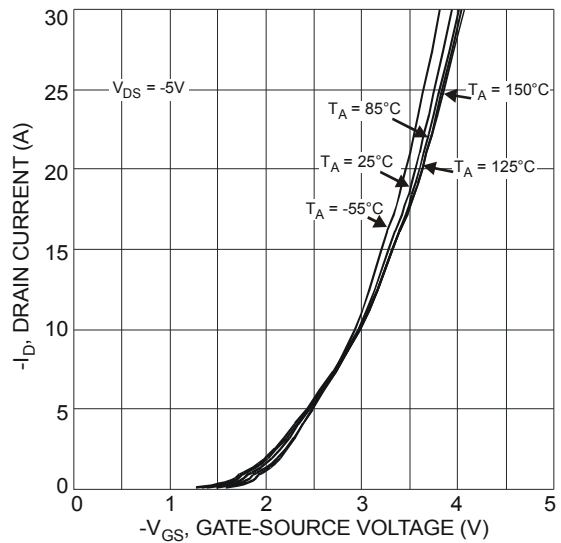


Fig. 14 Typical Transfer Characteristic

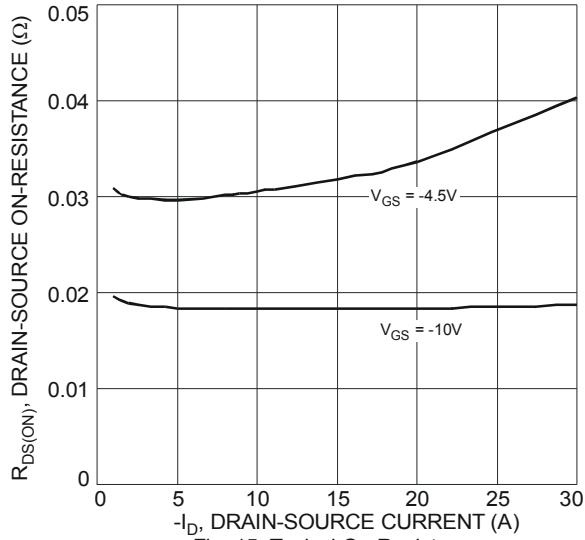


Fig. 15 Typical On-Resistance vs. Drain Current and Gate Voltage

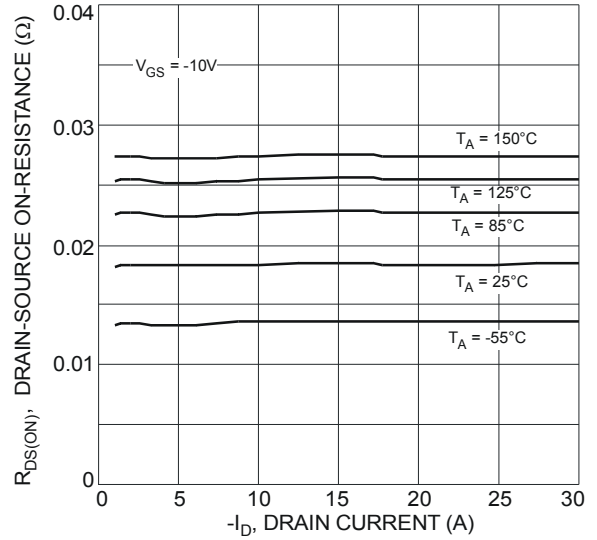


Fig. 16 Typical On-Resistance vs. Drain Current and Temperature

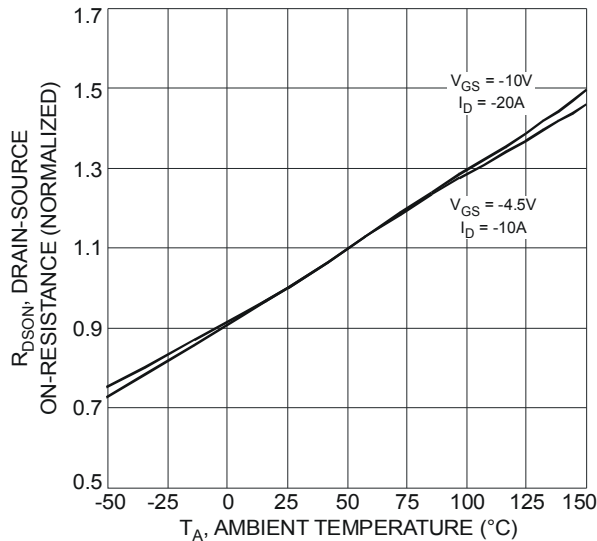


Fig. 17 On-Resistance Variation with Temperature

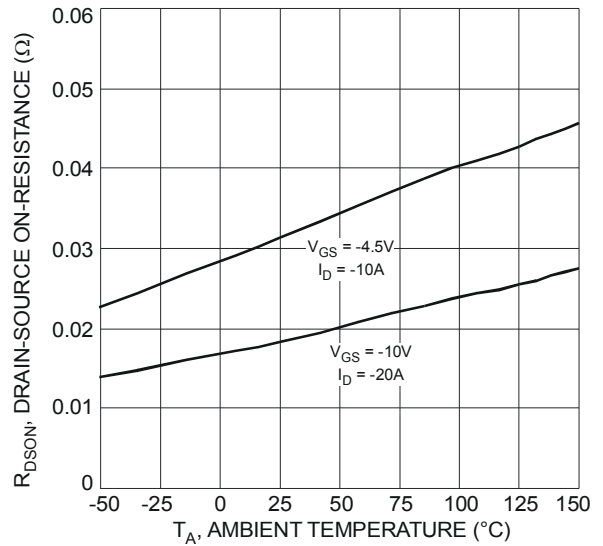


Fig. 18 On-Resistance Variation with Temperature

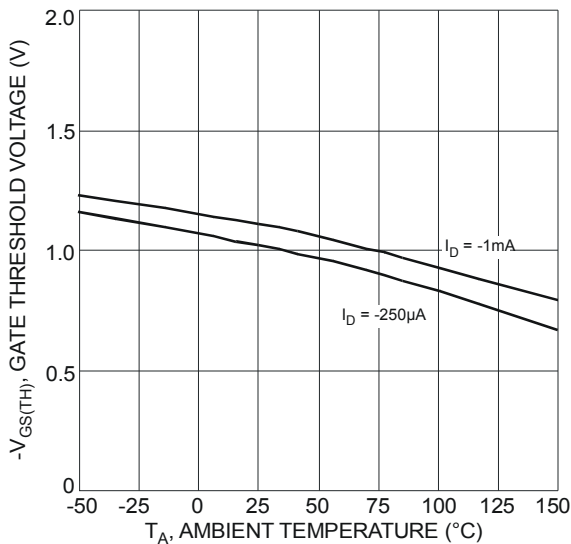


Fig. 19 Gate Threshold Variation vs. Ambient Temperature

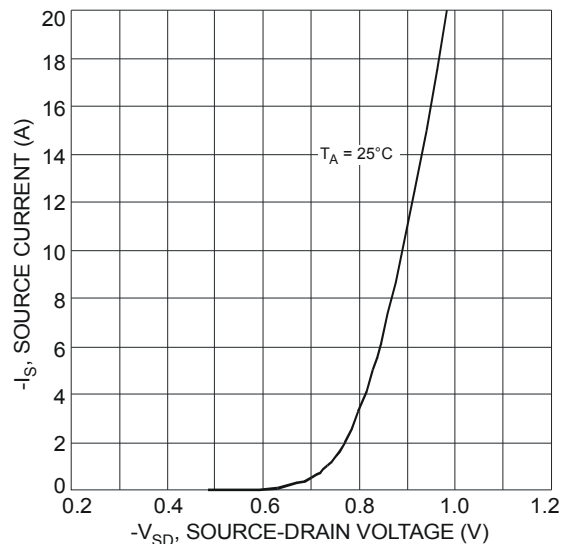


Fig. 20 Diode Forward Voltage vs. Current

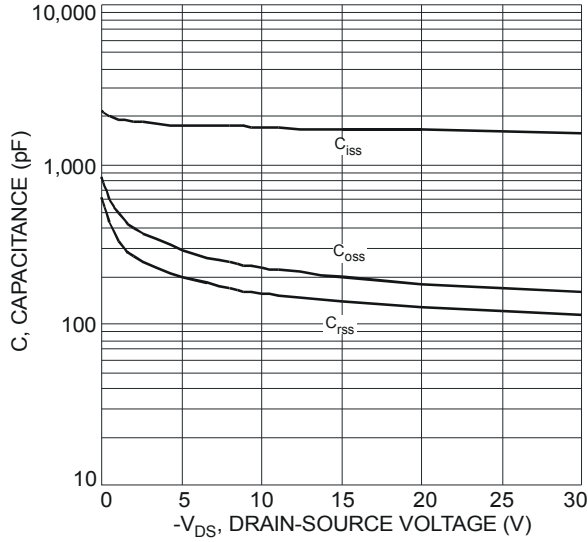


Fig. 21 Typical Total Capacitance

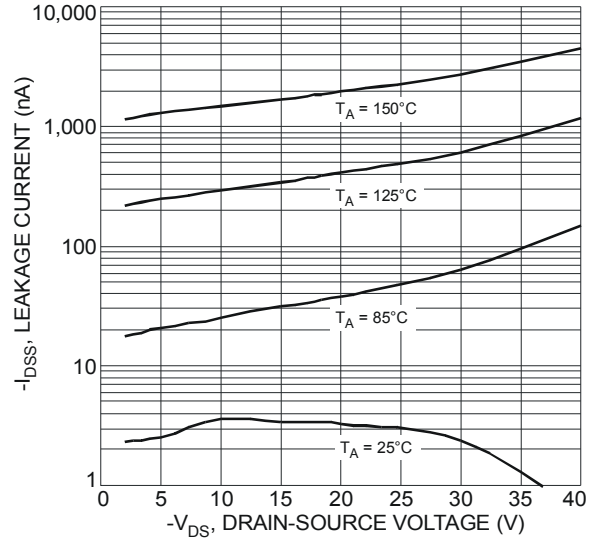


Fig. 22 Typical Leakage Current vs. Drain-Source Voltage

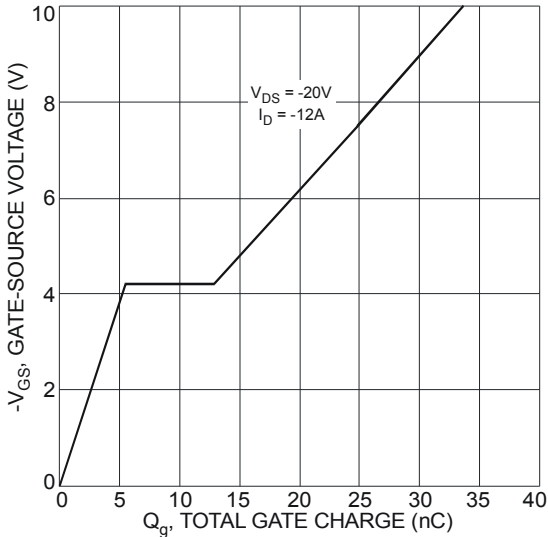
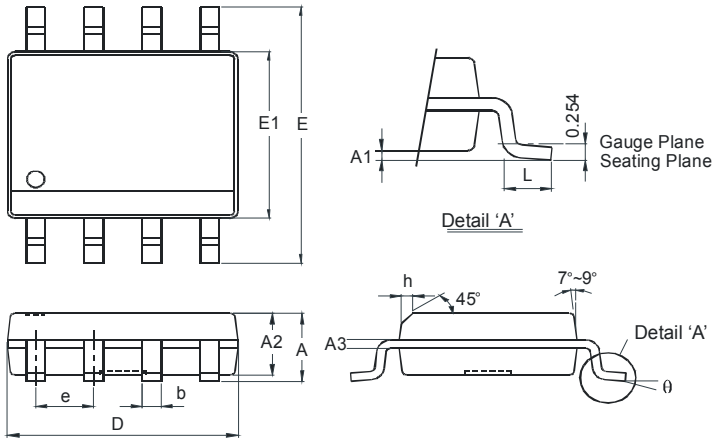


Fig. 23 Gate-Charge Characteristics

**Package Outline Dimensions**

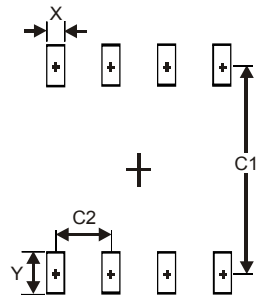
Please see AP02002 at <http://www.diodes.com/datasheets/ap02002.pdf> for the latest version.



SO-8		
Dim	Min	Max
A	-	1.75
A1	0.10	0.20
A2	1.30	1.50
A3	0.15	0.25
b	0.3	0.5
D	4.85	4.95
E	5.90	6.10
E1	3.85	3.95
e	1.27 Typ	
h	-	0.35
L	0.62	0.82
θ	0°	8°
All Dimensions in mm		

**Suggested Pad Layout**

Please see AP02001 at <http://www.diodes.com/datasheets/ap02001.pdf> for the latest version.



Dimensions	Value (in mm)
X	0.60
Y	1.55
C1	5.4
C2	1.27

NEW PRODUCT

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