



PSMN7R8-100PSE

N-channel 100 V 7.8 mΩ standard level MOSFET with improved SOA in TO220 package

11 August 2014

Product data sheet

1. General description

Standard level N-channel MOSFET with improved SOA in a TO220 package. Part of Nexperia "NextPower Live" portfolio, the PSMN7R8-100PSE is robust enough to withstand substantial in-rush and fault condition currents during turn on/off, whilst offering a low RDS(on) characteristic to keep temperatures down and efficiency up in continued use. Ideal for telecommunication systems based on 48 V backplanes / supply rails.

2. Features and benefits

- Enhanced safe operating area (SOA) for superior protection during linear mode operation
- Low RDS(on) for low conduction losses

3. Applications

- Electronic fuse
- Hot-swap / Soft-start
- Uninterruptible power supplies
- Motor control

4. Quick reference data

Table 1. Quick reference data

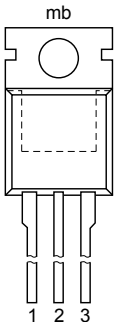
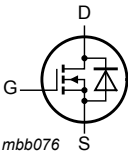
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{DS}	drain-source voltage	T _J ≥ 25 °C; T _J ≤ 175 °C	-	-	100	V
I _D	drain current	T _{mb} = 100 °C; V _{GS} = 10 V; Fig. 2	-	-	83	A
P _{tot}	total power dissipation	T _{mb} = 25 °C; Fig. 1	-	-	294	W
Static characteristics						
R _{DS(on)}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 25 A; T _J = 25 °C; Fig. 12	-	6.7	7.8	mΩ
Dynamic characteristics						
Q _{GD}	gate-drain charge	V _{GS} = 10 V; I _D = 25 A; V _{DS} = 50 V; Fig. 14 ; Fig. 15	-	41	-	nC
Q _{G(tot)}	total gate charge		-	128	-	nC

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}$; $T_{j(\text{init})} = 25\text{ °C}$; $I_D = 100\text{ A}$; $V_{sup} \leq 100\text{ V}$; $R_{GS} = 50\text{ }\Omega$; unclamped; Fig. 4	-	-	315	mJ

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 TO-220AB (SOT78)	
2	D	drain		
3	S	source		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN7R8-100PSE	TO-220AB	plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB	SOT78

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN7R8-100PSE	PSMN7R8-100PSE

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$	-	100	V

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Symbol	Parameter	Conditions		Min	Max	Unit
V _{DGR}	drain-gate voltage	T _j ≥ 25 °C; T _j ≤ 175 °C; R _{GS} = 20 kΩ		-	100	V
V _{GS}	gate-source voltage			-20	20	V
P _{tot}	total power dissipation	T _{mb} = 25 °C; Fig. 1		-	294	W
I _D	drain current	V _{GS} = 10 V; T _j = 25 °C; Fig. 2	[1]	-	100	A
		V _{GS} = 10 V; T _{mb} = 100 °C; Fig. 2		-	83	A
I _{DM}	peak drain current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C; Fig. 3		-	473	A
T _{stg}	storage temperature			-55	175	°C
T _j	junction temperature			-55	175	°C
T _{sld(M)}	peak soldering temperature			-	260	°C
Source-drain diode						
I _S	source current	T _{mb} = 25 °C	[1]	-	100	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C		-	473	A
Avalanche ruggedness						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	V _{GS} = 10 V; T _{j(initial)} = 25 °C; I _D = 100 A; V _{sup} ≤ 100 V; R _{GS} = 50 Ω; unclamped; Fig. 4		-	315	mJ

[1] Continuous current limited by package

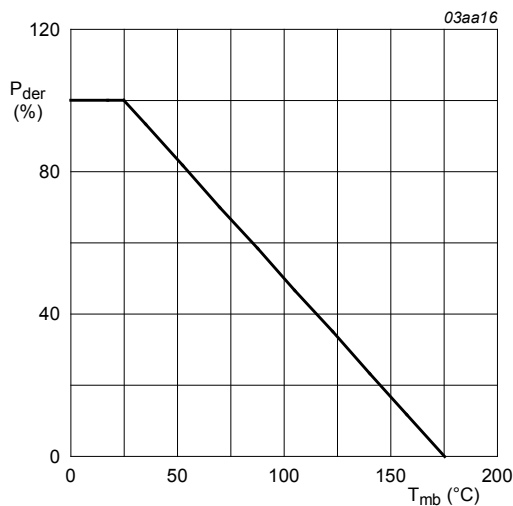
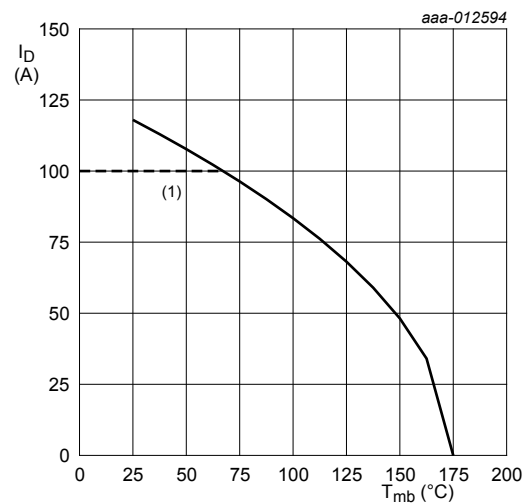


Fig. 1. Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}\text{C})}} \times 100\%$$



(1) Capped at 100A due to package

Fig. 2. Continuous drain current as a function of mounting base temperature

$$V_{GS} \geq 10V$$

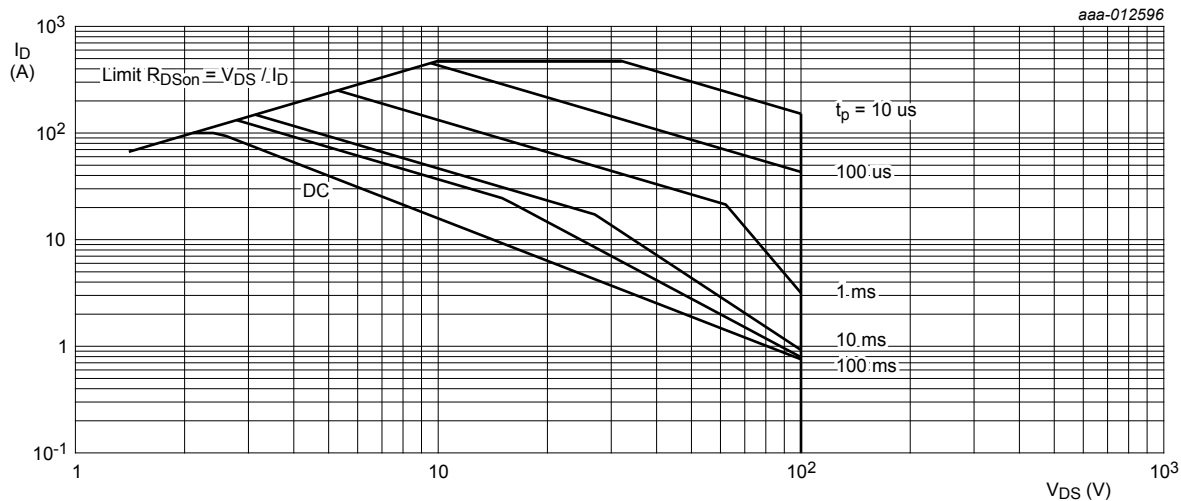


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$T_{mb} = 25^{\circ}\text{C}$; I_{DM} is a single pulse

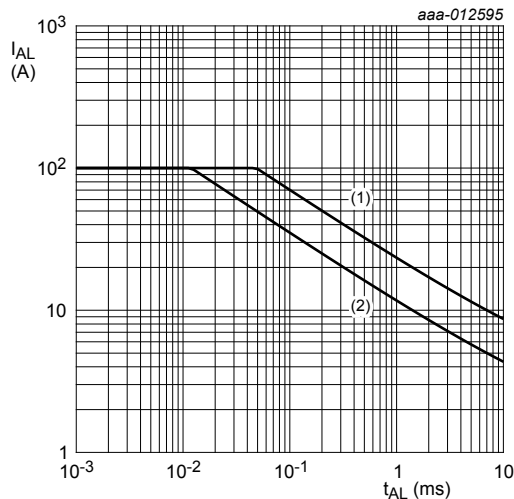


Fig. 4. Single pulse avalanche rating; avalanche current as a function of avalanche time

(1) $T_{j\ (init)} = 25^{\circ}\text{C}$; (2) $T_{j\ (init)} = 100^{\circ}\text{C}$

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	0.42	0.51	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Minimum footprint; mounted on a printed circuit board	-	50	-	K/W

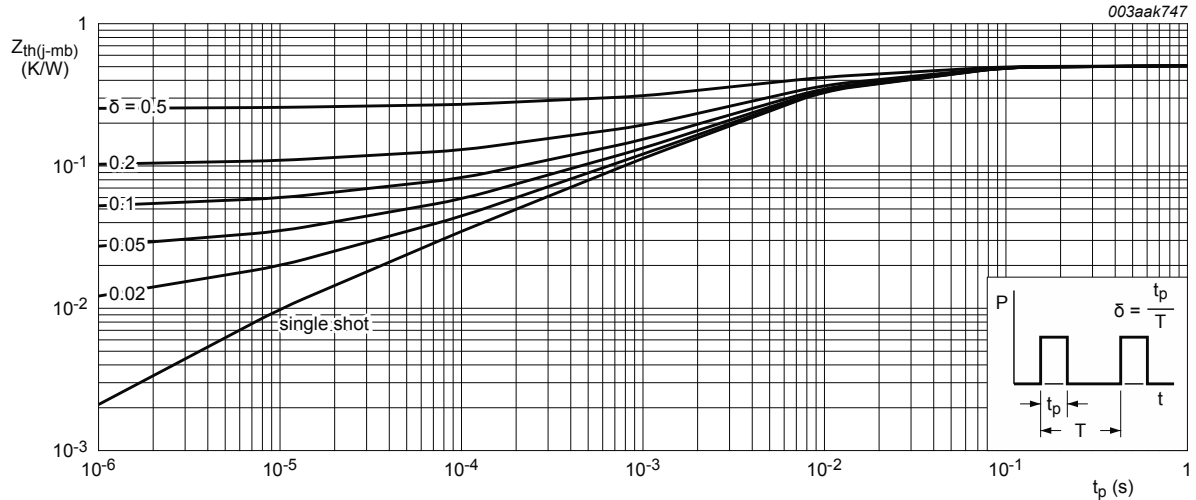


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_J = 25 ^\circ C$	100	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_J = -55 ^\circ C$	90	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 mA; V_{DS} = V_{GS}; T_J = 25 ^\circ C$; Fig. 10 ; Fig. 11	2	3	4	V
V_{GSth}	gate-source threshold voltage	$I_D = 1 mA; V_{DS} = V_{GS}; T_J = 175 ^\circ C$; Fig. 11	1	-	-	V
		$I_D = 1 mA; V_{DS} = V_{GS}; T_J = -55 ^\circ C$; Fig. 11	-	-	4.6	V
I_{DSS}	drain leakage current	$V_{DS} = 100 V; V_{GS} = 0 V; T_J = 25 ^\circ C$	-	0.1	2	μA
		$V_{DS} = 100 V; V_{GS} = 0 V; T_J = 175 ^\circ C$	-	-	500	μA
I_{GSS}	gate leakage current	$V_{GS} = -20 V; V_{DS} = 0 V; T_J = 25 ^\circ C$	-	10	100	nA
		$V_{GS} = 20 V; V_{DS} = 0 V; T_J = 25 ^\circ C$	-	10	100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10 V; I_D = 25 A; T_J = 25 ^\circ C$; Fig. 12	-	6.7	7.8	mΩ
		$V_{GS} = 10 V; I_D = 25 A; T_J = 100 ^\circ C$; Fig. 12 ; Fig. 13	-	-	14	mΩ
		$V_{GS} = 10 V; I_D = 25 A; T_J = 175 ^\circ C$; Fig. 12 ; Fig. 13	-	-	21	mΩ
R_G	gate resistance	$f = 1 MHz$	0.42	0.83	1.66	Ω

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Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Dynamic characteristics							
Q _{G(tot)}	total gate charge	I _D = 25 A; V _{DS} = 50 V; V _{GS} = 10 V; Fig. 14 ; Fig. 15		-	128	-	nC
		I _D = 0 A; V _{DS} = 0 V; V _{GS} = 10 V		-	110	-	nC
Q _{GS}	gate-source charge	I _D = 25 A; V _{DS} = 50 V; V _{GS} = 10 V; Fig. 14 ; Fig. 15		-	33	-	nC
Q _{GD}	gate-drain charge			-	41	-	nC
V _{GS(pl)}	gate-source plateau voltage	I _D = 25 A; V _{DS} = 50 V; Fig. 14 ; Fig. 15		-	5.3	-	V
C _{iss}	input capacitance	V _{DS} = 50 V; V _{GS} = 0 V; f = 1 MHz; T _j = 25 °C; Fig. 16		-	7110	-	pF
C _{oss}	output capacitance			-	450	-	pF
C _{rss}	reverse transfer capacitance			-	310	-	pF
t _{d(on)}	turn-on delay time	V _{DS} = 50 V; R _L = 2 Ω; V _{GS} = 10 V; R _{G(ext)} = 5 Ω		-	31	-	ns
t _r	rise time			-	48	-	ns
t _{d(off)}	turn-off delay time			-	82	-	ns
t _f	fall time			-	47	-	ns
Source-drain diode							
V _{SD}	source-drain voltage	I _S = 25 A; V _{GS} = 0 V; T _j = 25 °C; Fig. 17		-	0.8	1.2	V
t _{rr}	reverse recovery time	I _S = 25 A; di _S /dt = -100 A/μs; V _{GS} = 0 V; V _{DS} = 50 V		-	69	-	ns
Q _r	recovered charge			-	210	-	nC

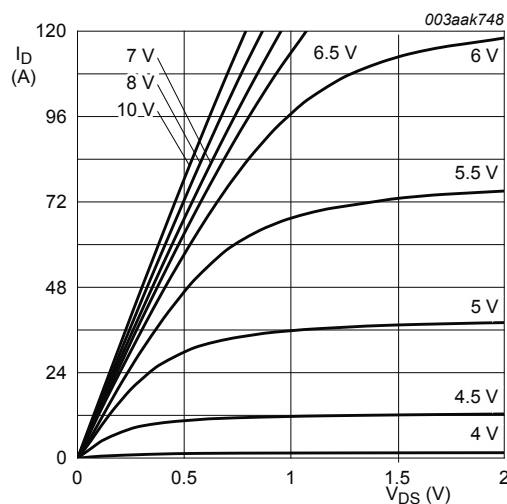


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

$T_j = 25^\circ\text{C}$

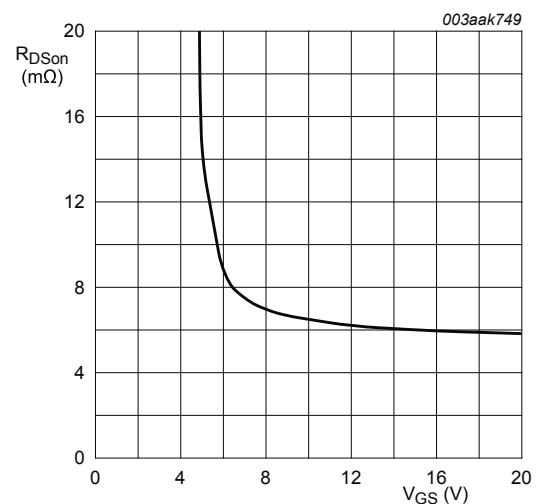


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

$T_j = 25^\circ\text{C}$; $I_D = 25 \text{ A}$

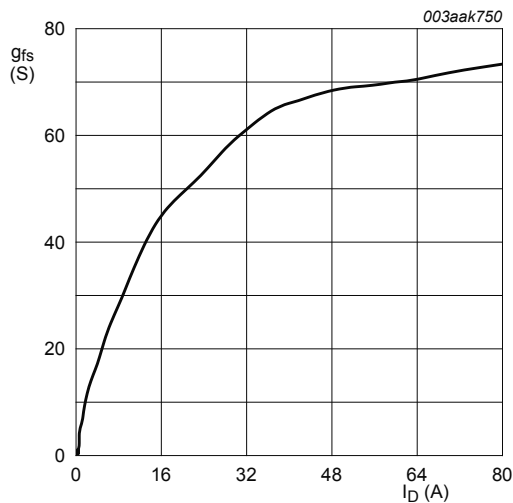


Fig. 8. Forward transconductance as a function of drain current; typical values

$T_j = 25^{\circ}\text{C}; V_{DS} = 10\text{V}$

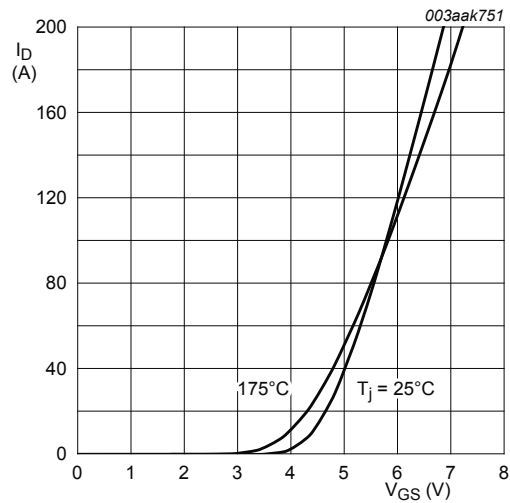


Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values

$V_{DS} = 10\text{V}$

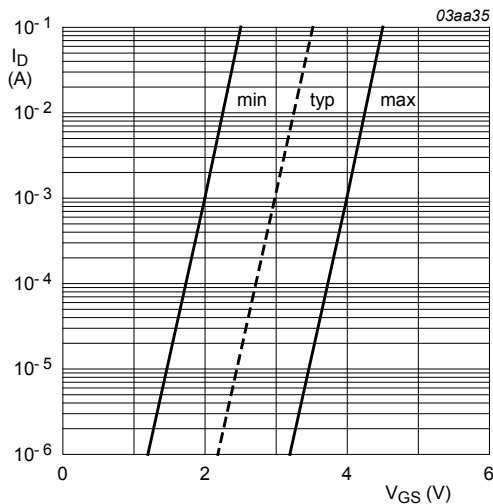


Fig. 10. Sub-threshold drain current as a function of gate-source voltage

$T_j = 25^{\circ}\text{C}; V_{DS} = 5\text{V}$

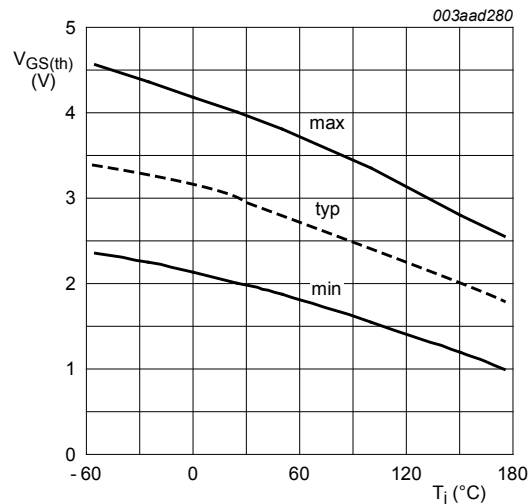


Fig. 11. Gate-source threshold voltage as a function of junction temperature

$I_D = 1\text{ mA}; V_{DS} = V_{GS}$

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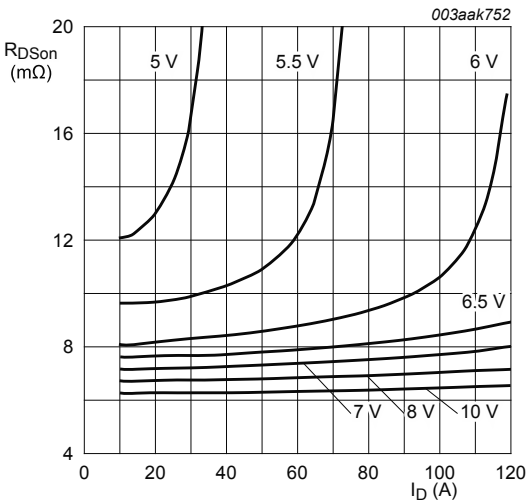


Fig. 12. Drain-source on-state resistance as a function of drain current; typical values

$T_j = 25^{\circ}C$

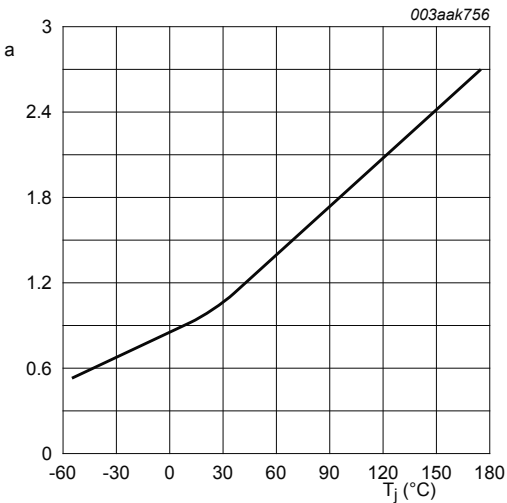


Fig. 13. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DS(on)}}{R_{DS(on)}(25^{\circ}C)}$$

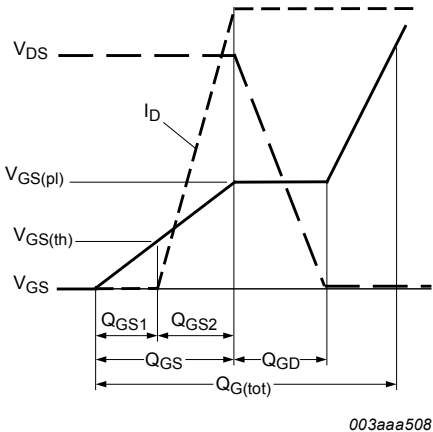


Fig. 14. Gate charge waveform definitions

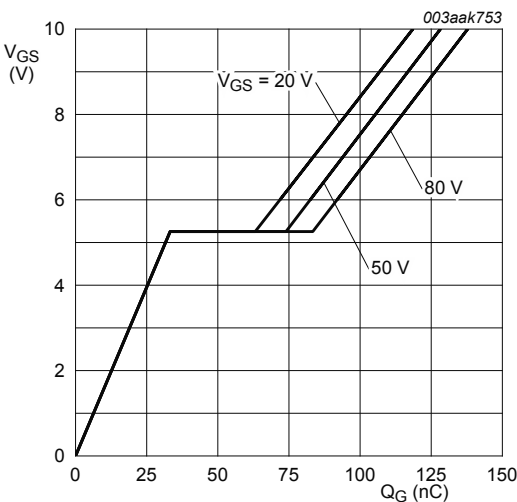


Fig. 15. Gate-source voltage as a function of gate charge; typical values

$T_j = 25^{\circ}C; I_D = 25A$

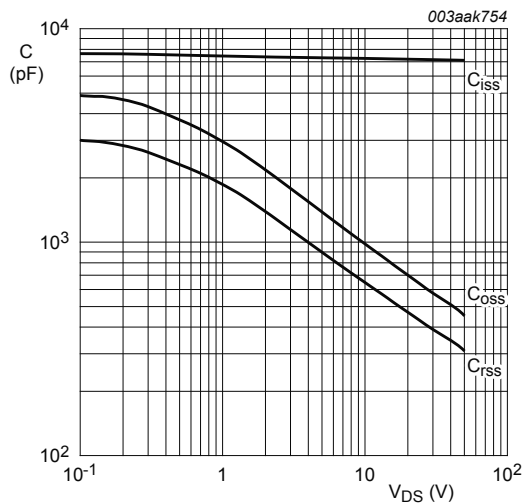


Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$V_{GS}=0V; f=1MHz$

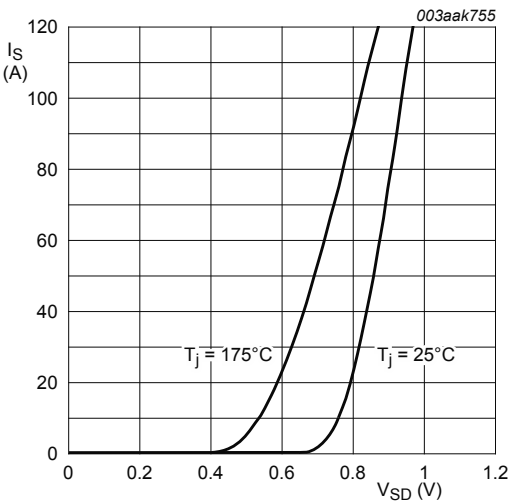


Fig. 17. Source current as a function of source-drain voltage; typical values

$V_{GS}=0V$

11. Package outline

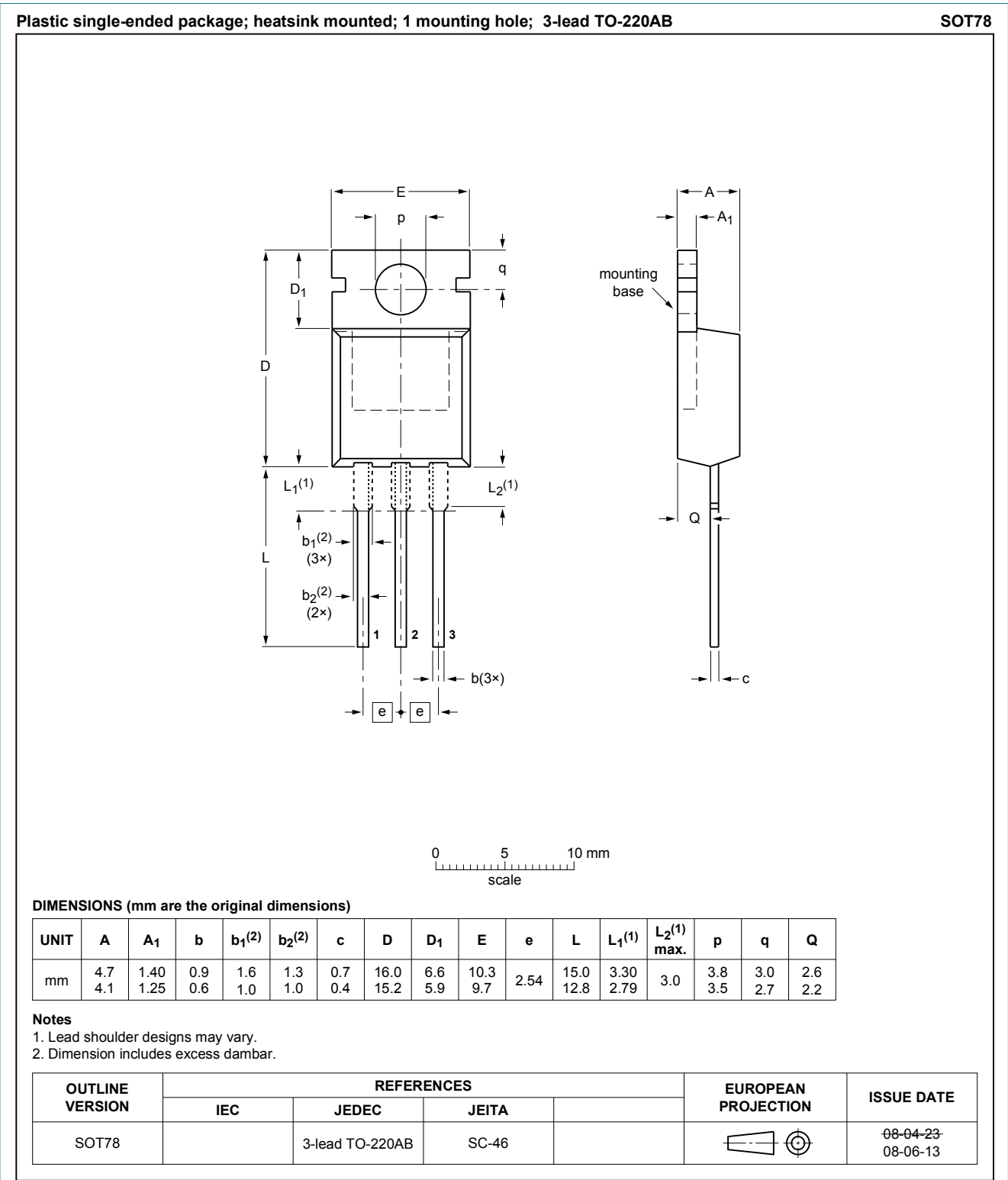


Fig. 18. Package outline TO-220AB (SOT78)

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12. Legal information

12.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
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Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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