

RJK03M5DNS

Silicon N Channel Power MOS FET Power Switching

R07DS0769EJ0110

Rev.1.10

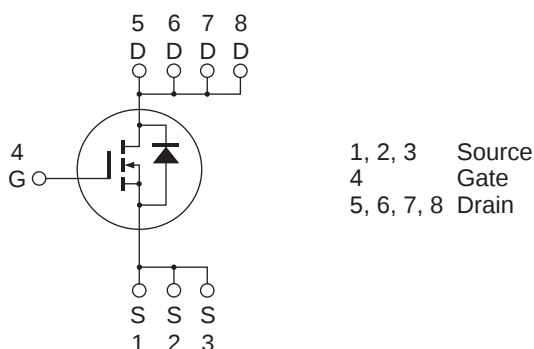
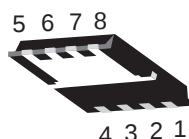
May 29, 2012

Features

- High speed switching
- Capable of 4.5 V gate drive
- Low drive current
- High density mounting
- Low on-resistance
 $R_{DS(on)} = 5.2 \text{ m}\Omega$ typ. (at $V_{GS} = 10 \text{ V}$)
- Pb-free
- Halogen-free

Outline

RENESAS Package code: PWSN0008JB-A
(Package name: HWSN-8)



1, 2, 3 Source
4 Gate
5, 6, 7, 8 Drain

Absolute Maximum Ratings

($T_a = 25^\circ\text{C}$)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	30	V
Gate to source voltage	V_{GSS}	± 20	V
Drain current	I_D	25	A
Drain peak current	$I_{D(pulse)}$ ^{Note 1}	100	A
Body-drain diode reverse drain current	I_{DR}	25	A
Avalanche current	I_{AP} ^{Note 2}	10.5	A
Avalanche energy	E_{AS} ^{Note 2}	11	mJ
Channel dissipation	P_{ch} ^{Note 3}	15	W
Channel to case thermal impedance	θ_{ch-c} ^{Note 3}	8.3	$^\circ\text{C/W}$
Channel temperature	T_{ch}	150	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

Notes: 1. $PW \leq 10 \mu\text{s}$, duty cycle $\leq 1\%$
2. Value at $T_{ch} = 25^\circ\text{C}$, $R_g \geq 50 \Omega$
3. $T_c = 25^\circ\text{C}$

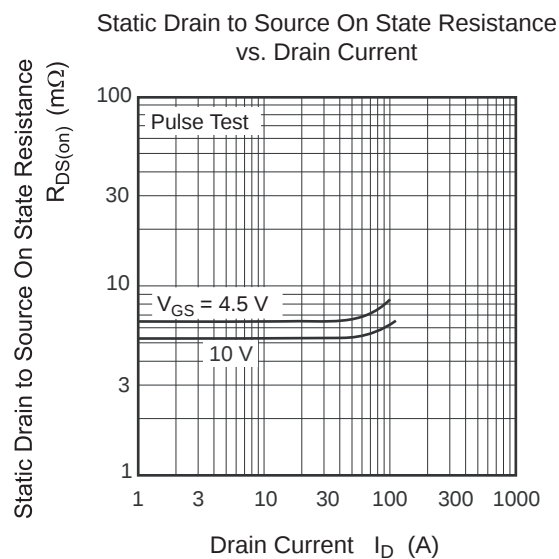
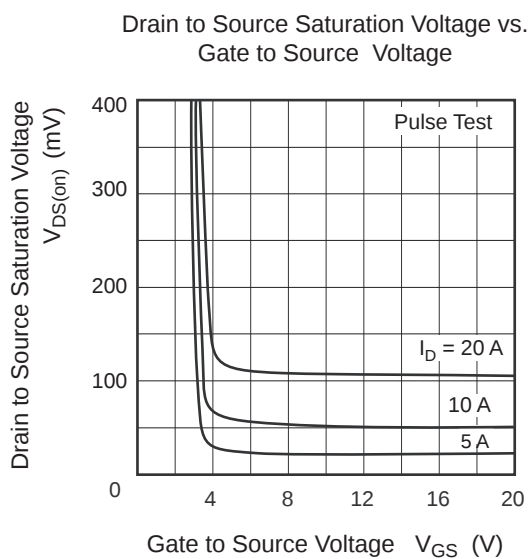
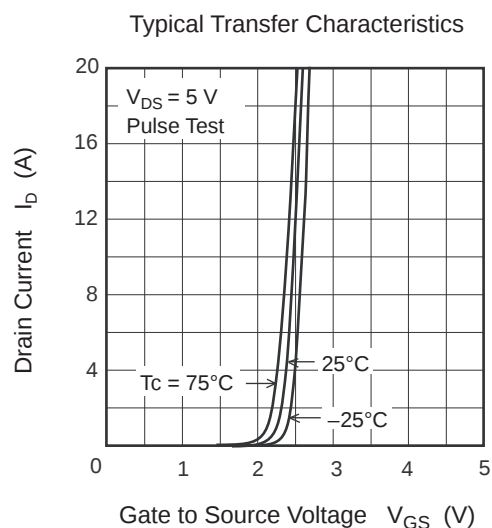
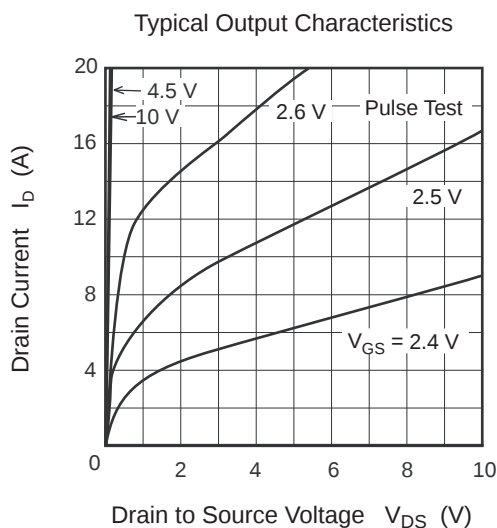
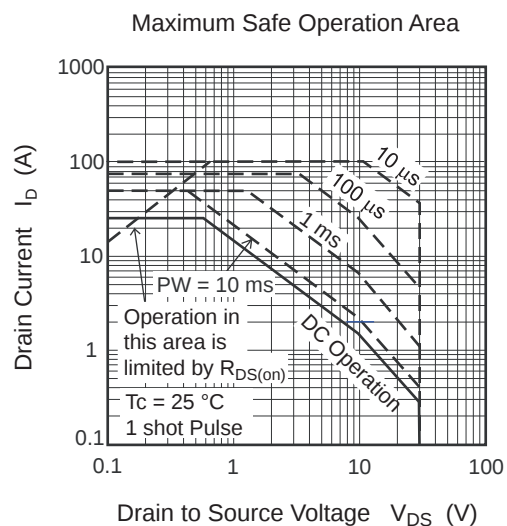
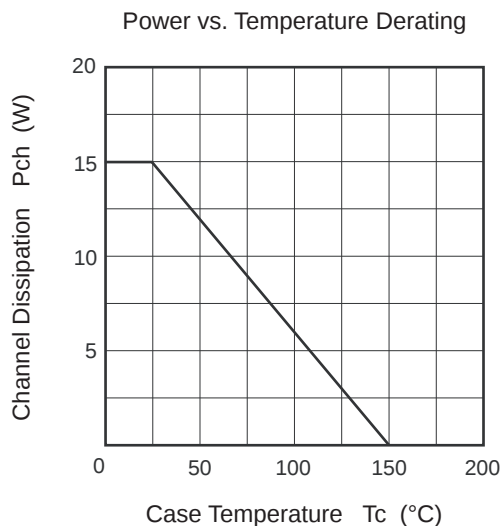
Electrical Characteristics

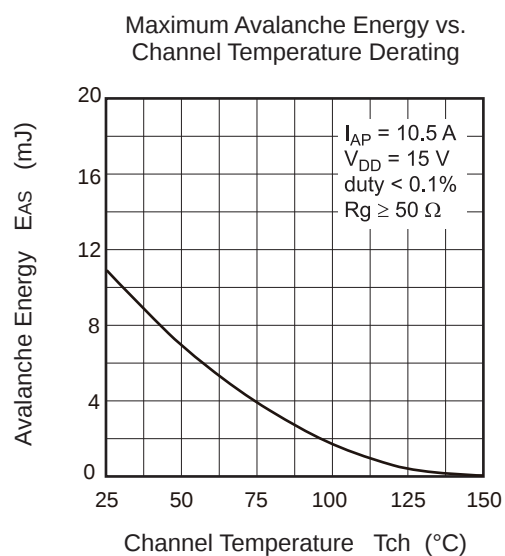
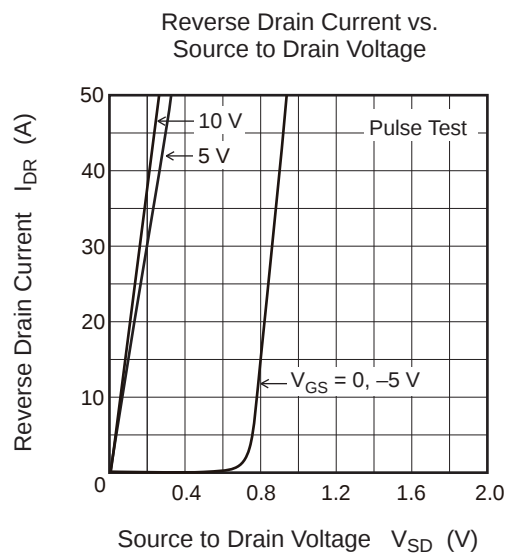
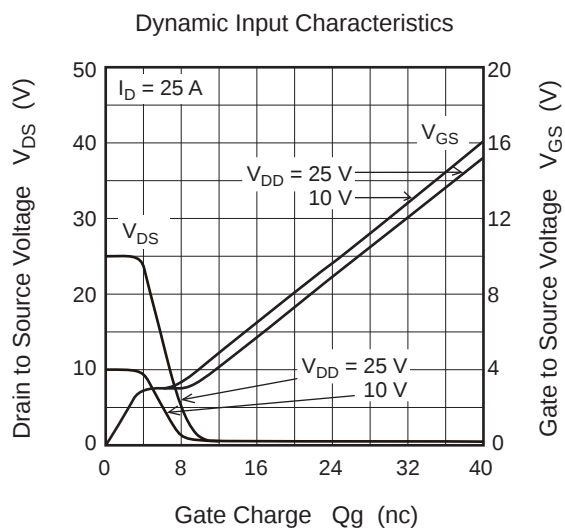
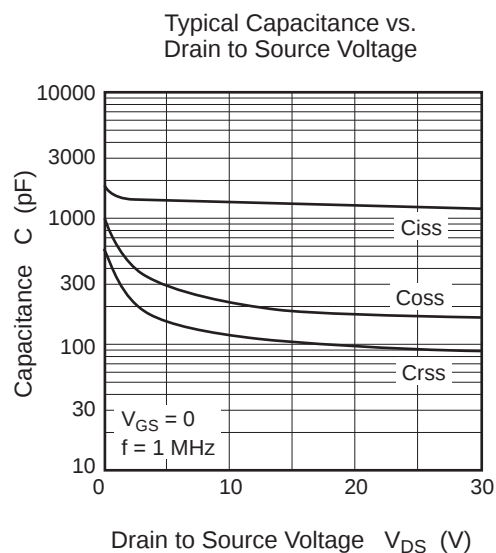
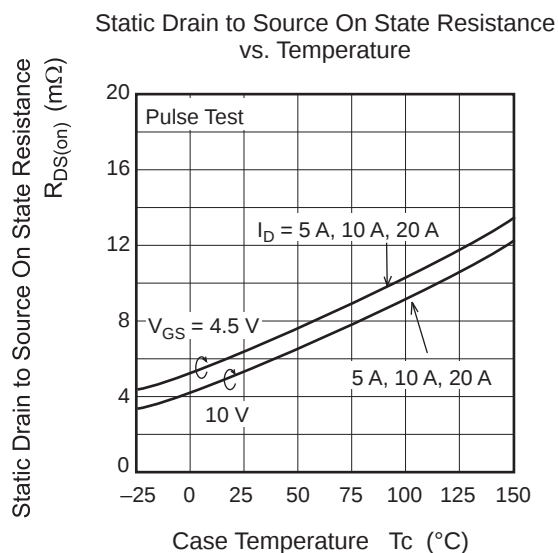
(Ta = 25°C)

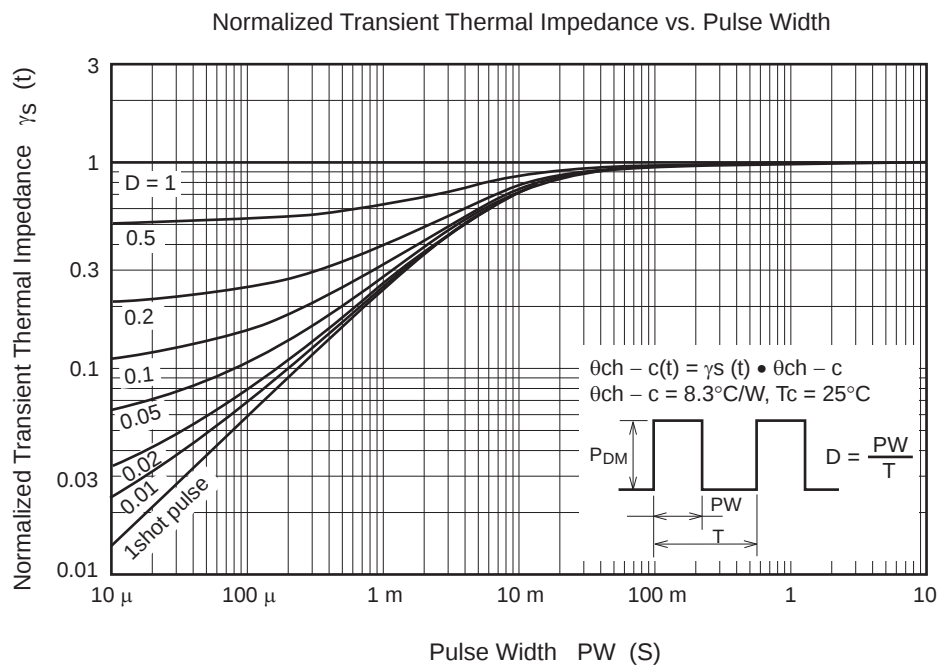
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	30	—	—	V	$I_D = 10 \text{ mA}$, $V_{GS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 0.5	μA	$V_{GS} = \pm 20 \text{ V}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	1	μA	$V_{DS} = 24 \text{ V}$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.2	—	2.5	V	$V_{DS} = 10 \text{ V}$, $I_D = 1 \text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	5.2	6.3	$\text{m}\Omega$	$I_D = 12.5 \text{ A}$, $V_{GS} = 10 \text{ V}$ ^{Note4}
	$R_{DS(on)}$	—	6.4	8.4	$\text{m}\Omega$	$I_D = 12.5 \text{ A}$, $V_{GS} = 4.5 \text{ V}$ ^{Note4}
Forward transfer admittance	$ y_{fs} $	—	60	—	S	$I_D = 12.5 \text{ A}$, $V_{DS} = 5 \text{ V}$ ^{Note4}
Input capacitance	C_{iss}	—	1350	1890	pF	$V_{DS} = 10 \text{ V}$ $V_{GS} = 0$ $f = 1 \text{ MHz}$
Output capacitance	C_{oss}	—	220	—	pF	
Reverse transfer capacitance	C_{rss}	—	120	—	pF	
Gate Resistance	R_g	—	1.4	2.8	Ω	
Total gate charge	Q_g	—	10.4	—	nC	$V_{DD} = 10 \text{ V}$ $V_{GS} = 4.5 \text{ V}$ $I_D = 25 \text{ A}$
Gate to source charge	Q_{gs}	—	4.0	—	nC	
Gate to drain charge	Q_{gd}	—	3.1	—	nC	
Turn-on delay time	$t_{d(on)}$	—	3.7	—	ns	$V_{GS} = 10 \text{ V}$, $I_D = 12.5 \text{ A}$ $V_{DD} \cong 10 \text{ V}$ $R_L = 0.8 \Omega$ $R_g = 4.7 \Omega$
Rise time	t_r	—	3.0	—	ns	
Turn-off delay time	$t_{d(off)}$	—	21.7	—	ns	
Fall time	t_f	—	7.0	—	ns	
Body-drain diode forward voltage	V_{DF}	—	0.85	1.11	V	$I_F = 25 \text{ A}$, $V_{GS} = 0$ ^{Note4}
Body-drain diode reverse recovery time	t_{rr}	—	8.8	—	ns	$I_F = 25 \text{ A}$, $V_{GS} = 0$ $di_F/dt = 500 \text{ A}/\mu\text{s}$

Notes: 4. Pulse test

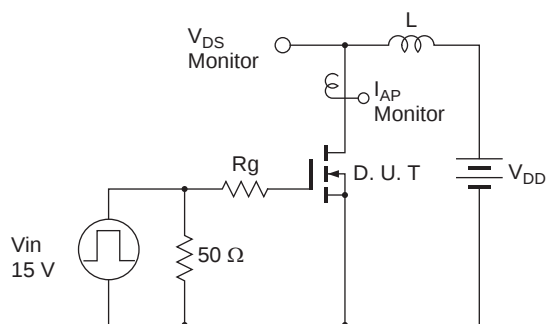
Main Characteristics





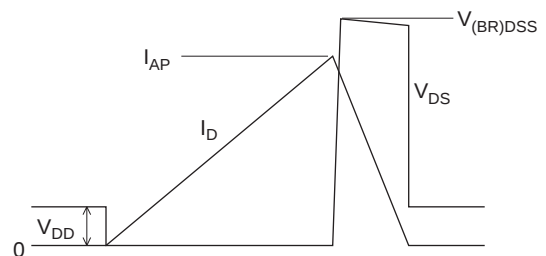


Avalanche Test Circuit

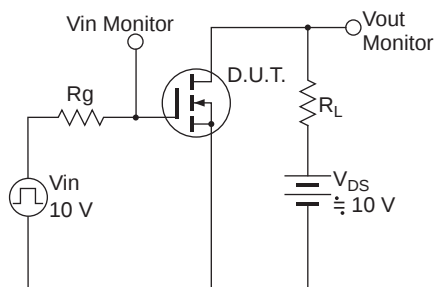


Avalanche Waveform

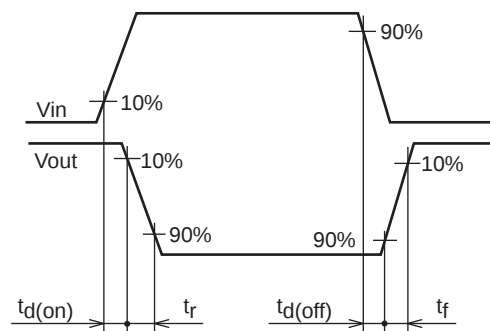
$$E_{AS} = \frac{1}{2} L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



Switching Time Test Circuit

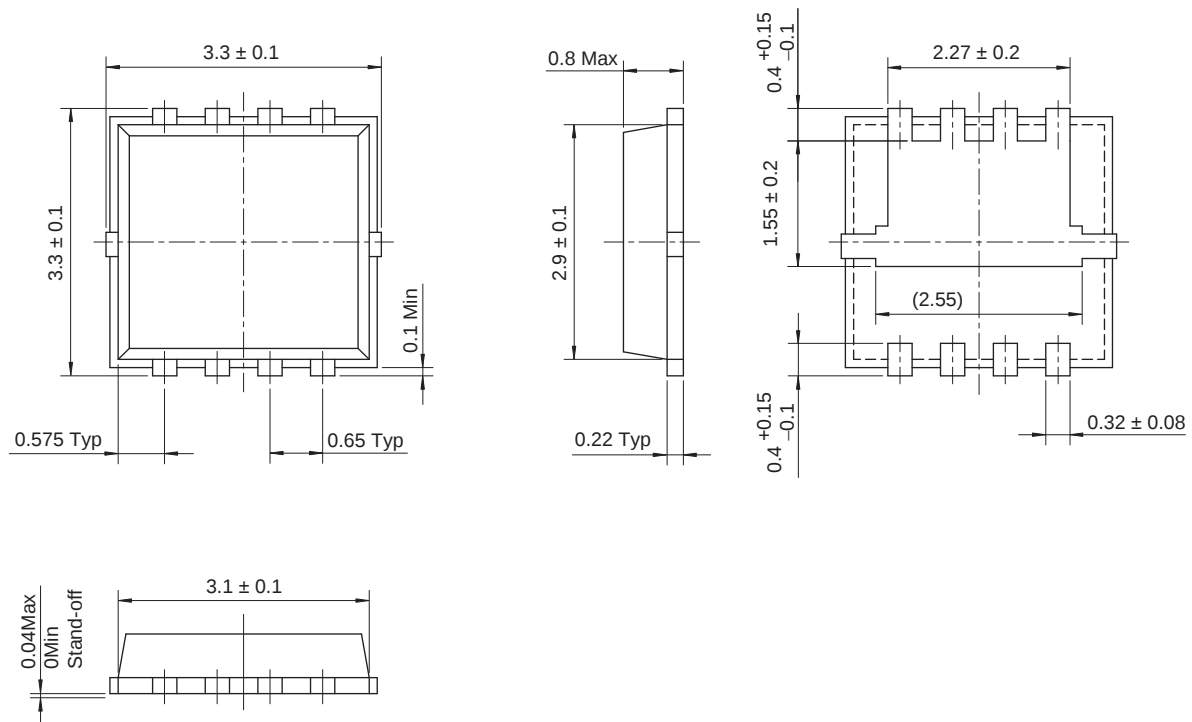


Switching Time Waveform



Package Dimensions

Package Name	JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
HWSO8-8	P-HWSO8-2.9x3.1-0.65	PWSN0008JB-A	—	0.022g



Ordering Information

Orderable Part Number	Quantity	Shipping Container
RJK03M5DNS-00-J5	5000 pcs	Taping

Note: The symbol of 2nd "-" is occasionally presented as "#".

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