

### Description

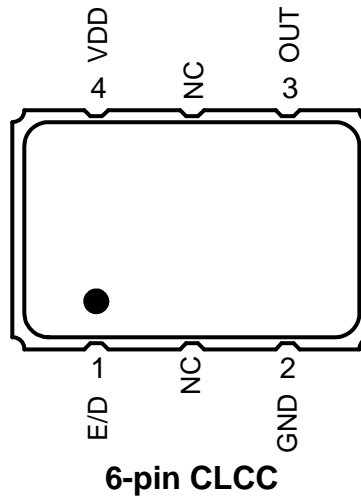
The XLH is an HCMOS Crystal Oscillator with 750fs typical phase jitter over 12kHz to 20 MHz bandwidth. Available in a wide frequency range from 0.750MHz to 250MHz, the IDT XLH Series Crystal Oscillator utilizes a family of proprietary ASICs, with a key focus on noise reduction technologies.

The 3rd order Delta Sigma Modulator reduces noise to the levels that are comparable to traditional Bulk Quartz and SAW oscillators. With short lead-time, low cost, low noise, wide frequency range, excellent ambient performance, the XLH is an excellent choice over the conventional technologies. The XLH has stabilities as tight as  $\pm 20\text{ppm}$  with extremely quick delivery for both standard and custom frequencies

### Features

- Frequency range: 0.750 to 250MHz
- Output Type: HCMOS/LVCMOS Compatible
- Frequency Stability:  $\pm 20\text{ppm}$ ,  $\pm 25\text{ppm}$ ,  $\pm 50\text{ppm}$ , or  $\pm 100\text{ppm}$
- Supply Voltage: 2.5V or 3.3V
- Phase Jitter (1.875MHz to 20MHz): 225fs typical
- Phase Jitter (12kHz to 20MHz): 750fs typical
- Package options: 3.2mm x 2.5mm x 1.0mm (JX4)  
5.0mm x 3.2mm x 1.2mm (JS4)  
7.0mm x 5.0mm x 1.3mm (JU4)
- Operating Temperatures:  $-20^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$  or  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$

### Pin Assignment



### Pin Descriptions

Pin Number	Pin Name	Description
1	E/D	Enable/Disable <sup>1</sup> (0=Output Disabled)
2	GND	Connect to ground
3	OUT	Output
4	VDD	Supply voltage

1. Pulled high internally.

## Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the XLH. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
VDD	-0.5 to +5.0V
E/D	-0.5 V to VDD + 0.5V
OUT	-0.5 V to VDD + 0.5
Storage Temperature	-55°C to 125°C
Theta Ja (Junction to Ambient)	102°C/W – Still Air

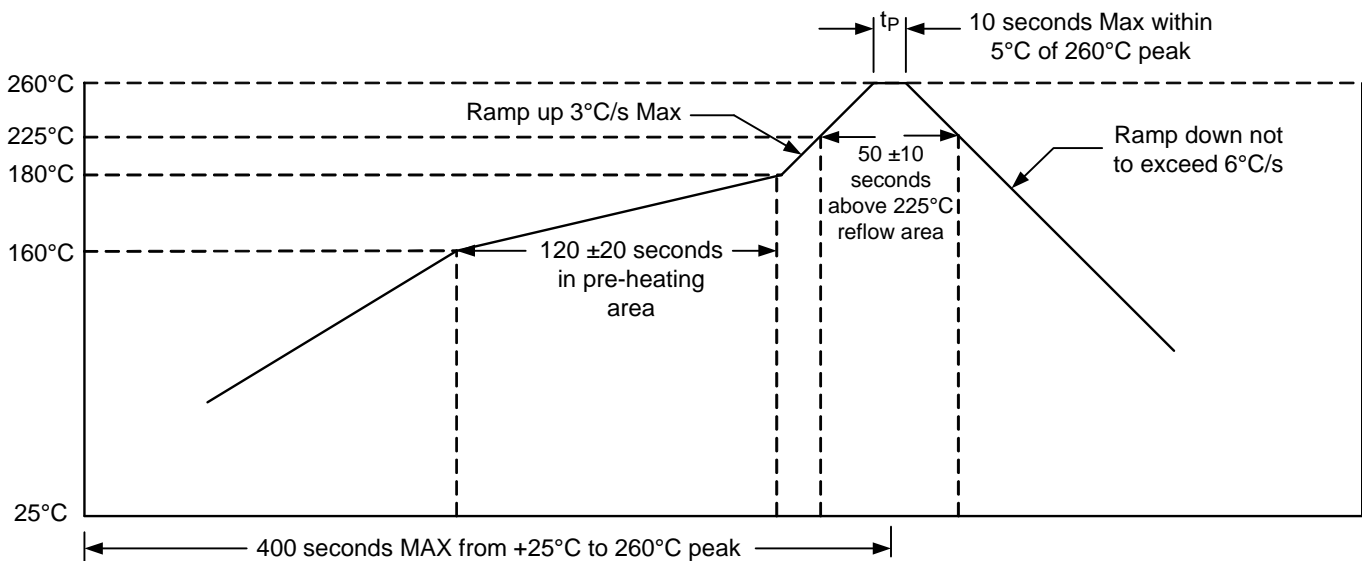
## ESD Compliance

Human Body Model (HBM)	1000V
Machine Model (MM)	150V

## Mechanical Testing

Parameter	Test Method
Mechanical Shock	Drop from 75cm to hardwood surface–3 times
Mechanical Vibration	10~55Hz, 1.5mm amplitude, 1 minute sweep 2 hours each in 3 directions (X, Y, Z)
High Temperature Burn-in	Under power at 125°C for 2000 hours
Hermetic Seal	He pressure: 4 ±1kgf/cm <sup>2</sup> 2 hour soak

## Solder Reflow Profile



## DC Characteristics

( $V_{DD} = 3.3V \pm 5\%$ ,  $T_A = -20^\circ C$  to  $+70^\circ C$ ;  $-40^\circ$  to  $+85^\circ C$ )

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Supply Current	$I_{DD}$	Standard Frequencies			55	mA
Output HIGH Voltage	$V_{OH}$	$F_{out} = 0.750$ to $150MHz$ $F_{out} = 150+$ to $250MHz$	$90\%V_{DD}$ $80\%V_{DD}$			V
Output LOW Voltage	$V_{OL}$	$F_{out} = 0.750$ to $150MHz$ $F_{out} = 150+$ to $250MHz$			$10\%V_{DD}$ $20\%V_{DD}$	V
Enable/Disable Input HIGH Voltage (Output enabled)*	$V_{IH}$		$70\%V_{DD}$			V
Enable/Disable Input LOW Voltage (Output disabled)	$V_{IL}$				$30\%V_{DD}$	V

\* A pullup resistor from pin 4 (VDD) to pin 1 (E/D) enables output when pin 1 is left open.

## AC Characteristics

( $V_{DD} = 3.3V \pm 5\%$ ,  $T_A = -20^\circ C$  to  $+70^\circ C$ ;  $-40^\circ$  to  $+85^\circ C$ )

Parameter	Symbol	Condition	Min	Typ	Max	Units
Output Frequency Range	$F_{OUTR}$		0.750		250	MHz
Frequency Stability		Temperature = $-20^\circ C$ to $+70^\circ C$	$\pm 20$		$\pm 100$	ppm
		Temperature = $-40^\circ C$ to $+85^\circ C$	$\pm 25$		$\pm 100$	ppm
Aging (1 <sup>st</sup> year)		$T_a = 25^\circ C$			$\pm 3$	
Aging (10 years)		$T_a = 25^\circ C$			$\pm 10$	
Output Load					15	pF
Start-up Time	$T_{ST}$	Output valid time after VDD meets minimum specified level			10	ms
Output Rise Time		20% to 80% $V_{DD}$			3	ns
Output Fall Time		80% to 20% $V_{DD}$			3	ns
Duty Cycle	$T_{DTCY}$	At 50% $V_{DD}$	45		55	%
Output Enable/ Disable Time	$T_{OE}$				100	ns
Period Jitter, RMS	$J_{PER}$	Frequency = 125MHz		3		psec
Random Jitter	$R_J$	Frequency = 125MHz Per MJSQ spec (Methodologies for Jitter and Signal Quality specifications)		1.2		psec
Deterministic Jitter	$D_J$			8		psec
Total Jitter	$T_J$			25.2		psec
Phase Jitter (12kHz – 20MHz)	$\phi_{JITTER}$	Frequency = 125MHz		0.75		psec
Phase Noise Performance Frequency = 125MHz	$\phi_{NOISE}$	100Hz of Carrier		-95		dBc/Hz
		1kHz of Carrier		-118		dBc/Hz
		10kHz of Carrier		-120		dBc/Hz
		100kHz of Carrier		-124		dBc/Hz
		1MHz of Carrier		-143		dBc/Hz
		10MHz of Carrier		-153		dBc/Hz
Output Frequency (Standards)	$F_{OUT}$	10MHz, 12MHz, 12.288MHz, 16MHz, 20MHz, 24MHz, 24.576MHz, 25MHz, 33.333MHz, 40MHz, 48MHz, 50MHz, 100MHz, 125MHz, 156.25MHz (Contact IDT for additional frequencies)				

Note: Inclusive of initial frequency accuracy, operating temperature range, supply variation, load variation, 3 times solder reflow, shock, vibration and 1 year aging at 25°C. We do not recommend hand soldering the devices

## DC Characteristics

( $V_{DD} = 2.5V \pm 5\%$ ,  $T_A = -20^\circ C$  to  $+70^\circ C$ ;  $-40^\circ$  to  $+85^\circ C$ )

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Supply Current	$I_{DD}$	Standard Frequencies			35	mA
Output HIGH Voltage	$V_{OH}$	$F_{out} = 0.750$ to $160$ MHz $F_{out} = 160+$ to $180$ MHz	$10\%V_{DD}$ $20\%V_{DD}$			V
Output LOW Voltage	$V_{OL}$	$F_{out} = 0.750$ to $160$ MHz $F_{out} = 160+$ to $180$ MHz			$10\%V_{DD}$ $20\%V_{DD}$	V
Enable/Disable Input HIGH Voltage (Output enabled)*	$V_{IH}$		$70\%V_{DD}$			V
Enable/Disable Input LOW Voltage (Output disabled)	$V_{IL}$				$30\%V_{DD}$	V

\* A pullup resistor from pin 4 (VDD) to pin 1 (E/D) enables output when pin 1 is left open.

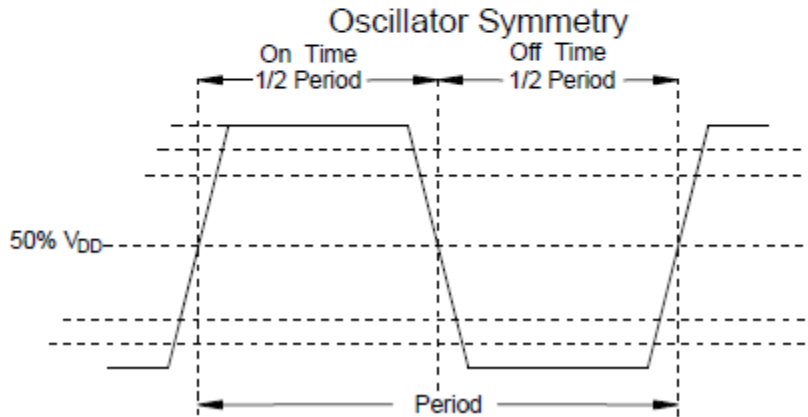
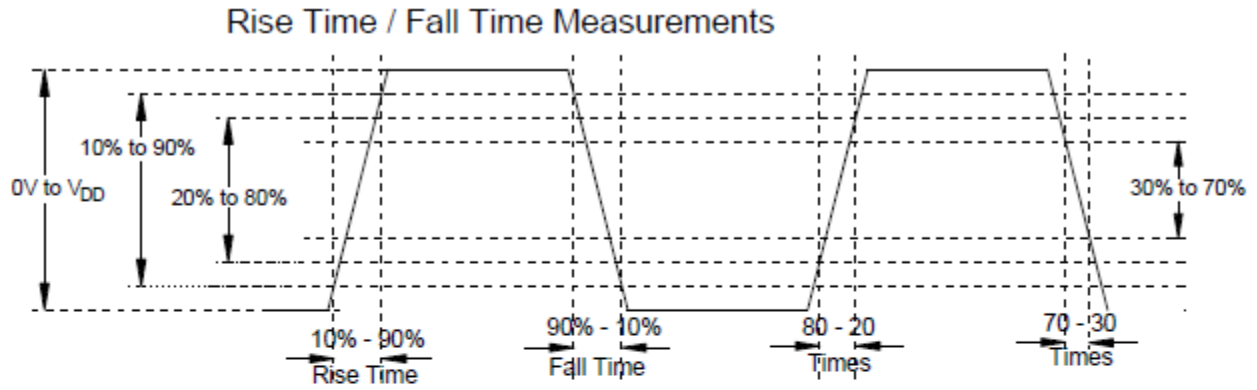
## AC Characteristics

( $V_{DD} = 2.5V \pm 5\%$ ,  $T_A = -20^\circ C$  to  $+70^\circ C$ ;  $-40^\circ$  to  $+85^\circ C$ )

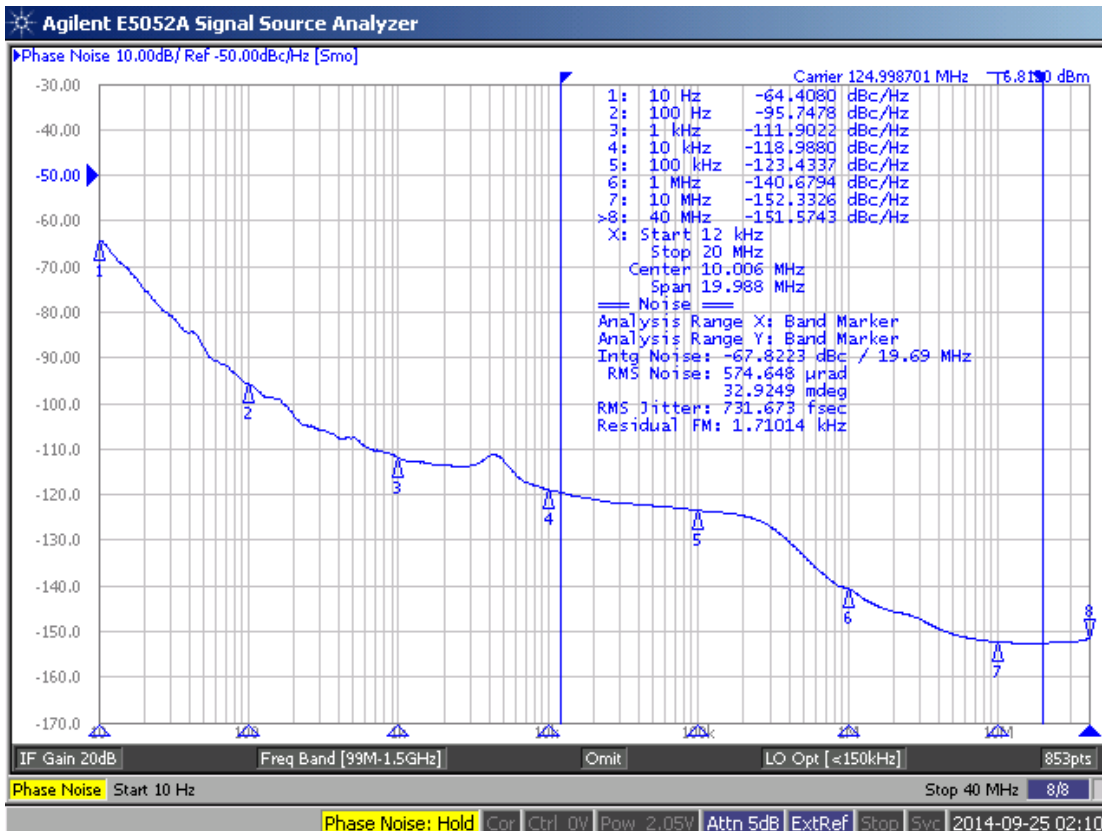
Parameter	Symbol	Condition	Min	Typ	Max	Units
Output Frequency Range	$F_{OUTR}$		0.750		180	MHz
Frequency Stability		Temperature = $-20^\circ C$ to $+70^\circ C$	$\pm 20$		$\pm 100$	ppm
		Temperature = $-40^\circ C$ to $+85^\circ C$	$\pm 25$		$\pm 100$	ppm
Output Load					15	pF
Start-up Time	$T_{ST}$	Output valid time after VDD meets minimum specified level			10	ms
Output Rise Time		20% to 80% $V_{DD}$			3	ns
Output Fall Time		80% to 20% $V_{DD}$			3	ns
Duty Cycle	$T_{DTCY}$	At 50% $V_{DD}$	45		55	%
Output Enable/ Disable Time	$T_{OE}$				100	ns
Period Jitter, RMS	$J_{PER}$	Frequency = 125MHz		3.3		psec
Random Jitter	$R_J$	Frequency = 125MHz		1.3		psec
Deterministic Jitter	$D_J$	Per MJSQ spec (Methodologies for Jitter and Signal Quality specifications)		6.7		psec
Total Jitter	$T_J$			25.6		psec
Phase Jitter (12kHz – 20MHz)	$\phi_{JITTER}$	Frequency = 125MHz		0.85		psec
Phase Noise Performance Frequency = 125MHz	$\phi_{NOISE}$	100Hz of Carrier		-91		dBc/Hz
		1kHz of Carrier		-107		dBc/Hz
		10kHz of Carrier		-117		dBc/Hz
		100kHz of Carrier		-123		dBc/Hz
		1MHz of Carrier		-140		dBc/Hz
		10MHz of Carrier		-149		dBc/Hz
Output Frequency (Standards)	$F_{OUT}$	10MHz, 12MHz, 12.288MHz, 16MHz, 20MHz, 24MHz, 24.576MHz, 25MHz, 33.333MHz, 40MHz, 48MHz, 50MHz, 100MHz, 125MHz, 156.25MHz (Contact IDT for additional frequencies)				

Note: Inclusive of initial frequency accuracy, operating temperature range, supply variation, load variation, 3 times solder reflow, shock, vibration and 1 year aging at 25°C. We do not recommend hand soldering the devices

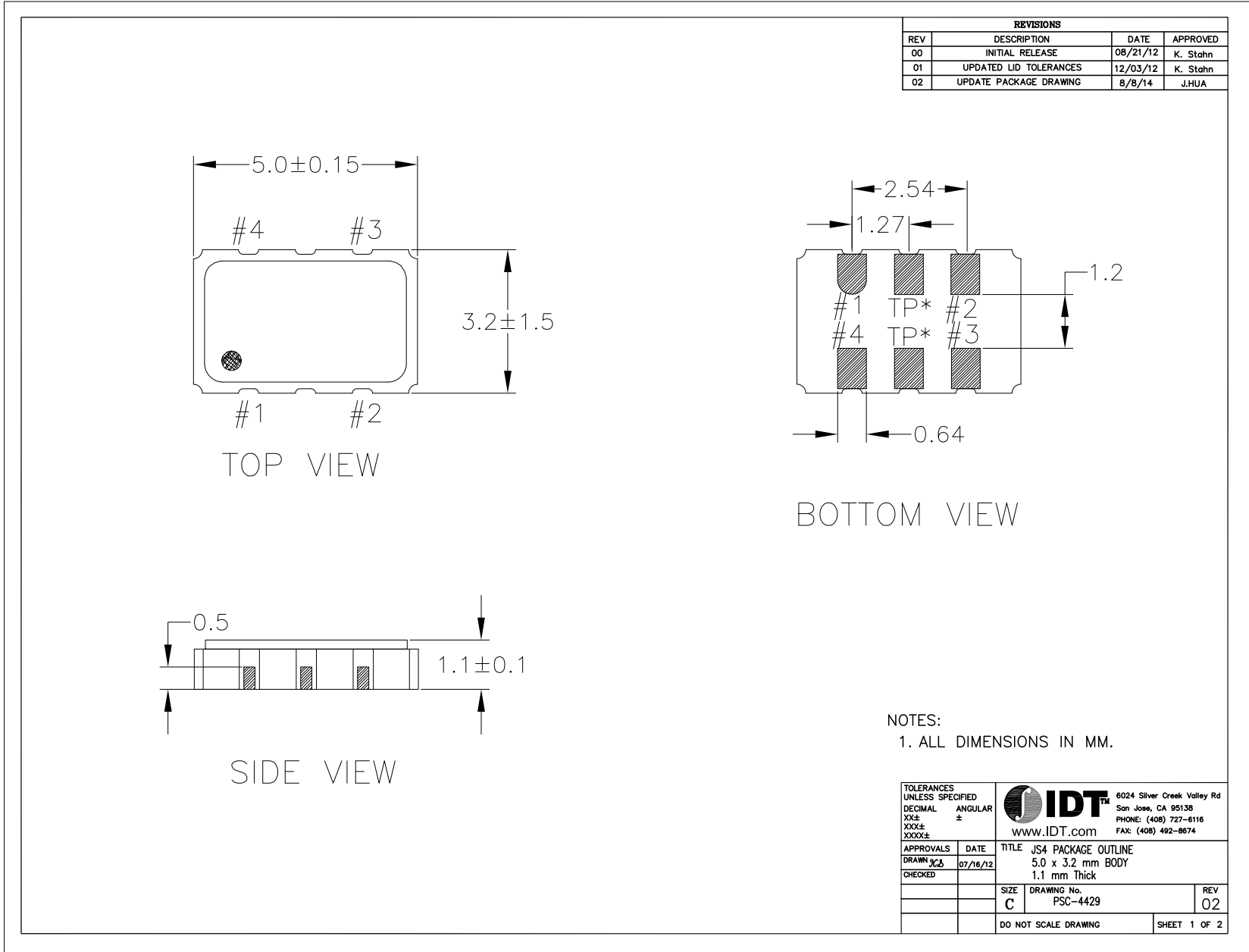
## Output Waveform



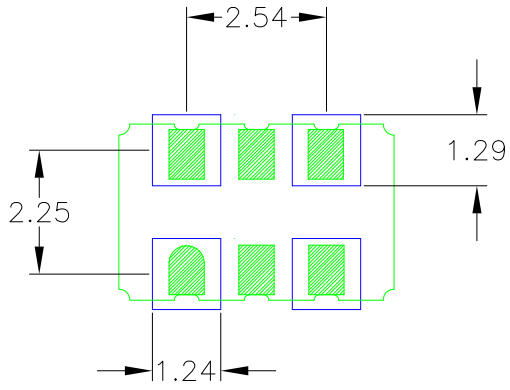
## Typical Phase Noise (3.3V)



# JS4 Package Outline and Dimensions



JS4 Package Outline and Dimensions (cont.)



RECOMMENDED LAND PATTERN

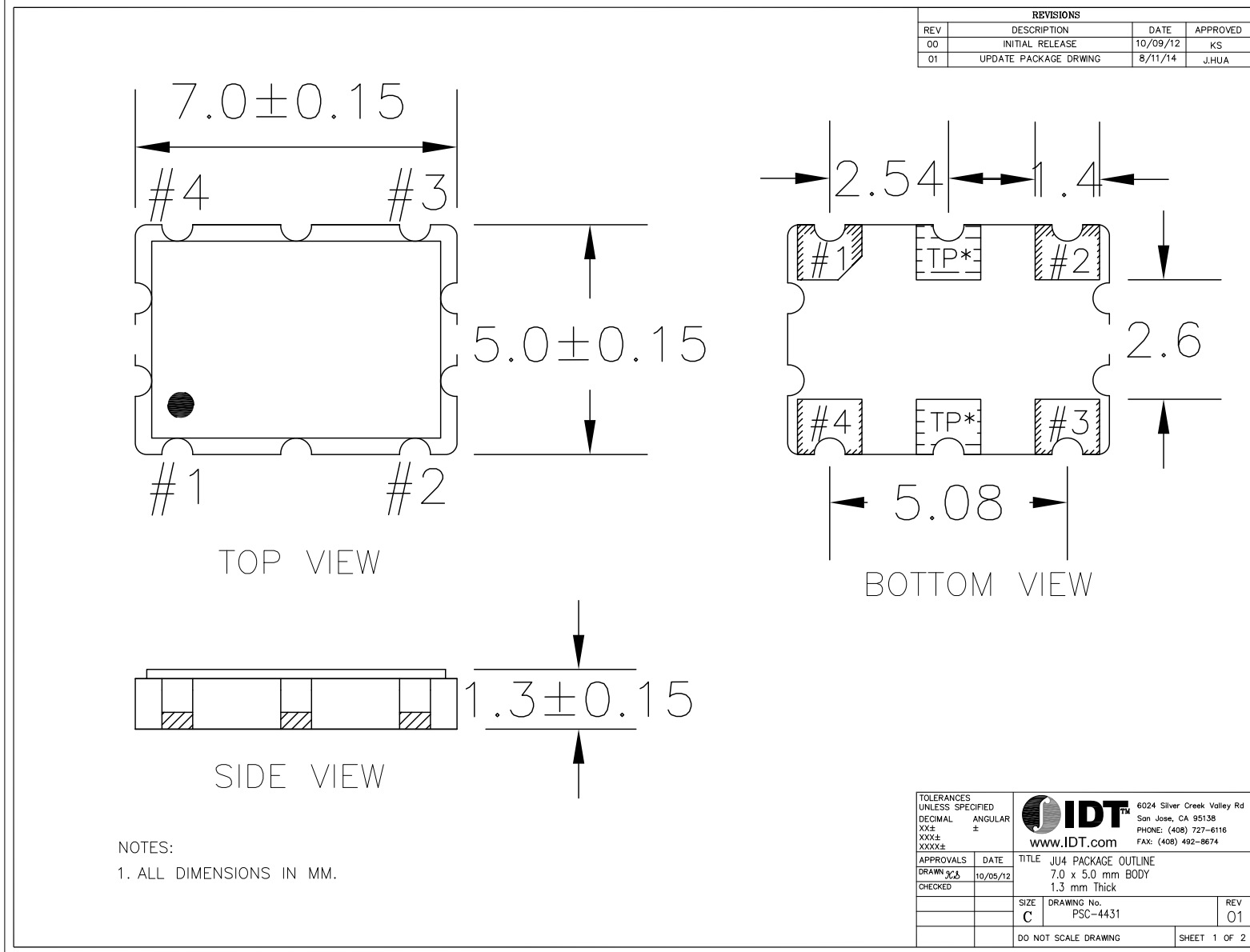
NOTES:

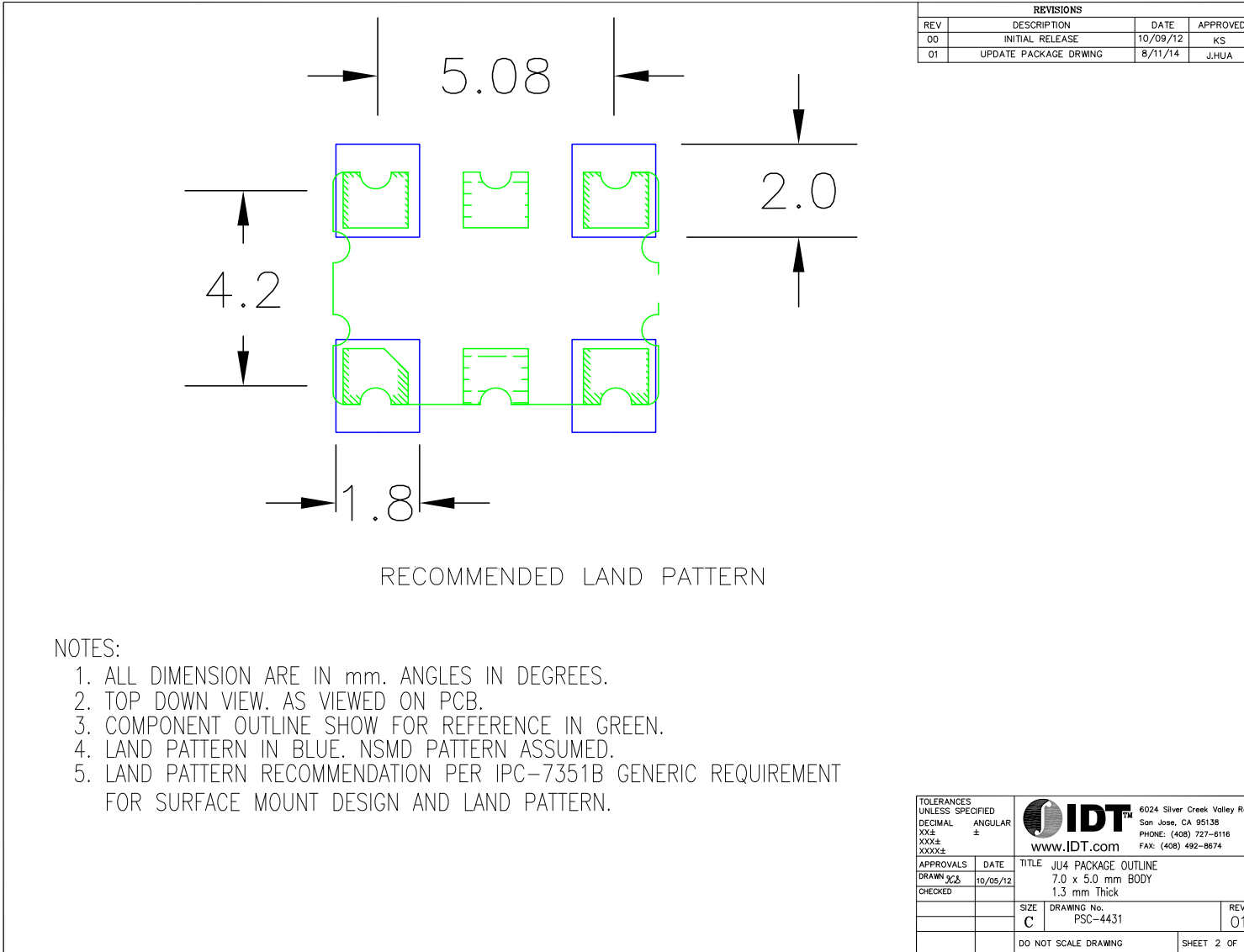
1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. COMPONENT OUTLINE SHOW FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	08/21/12	K. Stahn
01	UPDATED LID TOLERANCES	12/03/12	K. Stahn
02	UPDATE PACKAGE DRAWING	8/8/14	J.HUA

<b>TOLERANCES UNLESS SPECIFIED</b> DECIMAL    ANGULAR XXX±       ± XXXX± XXXX±		6024 Silver Creek Valley Rd San Jose, CA 95138 PHONE: (408) 727-8116 FAX: (408) 492-8674 www.IDT.com
APPROVALS    DATE DRAWN: XCS    07/16/12	TITLE JS4 PACKAGE OUTLINE 5.0 x 3.2 mm BODY 1.1 mm Thick	
CHECKED:		SIZE    DRAWING No.    REV C       PSC-4429       02
DO NOT SCALE DRAWING		SHEET 2 OF 2

# JU4 Package Outline and Dimensions

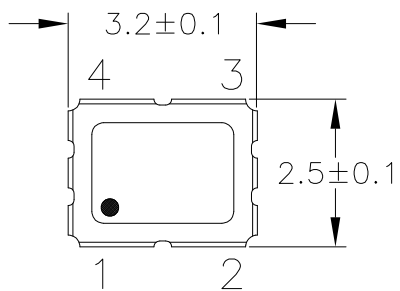




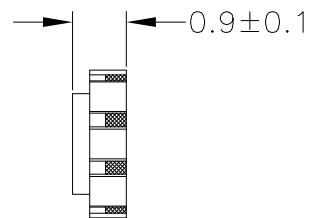
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	10/09/12	KS
01	UPDATE PACKAGE DRAWING	8/11/14	J.HUA

TOLERANCES UNLESS SPECIFIED DECIMAL ANGULAR XXX± XXXX±		6024 Silver Creek Valley Rd San Jose, CA 95138 PHONE: (408) 727-6116 FAX: (408) 492-8674 www.IDT.com	
APPROVALS	DATE		
DRAWN <i>KS</i>	10/09/12	TITLE	
CHECKED		JU4 PACKAGE OUTLINE 7.0 x 5.0 mm BODY 1.3 mm Thick	
	SIZE	DRAWING No.	REV
	C	PSC-4431	01
DO NOT SCALE DRAWING		SHEET 2 OF 2	

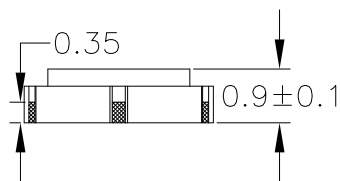
# JX4 Package Outline and Dimensions



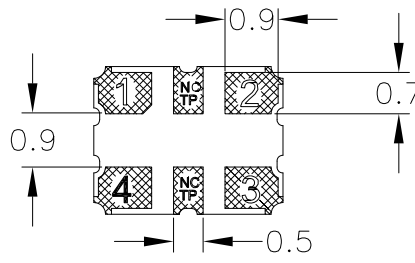
TOP VIEW



END VIEW



SIDE VIEW



BOTTOM VIEW

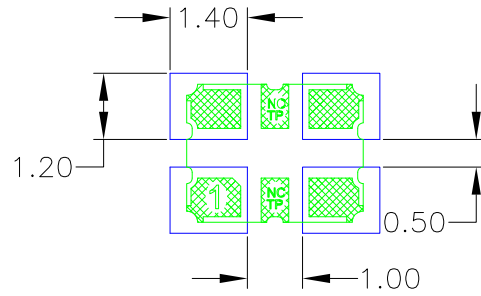
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	8/8/14	J.HUA

NOTES:

1. ALL DIMENSIONS IN MM.

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DECIMAL	ANGULAR	
XX±	±	
XXX±		
XXXX±		
APPROVALS	DATE	TITLE
DRAWN <i>RAC</i>	8/8/14	JX4 PACKAGE OUTLINE
CHECKED		3.2 x 2.5 mm BODY
		0.9 mm Thick
SIZE	DRAWING No.	REV
C	PSC-4489	00
DO NOT SCALE DRAWING		SHEET 1 OF 2

# JX4 Package Outline and Dimensions (cont.)



RECOMMENDED LAND PATTERN

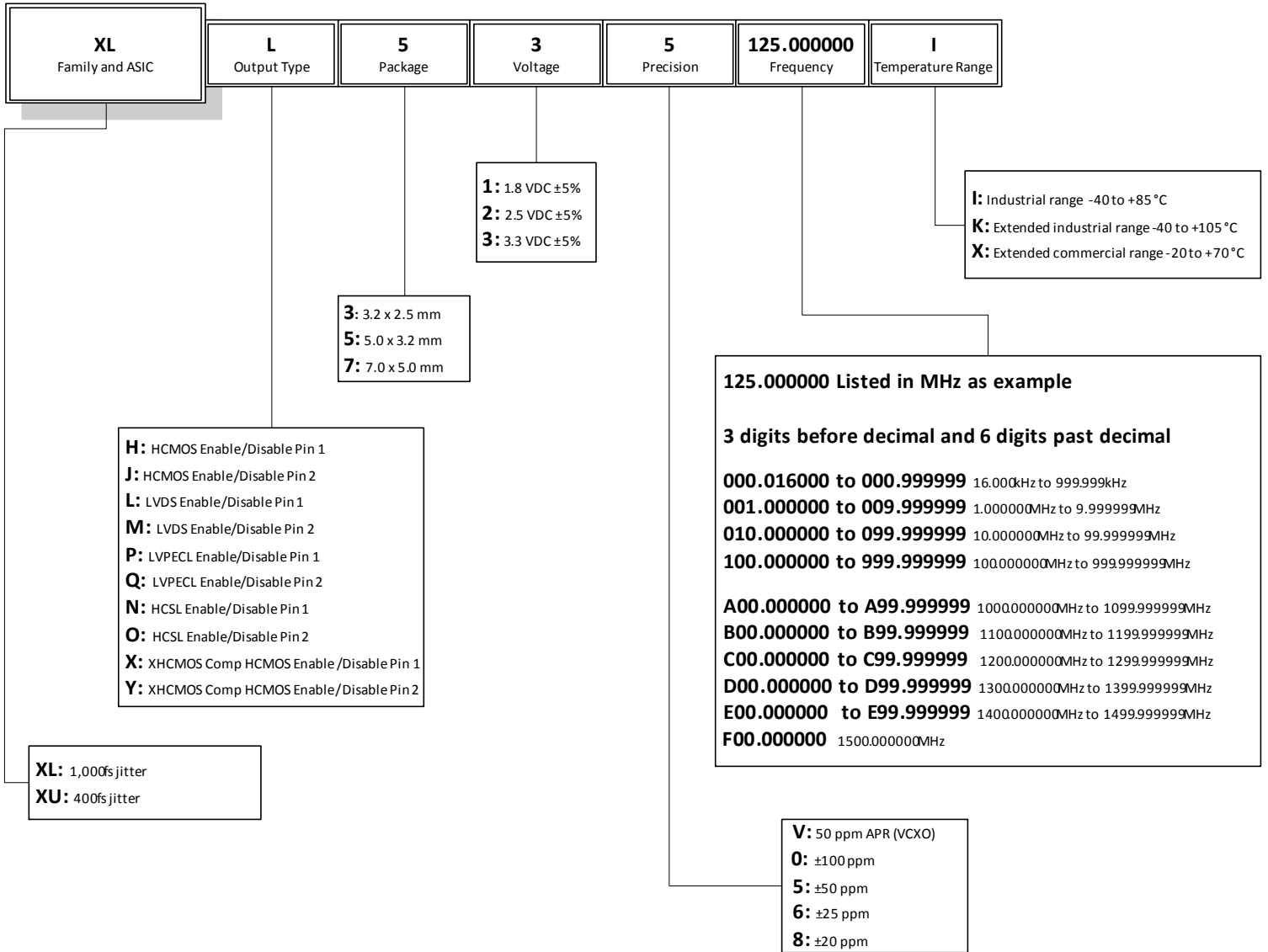
NOTES:

1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. COMPONENT OUTLINE SHOW FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	8/8/14	J.HUA

TOLERANCES UNLESS SPECIFIED		6024 Silver Creek Valley Rd San Jose, CA 95138 PHONE: (408) 727-6116 FAX: (408) 492-8674	
DECIMAL	ANGULAR	www.IDT.com	
XX±	±	APPROVALS DATE TITLE JX4 PACKAGE OUTLINE DRAWN <i>BAC</i> 8/8/14 3.2 x 2.5 mm BODY CHECKED 0.9 mm Thick	
XXX±		SIZE	REV
XXXX±		C	00
		DRAWING No.	
		PSC-4489	
DO NOT SCALE DRAWING			SHEET 2 OF 2

# IDT Ordering Information



## Revision History

Date	Originator	Description of Change
10/01/14	B. Chandhoke	1. Corrected typo in spec for Enable/Disable Low Voltage; from $\geq 30\%VDD$ to $\leq 30\%VDD$ . 2. Moved from Advance to Preliminary.
12/10/14	B. Chandhoke	1. Added 7 x 5 x 1.3mm JU4 and 3.2 x 2.5 x 1.0mm JX4 package options and package dimension/landing pattern drawings. 2. Updated ordering information table/graphic to show added package options.
10/28/16	P. Jenkins	Update ordering information decoder tables by separating them into Scheme 1 and Scheme 2; add note to distinguish the two tables.
06/13/17	L.S.	Removed "Ordering Information Scheme #1 (for reference only)". Replaced with a single ordering information table.
06/20/17	L.S.	Corrected frequency errors in Ordering Information table.



**Corporate Headquarters**  
6024 Silver Creek Valley Road  
San Jose, CA 95138 USA  
[www.IDT.com](http://www.IDT.com)

**Sales**  
1-800-345-7015 or 408-284-8200  
Fax: 408-284-2775  
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