Preliminary

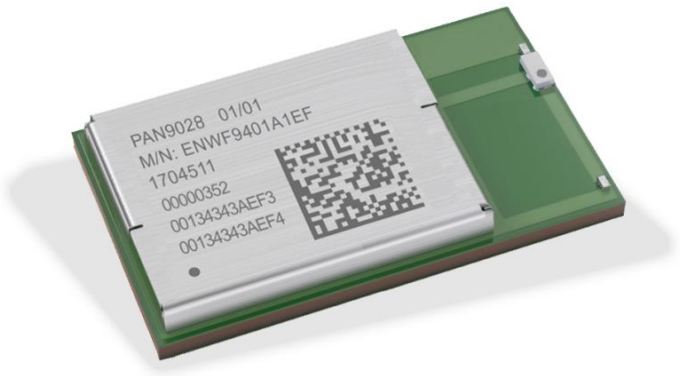
Panasonic
INDUSTRY

PAN9028

Wi-Fi Dual Band 2.4 GHz/5 GHz and Bluetooth® Module

Product Specification

Rev. 0.2



Wireless Connectivity

Overview

The PAN9028 is a 2.4 GHz and 5 GHz ISM band Wi-Fi and Bluetooth radio module, which includes a wireless radio and a power management IC for easy integration of Wi-Fi and Bluetooth connectivity into various electronic devices.

Features

- Dual band 2.4 GHz and 5 GHz 802.11 a/b/g/n/ac Wi-Fi/Bluetooth combo module
- Supports 802.11i security standards through AES, CCMP, and more security mechanism
- 802.11e Quality of Service is supported for multimedia application
- IEEE 802.11ac (Wave 2), 1×1 spatial stream with data rates up to 433 Mbps (MCS9, 80 MHz channel bandwidth)
- IEEE 802.11ac MU-MIMO beamformee
- Bluetooth 5 (includes Low Energy)
- Dual simultaneous and independent WLAN and Bluetooth operation
- Dynamic Rapid Channel Switching (DRCS) for simultaneous operation in 2.4 GHz and 5 GHz bands
- Indoor location and navigation with IEEE 802.11mc
- Power management with sleep clock
- Coexistence interface for arbitration of co-located WLAN, Bluetooth, or mobile wireless system (e.g. LTE or ZigBee®)
- Generic interfaces include SDIO 3.0 and high-speed UART for host processor connection
- Software driver Linux®

Characteristics

- Surface Mount Type (SMT) 24 mm × 12 mm × 2.8 mm
- NXP® 88W8987 WLAN 2.4 GHz and 5 GHz and Bluetooth single-chip solution inside
- Single power supply: 3.3 V with Marvell® 88PG823 Power Management IC (optional)
- Tx power: 16 dBm at 802.11b
- Rx sensitivity: –97 dBm at 802.11b DSSS 1 Mbps
- IEEE 802.11ac 20 MHz, 40 MHz, 80 MHz channel bandwidth
- Long and Short Guard Interval support
- Current consumption Wi-Fi typical 320 mA (at Tx) and 60 mA (at Rx)
- SDIO 1 bit or 4 bit
- Wide temperature range of -30 °C to 85 °C

Block Diagram

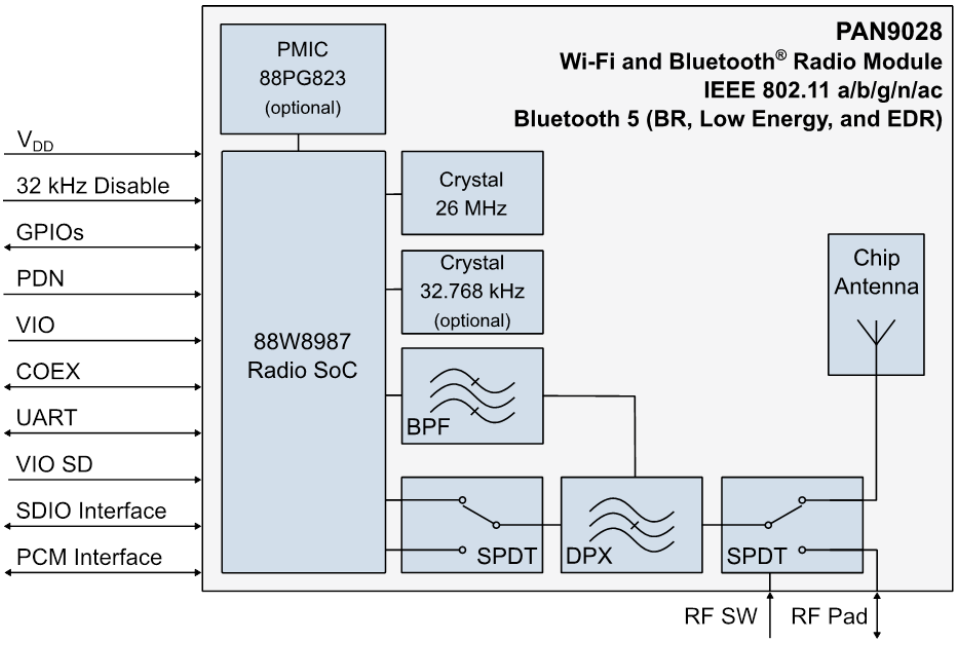


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Table of Contents

1 About This Document

1.1 Purpose and Audience

This Product Specification provides details on the functional, operational, and electrical characteristics of the Panasonic PAN9028 module. It is intended for hardware design, application, and Original Equipment Manufacturers (OEM) engineers. The product is referred to as “the PAN9028” or “the module” within this document. Unless otherwise stated the data in this document is valid for all module variants.

1.2 Revision History

Revision	Date	Modifications/Remarks
0.1	2017-09-15	First preliminary version
0.2	2020-08-28	New design. Added CPU frequencies, chapter “Restricted End Use”, additional module and kit variants and versions, second module variant without PMIC and 32 kHz, module specific parameters, MR variant. Changed storage temperature. Updated disclaimer, product overview, chapter “Overview”, block diagram. Formal changes.

1.3 Use of Symbols

Symbol	Description
	**Note** Indicates important information for the proper use of the product. Non-observance can lead to errors.
	**Attention** Indicates important notes that, if not observed, can put the product’s functionality at risk.
⇨ [chapter number] [chapter title]	**Cross reference** Indicates cross references within the document. **Example:** Description of the symbols used in this document ⇨ 1.3 Use of Symbols.

1.4 Related Documents

For related documents please refer to the Panasonic website ⇨ 7.2.2 Product Information.

2 Overview

The PAN9028 is a dual band 2.4 GHz and 5 GHz 802.11 a/b/g/n/ac Wi-Fi radio module with integrated Bluetooth BR/EDR/Low Energy (LE), specifically designed for highly integrated and cost-effective applications. The simultaneous and independent operation of the two standards enables very high data rates (802.11ac) and low-power operation (Bluetooth LE). Integrated power management, a fast dual-core CPU, 802.11i security standard support, and high-speed data interfaces deliver the performance for the speed, reliability, and quality requirements of next generation products. Tx power calibration data, Wi-Fi, and Bluetooth system parameters are pre-stored on the one-time-programmable memory of the PAN9028 during production at Panasonic. This simplifies passing the certification process for PAN9028 customers. Furthermore, the module reduces design, test, and calibration effort resulting in reduced time-to-market compared to discrete solutions.

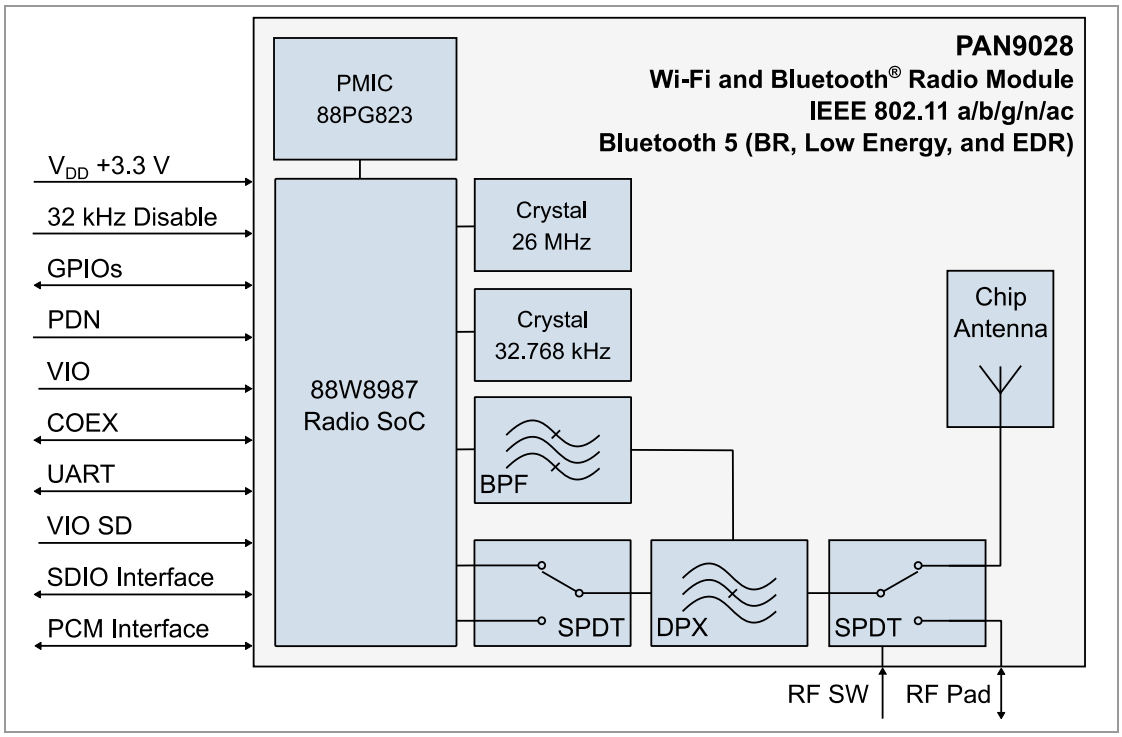
Integrating Wi-Fi and Bluetooth wireless connectivity allows high throughput applications for industrial devices and appliances. The combination of Wi-Fi and Bluetooth provides the highest flexibility for connectivity.

For related documents please refer to ⇨ 7.2.2 Product Information.

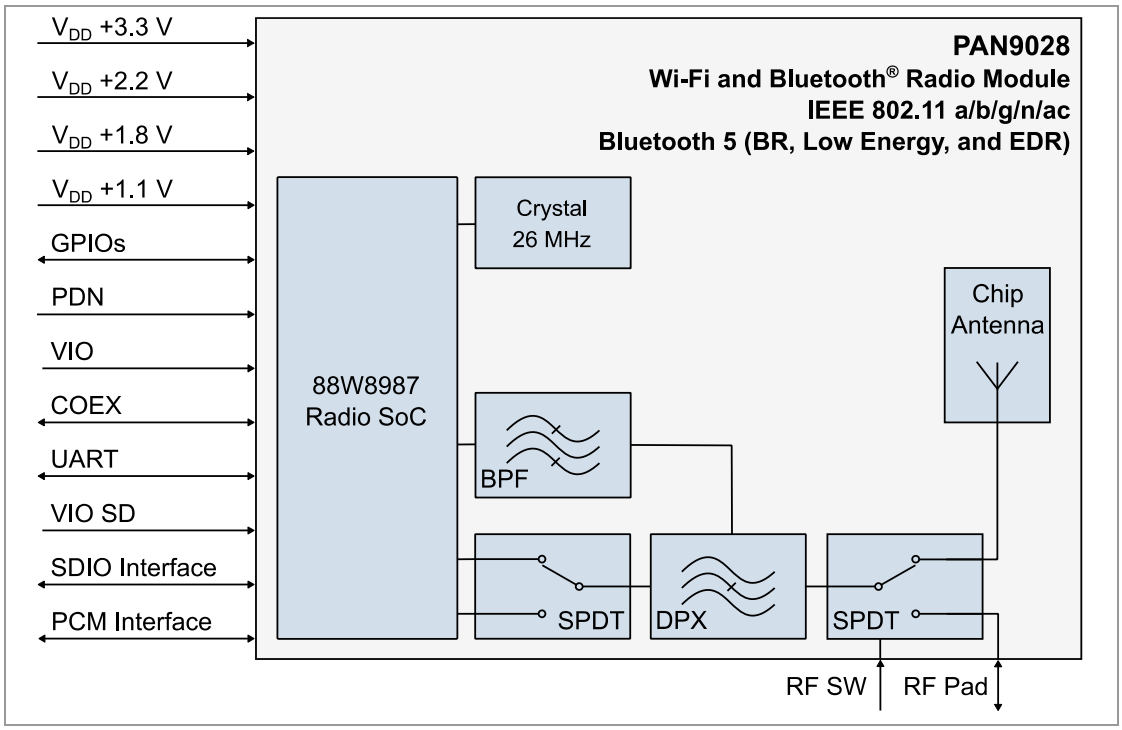
For further information on the variants and versions please refer to ⇨ 7.1 Ordering Information.

2.1 Block Diagram

For Module Variant ENWF940[x]A1EF:



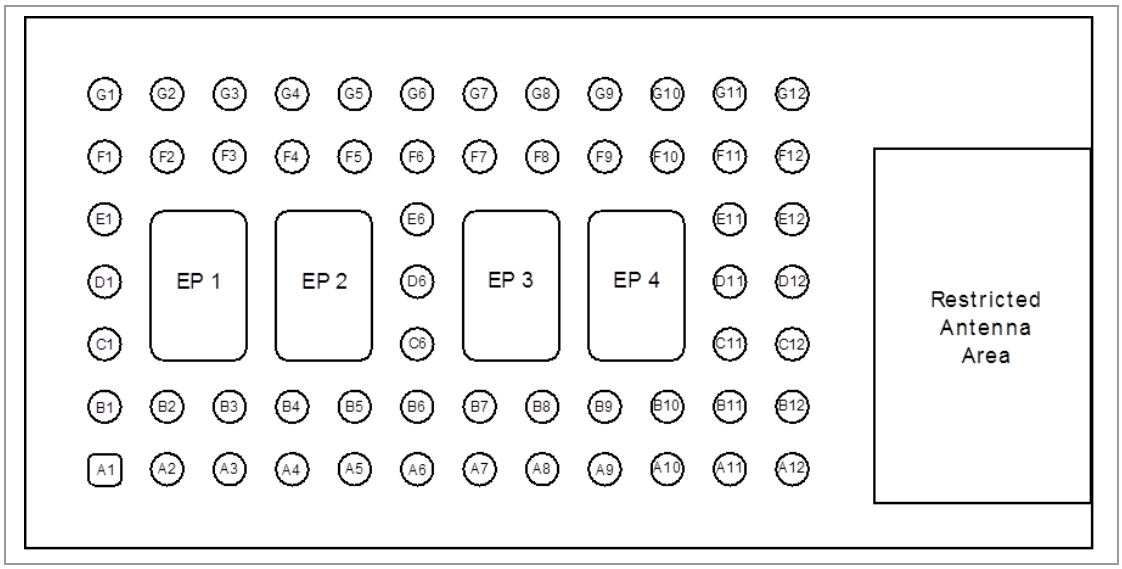
For Module Variant ENWF940[x]A2EF:



2.2 Pin Configuration

Pin Assignment

Top View



Pin Functions for Module Variant ENWF940[x]A1EF

No.	Pin Name	Pin Type	Description
A1	GND	Ground pin	Connect to ground
A2	PMIC_EN	Input signal	Power down of the PMIC, active-low
A3	V_{OUT1V1}	Power	+1.1 V power supply output, only for internal supply
A4	IO14[3]	Digital I/O	General Purpose I/O – GPIO [14]
A5	DNC	NC	Do not connect
A6[1]	UART_CTS[2]	Input signal	Clear-to-send input from peripheral device
	IO10[3]	Digital I/O	General Purpose I/O – GPIO [10]
A7[1]	UART_RTS	Output signal	Request-to-send output to peripheral device
	IO11[3]	Digital I/O	General Purpose I/O – GPIO [11]
A8[1]	UART_SIN	Input signal	Serial data input to peripheral device
	IO9[3]	Digital I/O	General Purpose I/O – GPIO [9]

[1] Multi-purpose pins: After the firmware download, the pins (GPIO, Serial Interface, RF control) are programmed in functional mode with dedicated functionality.

[2] UART mode: After the dedicated firmware download, the pin is used as Host Controller Interface (HCI) for Bluetooth.

[3] GPIO Mode: After the dedicated firmware download, the pin is used as Multi-Purpose Interface.

No.	Pin Name	Pin Type	Description
A9	DNC	NC	Do not connect
A10	IO20[3]	Digital I/O	General Purpose I/O – GPIO [20]
A11	RF_SW2	Input signal	RF Switch Pin 2 – logical voltage level to activate on-board antenna of RF Pad ⇨ RF-Switch Pin Function
A12	GND	Ground pin	Connect to ground
B1	PG1	Output signal	+1.1 V Power Good Output (float when not used) ⇨ 4.9 Power Good
B2	IO1[3]	Digital I/O	General Purpose I/O – GPIO [1]
B3	32KHZ_EN	Input signal	Disable internal 32.768 kHz crystal oscillator for LP modes (100 Ω to GND)
B4	IO0[3]	Digital I/O	General Purpose I/O – GPIO [0]
B5	DNC	NC	Do not connect
B6[1]	UART_DSR	Input signal	Data set ready from peripheral device
	IO12[3]	Digital I/O	General Purpose I/O – GPIO [12]
B7[1]	UART_DTR	Output signal	Data terminal ready to peripheral device
	IO13[3]	Digital I/O	General Purpose I/O – GPIO [13]
B8[1]	UART_SOUT	Output signal	Serial data output to peripheral device
	IO8[3]	Digital I/O	General Purpose I/O – GPIO [8]
B9	IO15[3]	Digital I/O	General Purpose I/O – GPIO [15]
B10[1]	COEX_OUT	Output signal	Serial data output to MWS modem or peripheral device
	IO17[3]	Digital I/O	General Purpose I/O – GPIO [17]
B11	RF_SW1	Input signal	RF Switch Pin 1 – logical voltage level to activate on-board antenna of RF Pad ⇨ RF-Switch Pin Function
B12	GND	Ground pin	Connect to ground
C1	PGLDO	Output signal	+1.8 V Power Good Output (float when not used) ⇨ 4.9 Power Good
C6	CNTL2	Input signal	Do not connect
C11	GND	Ground pin	Connect to ground
C12	GND	Ground pin	Connect to ground
D1	PG2	Output signal	+2.2 V Power Good Output (float when not used) ⇨ 4.9 Power Good
D6	CNTL0	Input signal	Keep open (DNC) if using SDIO interface for Bluetooth or connect with 100 kΩ to GND if using UART interface for Bluetooth ⇨ Control Pin Function.
D11	GND	Ground pin	Connect to ground
D12	GND	Ground pin	Connect to ground

No.	Pin Name	Pin Type	Description
E1[1]	PCM_CLK	Input/Output	PCM clock signal, output if PCM master, input if PCM slave
	IO6[3]	Digital I/O	General Purpose I/O – GPIO [6]
E6	DNC	NC	Do not connect
E11	GND	Ground pin	Connect to ground
E12	GND	Ground pin	Connect to ground
F1	GND	Ground pin	Connect to ground
F2	V_{DD3V3}	Power	+3.3 V power supply connection
F3	V_{DD3V3}	Power	+3.3 V power supply connection
F4	V_{IOSD}	Power	+1.8 V or +3.3 V Digital I/O SDIO power supply
F5[1]	COEX_SIN	Input signal	Serial data input from MWS modem or peripheral device
	IO16[3]	Digital I/O	General Purpose I/O – GPIO[16]
F6[1]	PCM_SYNC	Input/Output	PCM Sync Pulse signal, output if PCM master, input if PCM slave
	IO7[3]	Digital I/O	General Purpose I/O – GPIO [7]
F7[1]	PCM_DOUT	Output signal	PCM data output signal
	IO5[3]	Digital I/O	General Purpose I/O – GPIO [5]
F8[1]	LED_WLAN	Output pin	WLAN activity LED control
	IO2[3]	Digital I/O	General Purpose I/O – GPIO [2]
F9[1]	LED_BT	Output pin	Bluetooth activity LED control
	IO3[3]	Digital I/O	General Purpose I/O – GPIO [3]
F10[1]	PCM_DIN	Input signal	PCM data input signal
	IO4[3]	Digital I/O	General Purpose I/O – GPIO [4]
F11	GND	Ground pin	Connect to ground
F12	GND	Ground pin	Connect to ground
G1	V_{OUT2V2}	Power	+2.2 V power supply output, only for internal supply
G2	V_{OUT2V2}	Power	+2.2 V power supply output, only for internal supply
G3	V_{IO}	Power	+1.8 V or +3.3 V power supply for General Purpose I/O and UART
G4	V_{OUT1V8}	Power	+1.8 V power supply output, only for internal supply
G5	SD_CLK	Digital I/O	For SDIO specific terminals please refer to ⇨ SDIO Pin Functions.
G6	SD_CMD	Digital I/O	
G7	SD_DAT0	Digital I/O	
G8	SD_DAT1	Digital I/O	
G9	SD_DAT2	Digital I/O	
G10	SD_DAT3	Digital I/O	

No.	Pin Name	Pin Type	Description
G11	GND	Ground pin	Connect to ground
G12	RF_OUT	RF port	50 Ω bottom pad to be activated by RF_SW1/RF_SW2 control voltage ⇨ RF-Switch Pin Function.
EP1	EPAD1	Thermal pin	Connect to ground
EP2	EPAD2	Thermal pin	Connect to ground
EP3	EPAD3	Thermal pin	Connect to ground
EP4	EPAD4	Thermal pin	Connect to ground

The V_{OUT1V1}, V_{OUT1V8} and V_{OUT2V2} power supply pins are only for internal purpose. V_{OUT1V8} may be used to power V_{IO}/V_{IOSD} of the module.
Do not use them to power external curcuits.

Pin Functions for Module Variant ENWF940[x]A2EF

No.	Pin Name	Pin Type	Description
A1	GND	Ground pin	Connect to ground
A2	DNC	NC	Do not connect
A3	V_{DD1V1}	Power	+1.1 V power supply connection
A4	IO14[3]	Digital I/O	General Purpose I/O – GPIO [14]
A5	DNC	NC	Do not connect
A6[1]	UART_CTS[2]	Input signal	Clear-to-send input from peripheral device
	IO10[3]	Digital I/O	General Purpose I/O – GPIO [10]
A7[1]	UART_RTS	Output signal	Request-to-send output to peripheral device
	IO11[3]	Digital I/O	General Purpose I/O – GPIO [11]
A8[1]	UART_SIN	Input signal	Serial data input to peripheral device
	IO9[3]	Digital I/O	General Purpose I/O – GPIO [9]
A9	DNC	NC	Do not connect
A10	IO20[3]	Digital I/O	General Purpose I/O – GPIO [20]
A11	RF_SW2	Input signal	RF Switch Pin 2 – logical voltage level to activate on-board antenna of RF Pad ⇨ RF-Switch Pin Function.
A12	GND	Ground pin	Connect to ground
B1	DNC	NC	Do not connect
B2	IO1[3]	Digital I/O	General Purpose I/O – GPIO [1]
B3	DNC	NC	Do not connect

No.	Pin Name	Pin Type	Description
B4	IO0[3]	Digital I/O	General Purpose I/O – GPIO [0]
B5	PDn	Input signal	Power Down. Low active
B6[1]	UART_DSR	Input signal	Data set ready from peripheral device
	IO12[3]	Digital I/O	General Purpose I/O – GPIO [12]
B7[1]	UART_DTR	Output signal	Data terminal ready to peripheral device
	IO13[3]	Digital I/O	General Purpose I/O – GPIO [13]
B8[1,4]	UART_SOUT	Output signal	Serial data output to peripheral device
	IO8[3]	Digital I/O	General Purpose I/O – GPIO [8]
B9[1]	IO15[3]	Digital I/O	General Purpose I/O – GPIO [15]
B10[1]	COEX_OUT	Output signal	Serial data output to MWS modem or peripheral device
	IO17[3]	Digital I/O	General Purpose I/O – GPIO [17]
B11	RF_SW1	Input signal	RF Switch Pin 1 – logical voltage level to activate on-board antenna of RF Pad ⇨ RF-Switch Pin Function.
B12	GND	Ground pin	Connect to ground
C1	DNC	NC	Do not connect
C6	CNTL2	Input signal	Connect this pin (with 50 kΩ to 100 kΩ) to GND
C11	GND	Ground pin	Connect to ground
C12	GND	Ground pin	Connect to ground
D1	DNC	NC	Do not connect
D6	CNTL0	Input signal	Keep open (DNC) if using SDIO interface for Bluetooth or connect with 100 kΩ to GND if using UART interface for Bluetooth ⇨ Control Pin Function.
D11	GND	Ground pin	Connect to ground
D12	GND	Ground pin	Connect to ground
E1[1]	PCM_CLK	Input/Output	PCM clock signal, output if PCM master, input if PCM slave
	IO6[3]	Digital I/O	General Purpose I/O – GPIO [6]
E6	DNC	NC	Do not connect
E11	GND	Ground pin	Connect to ground
E12	GND	Ground pin	Connect to ground
F1	GND	Ground pin	Connect to ground
F2	V_{DD3V3}	Power	+3.3 V power supply connection
F3	V_{DD3V3}	Power	+3.3 V power supply connection

[4] Keep this pin open until firmware initialization or reset is finished. The definition of this pin changes immediately after firmware initialization or reset to its usual function

No.	Pin Name	Pin Type	Description
F4	V_{IOSD}	Power	+1.8 V or +3.3 V Digital I/O SDIO power supply
F5[1]	COEX_SIN	Input signal	Serial data input from MWS modem or peripheral device
	IO16[3]	Digital I/O	General Purpose I/O – GPIO [16]
F6[1]	PCM_SYNC	Input/Output	PCM Sync Pulse signal, output if PCM master, input if PCM slave
	IO7[3]	Digital I/O	General Purpose I/O – GPIO [7]
F7[1]	PCM_DOUT	Output signal	PCM data output signal
	IO5[3]	Digital I/O	General Purpose I/O – GPIO [5]
F8[1]	LED_WLAN	Output pin	WLAN activity LED control
	IO2[3]	Digital I/O	General Purpose IO – GPIO [2]
F9[1]	LED_BT	Output pin	Bluetooth activity LED control
	IO3[3]	Digital I/O	General Purpose I/O – GPIO [3]
F10[1]	PCM_DIN	Input signal	PCM data input signal
	IO4[3]	Digital I/O	General Purpose I/O – GPIO [4]
F11	GND	Ground pin	Connect to ground
F12	GND	Ground pin	Connect to ground
G1	V_{DD2V2}	Power	+2.2 V power supply connection
G2	V_{DD2V2}	Power	+2.2 V power supply connection
G3	V_{IO}	Power	+1.8 V or +3.3 V power supply for General Purpose I/O and UART
G4	V_{DD1V8}	Power	+1.8 V power supply connection
G5	SD_CLK	Digital I/O	For SDIO specific terminals please refer to ⇨ SDIO Pin Functions.
G6	SD_CMD	Digital I/O	
G7	SD_DAT0	Digital I/O	
G8	SD_DAT1	Digital I/O	
G9	SD_DAT2	Digital I/O	
G10	SD_DAT3	Digital I/O	
G11	GND	Ground pin	Connect to ground
G12	RF_OUT	RF port	50 Ω bottom pad to be activated by RF_SW1/RF_SW2 control voltage ⇨ RF-Switch Pin Function.
EP1	EPAD1	Thermal pin	Connect to ground
EP2	EPAD2	Thermal pin	Connect to ground
EP3	EPAD3	Thermal pin	Connect to ground
EP4	EPAD4	Thermal pin	Connect to ground

SDIO Pin Functions for all Module Variants

No.	Pin Name	Pin Type	Description	
			4-Bit Mode	1-Bit Mode
G5	SD_CLK	Digital I/O	Clock	Clock
G6	SD_CMD	Digital I/O	Command Line	Command Line
G7	SD_DAT0	Digital I/O	Data Line bit [0]	Data Line
G8	SD_DAT1	Digital I/O	Data Line bit [1] or Interrupt (optional)	Interrupt
G9	SD_DAT2	Digital I/O	Data Line bit [2] or Read Wait (optional)	Read Wait (optional)
G10	SD_DAT3	Digital I/O	Data Line bit [3]	Not used

RF-Switch Pin Functions for all Module Variants

No.	Pin Name	Pin Type	Logical Level for Activation	
			On-Board Chip Antenna	RF OUT Pin
B11	RF_SW1	Input signal	GND (0 V)	3.0 V to 3.6 V (typ. 3.3 V)
A11	RF_SW2	Input signal	3.0 V to 3.6 V (typ. 3.3 V)	GND (0 V)

Control Pin Function for all Module Variants

The control pin is used as configuration input to set parameters following a reset. The definition of the pin changes immediately after a reset to its usual function. To set a configuration bit to “02, attach a 50 kΩ to 100 kΩ resistor from the pin to ground. No external circuitry is required to set a configuration bit to “1”.

The configuration of the control pin is used for the firmware boot option. The software reads and boots accordingly.

No.	Pin Name	Pin Type	Strap Value	WLAN	Bluetooth/ Bluetooth LE	Firmware Download		Number SDIO Functions
						Type	Mode	
D6	CNTL0	Input Signal	0	SDIO	UART	SDIO+UART	Parallel/Serial	1 (WLAN)
			1	SDIO	SDIO	SDIO+SDIO	Parallel/Serial	2 (WLAN, Bluetooth)

2.3 Host Interface

The bus interface connects several host interface bus units to the CPU bus of the device through the internal bus. The connection of each unit is multiplexed with other bus units.

The high-speed UART interface is connected to the CPU bus through a separate bus.

Type	Features
High-speed UART interface	The device supports a high-speed Universal Asynchronous Receiver/Transmitter (UART) interface, compliant with the industry standard 16550 specification. • FIFO mode permanently selected for transmit and receive operations • Two pins for transmit and receive operations • Two flow control pins • Interrupt triggers for low-power, high throughput operation
SDIO interface	The device supports an SDIO device interface that conforms to the industry standard SDIO full-speed card specification and allows a host controller using the SDIO bus protocol to access the device. • Supports SDIO 3.0 Standard • 1-bit SDIO or 4-bit SDIO transfer modes with full clock range up to 208 MHz • On-chip memory used for CIS • Special interrupt register for information exchange • Allows card to interrupt host

For further information please refer to ⇨ 4.10.1 Host Interface.

2.4 Peripheral Bus Interfaces

The Peripheral Bus Unit (PBU) connects several low speed peripherals to the internal bus of the device. The device consists of the GPIO Interface and the One Time Programmable Memory (OTP).

Type	Features
General Purpose I/O (GPIO) Interface	• User-defined GPIOs (each configured to either input or output) • Each GPIO controlled independently • Each I/O configurable to output bit from GPIO_OUT
One Time Programmable Memory (OTP)	• Storing device-specific calibration data and hardware information like MAC/BD address, WLAN, and Bluetooth parameters • Programmed during production process of device • Device performs calibration when it is powered up

For further information please refer to ⇨ 4.10.2 Peripheral Interface.

2.5 PCM Interfaces

The device supports the PCM interface.

Type	Features
PCM Interface	• Master or slave mode • PCM bit width size of 8 bits or 16 bits • Up to four slots with configurable bit width and start positions • Short frame and long frame synchronization

For further information please refer to ⇨ 4.10.3 Audio Interface.

2.6 Coexistence

The implemented coexistence framework is based on the IEEE 802.15.2 recommended practice Packet Traffic Arbitration (PTA) scheme and the Bluetooth Special Interest Group (Bluetooth) Core Specification Volume 7 (Wireless Coexistence Volume).

2.6.1 WLAN and Bluetooth Channel Information Exchange

Since Bluetooth and IEEE 802.11b/g/n WLAN use the same 2.4 GHz frequency band, each can cause interference with the other. The level of interference depends on the respective frequency channel used by Bluetooth and WLAN (other factors can impact interference, like Tx power and Rx sensitivity of the device).

In a system with both Bluetooth and WLAN, the common host receives information about WLAN channel usage and passes the information to the Bluetooth device. For Bluetooth 1.2 devices with Adaptive Frequency Hopping (AFH) enabled, the Bluetooth device can block channel usage that overlaps the WLAN channel in use.

When the Bluetooth device avoids all channels used by the WLAN, the impact of interference is reduced, but not completely eliminated. For Bluetooth 1.1 devices, the Bluetooth device cannot block WLAN channel usage. In this case, a Bluetooth Coexistence Arbiter (BCA) scheme at MAC level is required. The BCA scheme can also be used with Bluetooth 1.2 devices to further reduce the impact of interference to a minimum.

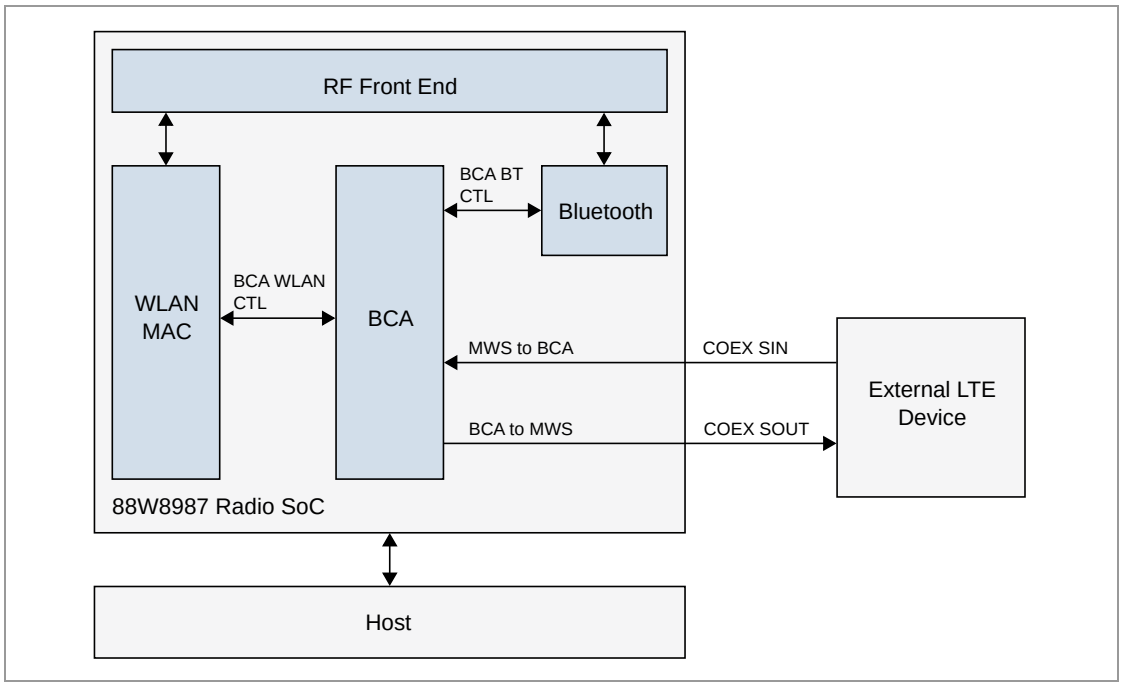
2.6.2 External Mobile Wireless System (LTE or ZigBee) and BCA Exchange

Based on the Bluetooth SIG Wireless Coexistence Volume, the device supports a Wireless Coexistence Interface 2 (WCI-2) protocol for WLAN/Bluetooth coexistence with an external Mobile Wireless System (MWS), such as a Long Term Evolution (LTE) or ZigBee device.

WCI-2 is a 2-wire transport interface. An internal coexistence is used to exchange request/grant with the BCA.

2.6.3 System Configuration

External MWS Device



2.6.4 WCI-2 Interface

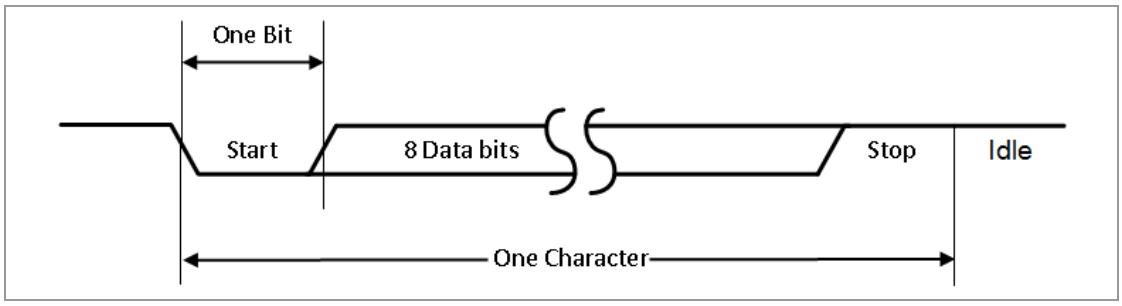
The coexistence interface includes a Mobile Wireless System (MWS) transport controller to accommodate a 2-wire, UART-based serial transport interface. This interface is a standard full-duplex UART (TxD and RxD) carrying logical signals framed as UART characters. In addition, it allows support of multiple logical channels.

Interface Signals

Pin No.	Signal Name	Specification Name	Pin Type	Description
F5	COEX_SIN	RxD	Input	Serial data from external MWS device
B10	COEX_SOUT	TxD	Output	Serial data to external MWS device

Signal Waveform Format

The messaging is based on a standard UART format. The UART signals should be connected like a null-modem. For example, the local TxD connected to the remote RxD and vice versa.



Interface Transport Settings

Item	Range	Comment
Baudrate	921 600 ~ 4 000 000	Baud
Data Bits	8	LSB first
Parity Bits	0	No parity
Stop Bit	1	One stop bit
Flow Control	No	No flow control

Support Baud Rates

Baud			
921 600	2 000 000	3 000 000	4 000 000

Real-Time Signaling Message

The real-time signaling message is used to transport real-time signals over the 2-wire transport interface.

The real-time signaling message conveys the real-time signals (Bluetooth Core Specification, Volume 7, Part A) in one message. The time reference point for the real-time signaling message is the end of message bit 5 (transition to stop bit).

Defined real-time signaling messages include:

- Coexistence Controller to MWS device
- MWS device to Coexistence Controller

Real-Time Signaling	MSG [0]	MSG [1]	MSG [2]	MSG [3]	MSG [4]
MWS to Coexistence Controller (Signal)	FRAME_SYNC	MWS_RX	MWS_TX	PATTERN [0]	PATTERN [1]
Coexistence Controller to MWS (Message)	BLUETOOTH _RX_PRI	BLUETOOTH _TX_ON	802_RX_PRI	802_TX_ON	RFU

Signal Name
FRAME_SYNC
MWS_RX
MWS_TX
PATTERN [1, 0]
BT_RX_PRI
BT_TX_ON
802_RX_PRI
802_TX_ON
MWS_INACTIVITY_DURATION
MWS_SCAN_FREQUENCY_OFFSET

Transport Control Message

The transport control messages can modify the state and request state information of the MWS coexistence interface.

Message	MSG [0]	MSG [1]	MSG [2]	MSG [3]	MSG [4]
Transport Control Message	RESEND_REAL_TIME	RFU	RFU	RFU	RFU

Signal Name	Description
RESEND_REAL_TIME	This bit is set if a device wants to get a status update of the real-time signals. The signal is usually used after wake-up from sleep of the transport interface to get an update of the real-time signals. If the receiving device's transport interface is awake it shall send a real-time message with the current status of the real-time signals within 4 UART character period. If the signal is not transmitted within 4 UART character periods, the device is considered asleep. If the receiving device's transport interface is not awake it shall not send a real-time message. **Bluetooth initiated:** If the MWS is currently scanning or has an ongoing inactivity duration, the MWS shall send a frequency scan message or an inactivity duration message after transmitting the real-time message. If the receiving device's transport interface is not awake it shall not send a frequency scan or inactivity duration message.

Transparent Data Message

The transparent control messages can modify the state and request state information of the MWS coexistence interface.

Message	MSG [0]	MSG [1]	MSG [2]	MSG [3]	MSG [4]
Transparent Data Message	NIBBLE_POSITION	DATA [0]/[4]	DATA [1]/[5]	DATA [2]/[6]	DATA [3]/[7]

Signal Name	Description
NIBBLE_POSITION	0 = least significant nibble 1 = most significant nibble
DATA[n]; n=0 .. 7	Data bits of the message octet

MWS Inactivity Duration Message

The inactivity duration messages is used to send the MWS_INACTIVITY_DURATION signal from the MWS device to the Coexistence Controller.

Message	MSG [0]	MSG [1]	MSG [2]	MSG [3]	MSG [4]
MWS Inactivity Duration Message	DURATION [0]	DURATION [1]	DURATION [2]	DURATION [3]	DURATION [4]

The idle duration is encoded in 5 bits given by the formula:

$$\text{Inactivity\_Duartion} = \text{DURATION} \cdot 5\,\text{ms}$$

Inactivity durarations smaller than 5 ms are not communicated.

If all bits are set to “1” the inactivity duration is infinite. If all bits are set to “0” or MWS_RX or MWS_TX are set to “1”, the inactivity period ends.

MWS Scan Frequency Offset Message

The MWS scan frequency offset message is used to send the MWS_SCAN_FREQUENCY_ OFFSET signal from the MWS device to the Coexistence Controller.

Message	MSG [0]	MSG [1]	MSG [2]	MSG [3]	MSG [4]
MWS Scan Frequency Offset	BAND	FREQ [0]	FREQ [1]	FREQ [2]	FREQ [3]

The RF scan frequency is encoded in 5 bits given by the formula:

$$\text{RF\_FREQ\_OFFSET} = \text{FREQ} \cdot 10\,\text{MHz}$$

If BAND is set to “0” the RF_FREQ_OFFSET is the negative value from the lower edge of the ISM band and if BAND is set to “1”, RF_FREQ_OFFSET is the positive value from the top edge of the ISM band.

FREQ set to all “0” indicates the end of the scan period.

2.6.5 Bluetooth Coexistence Arbiter

Type	Features

Type	Features
Capability	• Programmable coexistence interface timing, interface modes, and signal polarity to support a variety of external Bluetooth devices • Programmable decision policies and transaction lock behavior for various use cases • Interface with external or on-chip Bluetooth device • Support Bluetooth 1.1 or Bluetooth 1.2 AFH • WLAN-/Bluetooth-coordinated low-power design • Enhanced information sharing between WLAN and Bluetooth for combo systems • WLAN/Bluetooth/MWS (LTE or ZigBee) coexistence support
Arbitration	• Contention resolved by a customizable decision matrix that allows independent grant decision for each device • Vectors for the decision matrix: – WLAN priority (2-bit) – WLAN direction – Bluetooth priority (1-bit or 2-bit) – Bluetooth direction – Bluetooth frequency in/out band – MWS priority (2-bit) – MWS direction
AFH	If AFH is enabled in the Bluetooth device, and there is a sufficient guard-band outside the WLAN operating frequency, the Bluetooth device uses the Out-Of-Band (OOB) channel with respect to the WLAN device. Otherwise, the Bluetooth device uses the In-Band (IB) and OOB channels with respect to the WLAN device. The IB and OOB information is either provided by the Bluetooth device through the coexistence interface, or it can be provided through firmware controls in a shared-host system. IB/OOB is a vector in the decision matrix.
Decision Policies	System configuration is a major consideration when planning decision policies. The configuration governs how RF paths are shared and how much interference will occur. Interference combinations include: – WLAN Tx and Bluetooth Tx – WLAN Tx and Bluetooth Rx – WLAN Rx and Bluetooth Tx – WLAN Rx and Bluetooth Rx
	Interference combinations where WLAN and Bluetooth share the same antenna: – WLAN Tx and Bluetooth Tx share same antenna, the decision matrix allows either WLAN or Bluetooth Tx (both OOB and IB), based on relative packet priorities. – WLAN Tx and Bluetooth Rx (both OOB and IB) have sizable interference impacts on Bluetooth Rx, the decision matrix grants or denies WLAN Tx based on relative packet priorities. – WLAN Rx and Bluetooth Tx (both OOB and IB) have sizable interference impacts on WLAN Rx, the decision matrix grants or denies Bluetooth Tx based on relative packet priorities. – WLAN Rx and Bluetooth Rx (both OOB and IB) have no impact on each other, the decision matrix grants both.

Type	Features
	Interference combinations where WLAN and Bluetooth have their own antenna: – WLAN Tx and Bluetooth Tx in OOB situation have little interference impact on each other, the decision matrix grants both. – WLAN Tx and Bluetooth Tx in IB have sizable interference impact on each other, the decision matrix allows either WLAN or Bluetooth Tx, based on relative packet priorities. – WLAN Tx and Bluetooth Rx in OOB situation have little interference impact on each other, the decision matrix grants both provided there is enough antenna isolation between WLAN and Bluetooth antenna. – WLAN Tx and Bluetooth Rx in IB situation have sizable interference impact on Bluetooth Rx, the decision matrix grants or denies WLAN Tx based on relative packet priorities. – WLAN Rx and Bluetooth Tx in OOB situation have little interference impact on each other, the decision matrix grants both provided there is enough antenna isolation between WLAN and Bluetooth antenna. – WLAN Rx and Bluetooth Tx in IB situation have sizable interference impact on WLAN RX, the decision matrix grants or denies Bluetooth Tx based on relative packet priorities. – WLAN Rx and Bluetooth Rx (both OOB and IB) have no impact on each other, the decision matrix grants both.
Decision Policies (continued)	For the devices running in a basic shared antenna configuration, the linear switching imposes restrictions on simultaneous transfer. Reasonable policies include: – WLAN and Bluetooth are never granted at the same time – Decision matrix grants a device based on relative packet priorities and direction – Priority order: High > Medium High > Medium > Low – For equal priority contention, select one device to win, that optimizes the usage case For the devices running in an enhanced shared antenna configuration, the linear switching imposes restrictions on some simultaneous transfers.
Transaction Stopping	The arbiter allows control of what transfers can be stopped after an initial grant. If allowed, a transaction can be stopped for higher priority request. A transaction stop decision is a function of the decision policies and transaction stopping control. The transaction stopping control is configurable per device and direction.

2.6.6 Bluetooth Capability

Type	Features
Request Schemes	The PTA signals are directly controlled by the hardware to meet timing requirements of the Bluetooth radio. The software controls the type of traffic in priority mode. Mechanisms enforced for control include: • Selection of certain types of communication always treated as high priority • Selection of individual frames marked with high priority • Real-time signaling of the next slot marked with high priority • Automatic hardware control based on the grant/denial history of the Bluetooth link
Timing Control	The PTA signal timing scheme is fully programmable relative to the Bluetooth packet timing.

2.6.7 WLAN Capability

Type	Features
Capability	The WLAN device technology uses an internal coexistence interface to exchange request/grant with the BCA. Features: • Packet-based request signaling with direction and priority information • 1-bit or 2-bit priority signaling to support 4 priority levels • Multiple WLAN Rx request trigger sources, including early prediction • WLAN Tx request cancellation and abort if grant denied or revoked in middle of request • 802.11n A-MPDU treated as single packet
Packet Classification	• Programmable mask allows each frame type to be mapped to a priority • Default setting puts response frames (ACK), beacons, and QoS frames as high priority • WLAN Tx and Rx have separate priority masks
Queue Classification	• Programmable mask allows each transmit queue to be mapped to a priority • Queue-based mapping is optional for software-generated frames only

2.6.8 LTE (MWS) Capability

The device supports a Bluetooth SIG WCI-2 MWS coexistence signaling interface. The coexistence logical signaling is designed to enable a standard interface to allow an MWS device and a Coexistence Controller to exchange information and support cooperative coexistence.

The WCI-2 signals carry time-critical information such as the start point of an MWS frame. The logical coexistence signaling architecture also includes transparent data messaging and vendor specific data messaging mechanism to enable passing information to and from the collocated MWS device and Coexistence Controller when long latency (tens of milliseconds) cannot be tolerated.

For further information please refer to ⇨ 2.6.4 WCI-2 Interface.

Coexistence Signals

The logical signals assist in time alignment, protecting MWS from interference and maximizing the usability of the Bluetooth radio.

Time-Critical Coexistence Signals

Signal Name	Direction
FRAME_SYNC	MWS to Bluetooth
BT_RX_PRI	Bluetooth to MWS
BT_TX_ON	Bluetooth to MWS
802_RX_PRI	Bluetooth to MWS
802_TX_ON	Bluetooth to MWS
MWS_PATTERN	MWS to Bluetooth
MWS_RX	MWS to Bluetooth
MWS_TX	MWS to Bluetooth
MWS_INACTIVITY_DURATION	MWS to Bluetooth
MWS_SCAN_FREQUENCY_OFFSET	MWS to Bluetooth
MWS_TX_PRIL (MWS TX Priority Level)	MWS to Bluetooth
MWS_RX_PRIL (MWS RX Priority Level)	MWS to Bluetooth

2.6.9 ZigBee (MWS) Coexistence Capability

ZigBee is based on the IEEE 802.15.4 standard and it is used by a suite of communication protocols to create Personal Area Networks (PANs) supporting home automation, lighting control, etc. ZigBee radios operate in the 2.4 GHz ISM band worldwide. Unlike Bluetooth, the ZigBee specification does not use AFH. When coexisting with WLAN/Bluetooth in the 2.4 GHz band, it is important to avoid co-channel (IB) operation of these radios.

The device re-uses the MWS coexistence interface to support ZigBee coexistence. The coexistence logical signaling is used to allow a ZigBee device and a WLAN/Bluetooth combo device to exchange information and support cooperative coexistence.

Coexistence Signals

The logical signals used for ZigBee and WLAN/Bluetooth coexistence are a subset of the LTE coexistence signaling. Considering the lower data rate of ZigBee packets, a lower baud rate may be chosen for the 2-wire UART physical interface. The BCA supports 3-way arbitration among ZigBee/WLAN/Bluetooth requests.

Coexistence Signals

Signal Name	Direction
MWS_RX	MWS to Bluetooth
MWS_TX	MWS to Bluetooth
MWS_PATTERN	MWS to Bluetooth
MWS_RX_PRI	MWS to Bluetooth
MWS_TX_PRI	MWS to Bluetooth
802_RX_PRI	Bluetooth to MWS
802_TX_ON	Bluetooth to MWS
BT_RX_PRI	Bluetooth to MWS
BT_TX_ON	Bluetooth to MWS

2.7 WLAN

Type	Features
IEEE 802.11/ Standards	• 802.11 data rates 1 Mbps and 2 Mbps (DSSS) • 802.11b data rates 5.5 Mbps and 11 Mbps (CCK) • 802.11a/g data rates 6 Mbps, 9 Mbps, 12 Mbps, 18 Mbps, 24 Mbps, 36 Mbps, 48 Mbps, and 54 Mbps (OFDM) • 802.11b/g performance enhancements • 802.11n/ac with maximum data rates up to 86.7 Mbps (20 MHz channel), 200 Mbps (40 MHz channel), 433 Mbps (80 MHz channel) • 802.11d international roaming • 802.11e quality of service (QoS) • 802.11h transmit power control • 802.11h DFS radar pulse detection • 802.11i enhanced security (WEP, WPA, WPA2) • 802.11k radio resource measurement • 802.11mc precise indoor location and navigation • 802.11n block acknowledgment extension • 802.11r fast hand-off for AP roaming • 802.11u Hotspot 2.0 (STA mode only) • 802.11v TIM frame transmission/reception • 802.11w protected management frames • Support clients (stations) implementing IEEE Power Save mode
WLAN MAC	• Frame exchange at the MAC level to deliver data • Received frame filtering and validation (CRC) • Generation of MAC header and trailer information (MPDUs) • Fragmentation of data frames (MSDUs) • Access mechanism support for fair access to shared wireless medium through: – Distributed Coordination Function (DCF) – Enhanced Distributed Channel Access (EDCA) • A-MPDU aggregation/de-aggregation (supports 802.11ac single-MPDU A-MPDU) • 20 MHz, 40 MHz, and 80 MHz channel coexistence • RIFS burst receive • Management information base • Radio resource measurement • Quality of service • Block acknowledgement • 802.11ac downlink MU-MIMO (receive) • Dynamic frequency selection • TIM frame Tx and Rx • Multiple BSS/Station • Transmit rate adaption • Transmit power control

Type	Features
WLAN Baseband	• 802.11ac 1×1 SISO (WLAN SoC with SISO RF radio) • Backward compatibility with legacy 802.11a/b/g/n technology • WLAN/Bluetooth LNA sharing • PHY data rates up to 433 Mbps • 20 MHz bandwidth/channel, 40 MHz bandwidth/channel, upper/lower 20 MHz bandwidth in 40 MHz channel, and 20 MHz duplicate legacy bandwidth in 40 MHz channel mode operation • 80 MHz bandwidth/channel, 4 positions of 20 MHz bandwidth in 80 MHz channel, upper/lower 40 MHz bandwidth in 80 MHz channel, 20 MHz quadruplicate legacy bandwidth in 80 MHz channel mode operation • Modulation and Coding Scheme – 802.11n: MCS 0 ~ 7 and MCS 32 (duplicate 6 Mbps) – 802.11ac: MCS 0~9 NSTS = 1 • Dynamic frequency selection (radar detection) – Enhanced radar detection for short and long pulse radar – Enhanced AGC scheme for DFS channel – Japan DFS requirement for W53 and W56 • 802.11k Radio resource measurement
	• 802.11n/ac optional features: – 20 MHz, 40 MHz, and 80 MHz coexistence with middle-packet detection (GI detection) for enhancd CCA – Space-Time-Block-Coding (STBC) one spatial stream reception – LDPC transmission and reception for both 802.11n and 802.11ac – 256 QAM (MCS 8, 9) modulation (optional support for 802.11ac MCS 9 in 20 MHz using LDPC) – Short Guard Interval – RIFS on receive path for 802.11n packets – Explicit Beamformee support – 802.11ac multi-user beamformee – 802.11n Greenfield Tx/Rx – MU-PPDUs (receive) • 802.11mc locationing • Power save features
WLAN Radio	• Integrated direct-conversion radio • 20 MHz, 40 MHz, and 80 MHz channel bandwidth • Shared WLAN/Bluetooth receive input scheme for 2.4 GHz band • Rx Path – On-chip gain selectable LNA with optimized noise figure and power consumption – High dynamic range AGC function in receive mode • Tx Path – Internal PA with power control – Optimized Tx gain distribution for linearity and noise performance • Local Oscillator with fine channel step

Type	Features
WLAN Encryption	• WEP 64-bit and 128-bit encryption with hardware TKIP processing (WPA) • AES-CCMP hardware implementation as part of 802.11i security standard (WPA2) • Advanced encryption standard (AES)/Counter-Mode/CBC-MAC Protocol (CCMP) • AES-Cipher-Based Message Authentication Code (CMAC) as part of the 802.11w security standard • WLAN Authentication and Privacy Infrastructure (WAPI)

Operation Modes

Parameter	Operation Mode				Specification
Standard Conformance	IEEE 802.11/IEEE 802.11b				
	IEEE 802.11a				
	IEEE 802.11g				
	IEEE 802.11n				
	IEEE 802.11ac				
Modulation	IEEE 802.11a				OFDM
	IEEE 802.11b				DSSS/CCK
	IEEE 802.11g				OFDM
	IEEE 802.11n				OFDM at MCS0~7 and MCS32 (duplicate 6 Mbps)
	IEEE 802.11ac				OFDM at MCS0~9
Physical layer data rates	IEEE 802.11				1 Mbps, 2 Mbps at DSSS
	IEEE 802.11b				5.5 Mbps, 11 Mbps at DSSS/CCK
Supported data rates	IEEE 802.11g				[6, 9, 12, 18, 24, 36, 48, 54] Mbps
	IEEE 802.11a				[6, 9, 12, 18, 24, 36, 48, 54] Mbps
	IEEE 802.11n	MCS0~7	HT20	LGI	[6.5, 13, 19.5, 26, 39, 52, 58.5, 65] Mbps
				SGI	[7.2, 14.4, 21.7, 28.9, 43.3, 57.8, 65, 72.2] Mbps
			HT40	LGI	[13.5, 27, 40.5, 54, 81, 108, 121.5, 135] Mbps
				SGI	[15, 30, 45, 60, 90, 120, 135, 150] Mbps
	IEEE 802.11ac	MCS0~8	HT20	LGI	[6.5, 13, 19.5, 26, 39, 52, 58.5, 65, 78] Mbps
				SGI	[7.2, 14.4, 21.7, 28.9, 43.3, 57.8, 65, 72.2, 86.7] Mbps
		MCS0~9	HT40	LGI	[13.5, 27, 40.5, 54, 81, 108, 121.5, 135, 162, 180] Mbps
				SGI	[15, 30, 45, 60, 90, 120, 135, 150, 180, 200] Mbps
			VHT80	LGI	[29.3, 58.5, 87.8, 117, 175.5, 234, 263.3, 292.5, 351, 390] Mbps
				SGI	[32.5, 65, 97.5, 130, 195, 260, 292.5, 325, 390, 433.3] Mbps

Parameter	Operation Mode	Specification
Supported bandwidth	IEEE 802.11n	20 MHz, 40 MHz (BW)
	IEEE 802.11ac	20 MHz, 40 MHz, 80 MHz (BW)
Supported channel mode operation	IEEE 802.11n	20 MHz BW/channel, 40 MHz BW/channel, upper/lower 20 MHz BW at 40 MHz channel, 20 MHz duplicate legacy BW at 40 MHz channel
	IEEE 802.11ac	20 MHz BW/channel, 40 MHz BW/channel, 80 MHz BW/channel, upper/lower 20 MHz BW at 40 MHz channel, 20 MHz duplicate legacy BW at 40 MHz channel, 4 positions of 20 MHz BW at 80 MHz channel, upper/lower 40 MHz BW at 80 MHz channel, 20 MHz quadruplicate legacy BW at 80 MHz channel
Supported Guard Interval	IEEE 802.11n	400 ns (SGI), 800 ns (LGI)
	IEEE 802.11ac	400 ns (SGI), 800 ns (LGI)

Channels and Frequencies (without Regulatory Restrictions)

2.4 GHz – IEEE 802.11b/g/n					
20 MHz Channels			40 MHz Channels		
Channel	Frequency	Unit	Channel	Frequency	Unit
1	2 412	MHz	1 to 5	2 422	MHz
2	2 417	MHz	2 to 6	2 427	MHz
3	2 422	MHz	3 to 7	2 432	MHz
4	2 427	MHz	4 to 8	2 437	MHz
5	2 432	MHz	5 to 9	2 442	MHz
6	2 437	MHz	6 to 10	2 447	MHz
7	2 442	MHz	7 to 11	2 452	MHz
8	2 447	MHz			
9	2 452	MHz			
10	2 457	MHz			
11	2 462	MHz			
12	2 467	MHz			
13	2 472	MHz			

5 GHz – IEEE 802.11a/n/ac					
20 MHz Channels			40 MHz Channels		
Channel	Frequency	Unit	Channel	Frequency	Unit
36	5 180	MHz	36 to 40	5 190	MHz
40	5 200	MHz	44 to 48	5 230	MHz
44	5 220	MHz	52 to 56	5 270	MHz

5 GHz – IEEE 802.11a/n/ac					
20 MHz Channels			**40 MHz Channels**		
Channel	**Frequency**	**Unit**	**Channel**	**Frequency**	**Unit**
48	5 240	MHz	60 to 64	5 310	MHz
52	5 260	MHz			
56	5 280	MHz			
60	5 300	MHz			
64	5 320	MHz			
100	5 500	MHz	100 to 104	5 510	MHz
104	5 520	MHz	108 to 112	5 550	MHz
108	5 540	MHz	116 to 120	5 590	MHz
112	5 560	MHz	124 to 128	5 630	MHz
116	5 580	MHz	132 to 136	5 670	MHz
120	5 600	MHz	149 to 153	5 755	MHz
124	5 620	MHz	157 to 161	5 795	MHz
128	5 640	MHz			
132	5 660	MHz			
136	5 680	MHz			
140	5 700	MHz			
149	5 745	MHz			
153	5 765	MHz			
157	5 785	MHz			
161	5 805	MHz			
165	5 825	MHz			

5 GHz – IEEE 802.11a/n/ac					
80 MHz Channels					
Channel	**Frequency**	**Unit**	**Channel**	**Frequency**	**Unit**
36 to 48	5 210	MHz			
52 to 64	5 290	MHz			
100 to 112	5 530	MHz			
116 to 128	5 610	MHz			
132 to 144	5 690	MHz			
149 to 161	5 775	MHz			

5 GHz – IEEE 802.11a/n/ac (India and additional UNII Channels)					
20 MHz Channels			**40 MHz Channels**		
Channel	**Frequency**	**Unit**	**Channel**	**Frequency**	**Unit**
144	5 720	MHz	68 to 72	5 350	MHz
169[5]	5 845	MHz	76 to 80	5 390	MHz
173[5]	5 865	MHz	84 to 88	5 430	MHz
177	5 885	MHz	92 to 96	5 470	MHz
181	5 905	MHz	140 to 144	5 710	MHz
			165 to 169	5 835	MHz
			169 to 173[6]	5 855	MHz
			173 to 177	5 875	MHz

5 GHz – IEEE 802.11a/n/ac (India and additional UNII Channels)					
80 MHz Channels					
Channel	**Frequency**	**Unit**	**Channel**	**Frequency**	**Unit**
68 to 80	5 370	MHz			
84 to 96	5 410	MHz			
165 to 177	5 855	MHz			

2.8 Bluetooth

Type	Features
General	• Supports Bluetooth 5 • Shared LNA for Bluetooth • Digital Audio Interface including PCM interface for voice application • Bluetooth and WLAN coexistence

[5] India channels that can be used in other countries as well.

[6] India use only.

Type	Features
Bluetooth Classic (BR/EDR)	• Bluetooth Classic with Bluetooth Class 1 support • Baseband and radio Basic Rate (BR) and Enhanced Data Rate (EDR) packet types with 1 Mbps (GFSK), 2 Mbps (π/4-DQPSK) and 3 Mbps (8DPSK) • Fully functional Bluetooth baseband with: – Adaptive Frequency Hopping (AFH) – Forward error correction – Header error control – Access code correlation – CRC – Encryption bit stream generation – Whitening • Adaptive Frequency Hopping (AFH) including Packet Loss Rate (PLR) • Interlaced scan for faster connection setup • Simultaneous 7 active ACL connection support • Automatic ACL packet type selection • Full master and slave piconet support
	• Scatternet support • Standard UART and SDIO HCI transport layer • 3 SCO/eSCO links with hardware accelerated audio signal processing and hardware supported PPEC algorithm for speech quality improvement • All standard SCO/eSCO voice coding • All standard pairing, authentication, link key, and encryption operations • Standard Bluetooth power saving mechanism (i.e. hold, sniff modes, and sniff-sub rating) • Enhanced Power Control (EPC) • Channel Quality Driven (CQD) data rate • Wideband Speech (WBS) support (1 WBS link) • Encryption (AES) support • LTE/MWS coexistence • Bluetooth 2.1 to 5.0 Core Specification Support • Packet types – ACL (DM1, DH1, DM3, DH3, DM5, DH5, 2-DH1, 2-DH3, 2-DH5, 3-DH1, 3-DH3, 3-DH5) – SCO (HV1, HC3) – eSCO (EV3, EV4, EV5, 2EV3, 3EV3, 2EV5, 3EV5) • Profile Support – A2DP Source/Sink – AVRCP Target/Controller – HFP Dev/gateway – OPP Server/Client – PAN Traffic – SPP – HID – PBAP

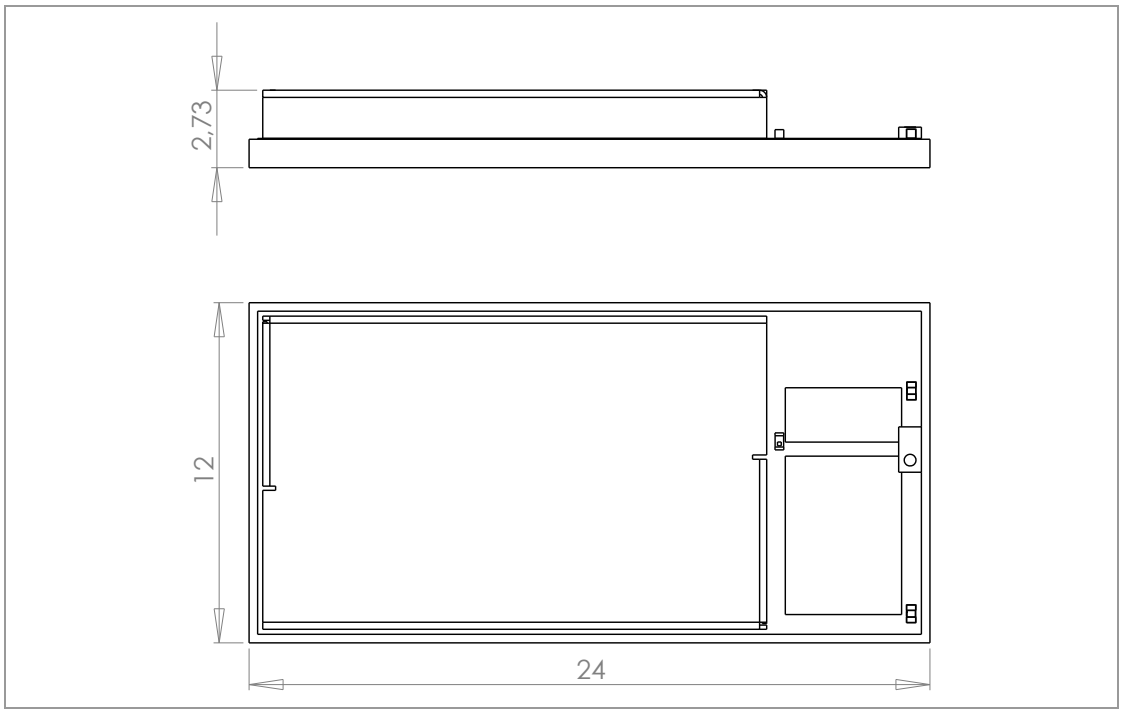
Type	Features
Bluetooth Low Energy (LE)	• Broadcaster, Observer, Central, and Peripheral roles • Supports link layer topology to be master and slave (connects up to 16 links) • Shared RF with BR/EDR • Encryption AES support • Hardware support for intelligent Adaptive Frequency Hopping (AFH) • LE Privacy 1.2 • LE Secure Connection • LE Data Length Extension • LE Advertising Length Extension • High Duty Cycle Directed Advertising • 2 Mbps LE Bluetooth Low Energy 4.0 to 5.0 Support • Direction Finding – Connectionless Angle of Departure (AoD) – Connection-oriented Angle of Arrival (AoA) • Profile Support – GATT – HOGP

3 Detailed Description

3.1 Dimensions

All dimensions are in millimeters.

Top View

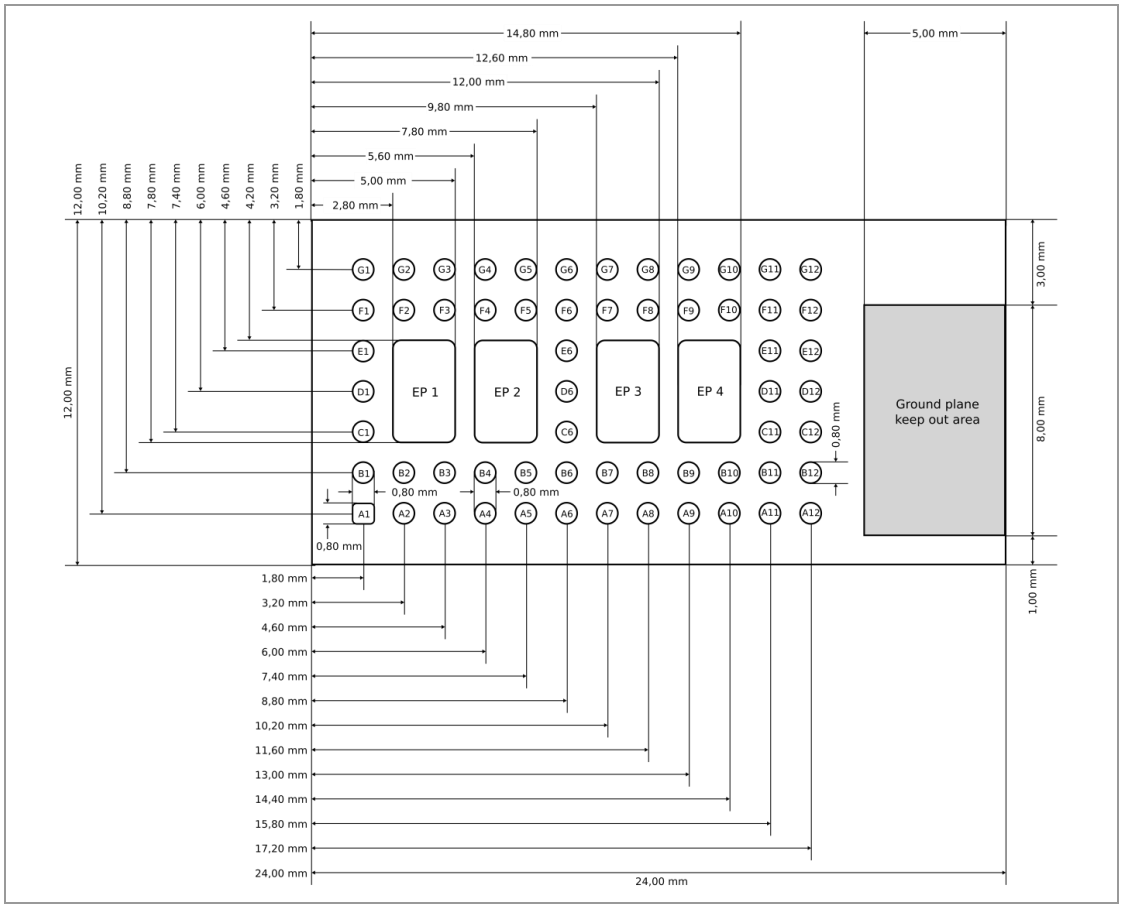


No.	Item	Dimension	Tolerance	Remark
1	Width	12.00	±0.35	
2	Length	24.00	±0.35	
3	Height	2.75	±0.20	With case

3.2 Footprint

The outer dimensions have a tolerance of ±0.35 mm.

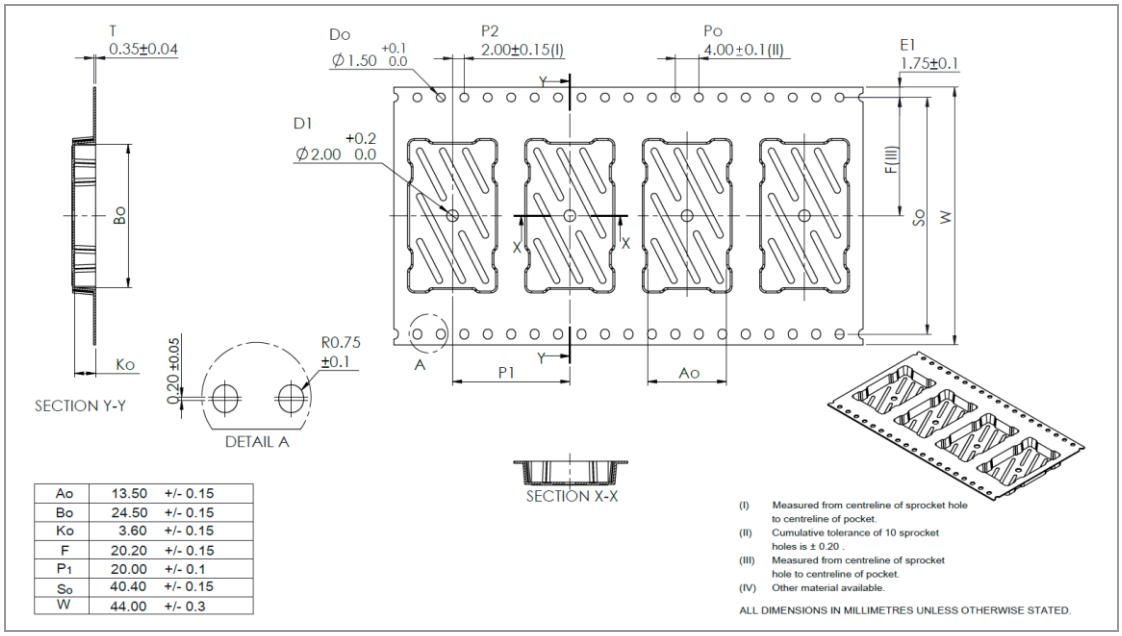
Top View



3.3 Packaging

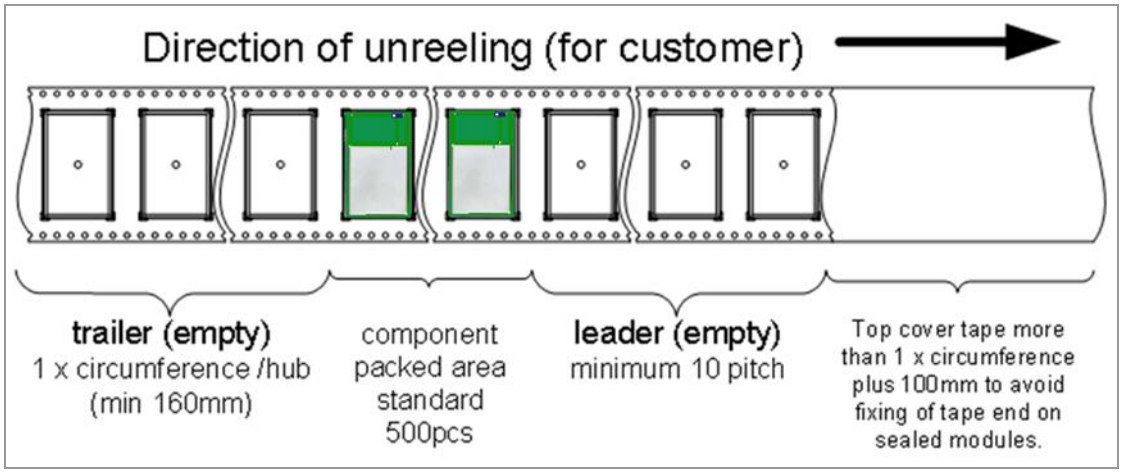
The module is a mass production status product and will be delivered in the package described below.

3.3.1 Tape Dimensions



Ao	13.50	+/- 0.15
Bo	24.50	+/- 0.15
Ko	3.60	+/- 0.15
F	20.20	+/- 0.15
P1	20.00	+/- 0.1
So	40.40	+/- 0.15
W	44.00	+/- 0.3

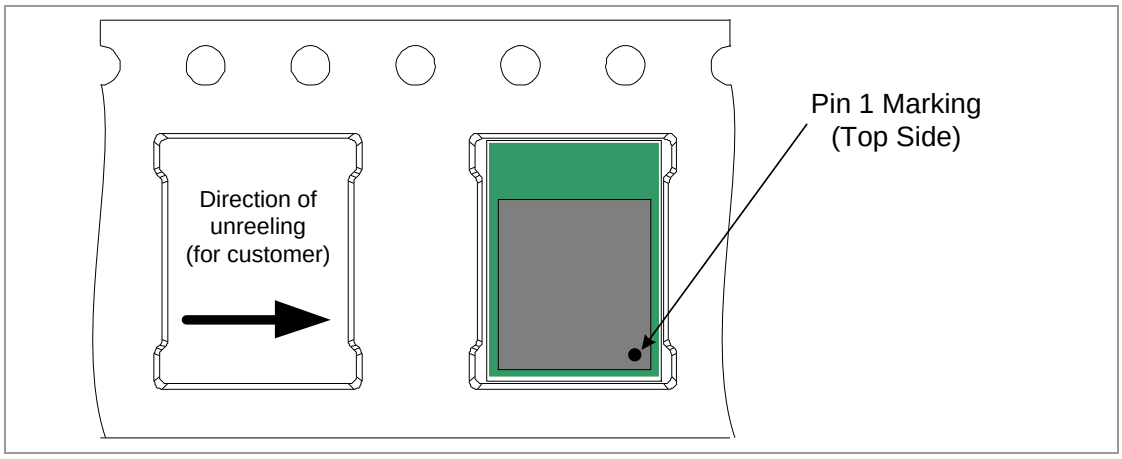
3.3.2 Packing in Tape



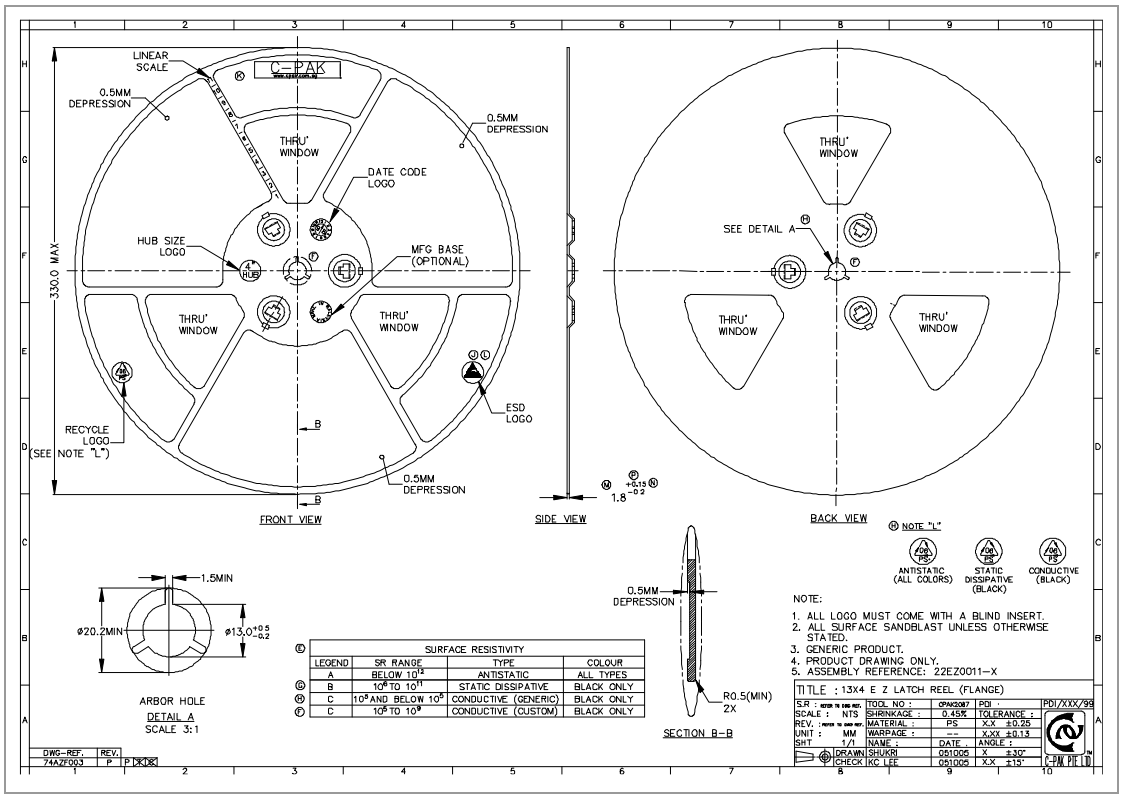
Empty spaces in the component packed area shall be less than two per reel and those spaces shall not be consecutive.

The top cover tape shall not be found on reel holes and it shall not stick out from the reel.

3.3.3 Component Direction

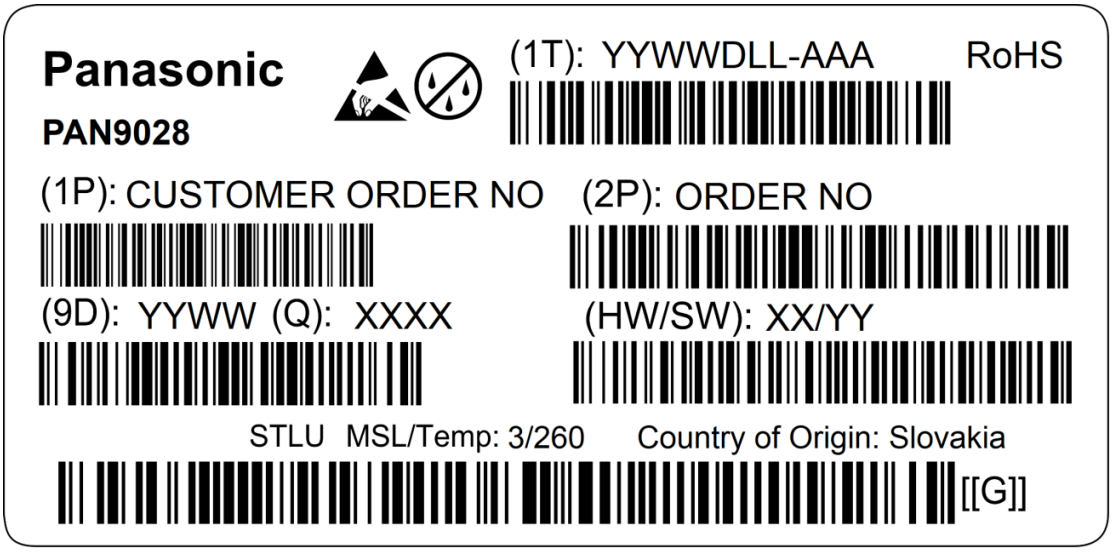


3.3.4 Reel Dimension



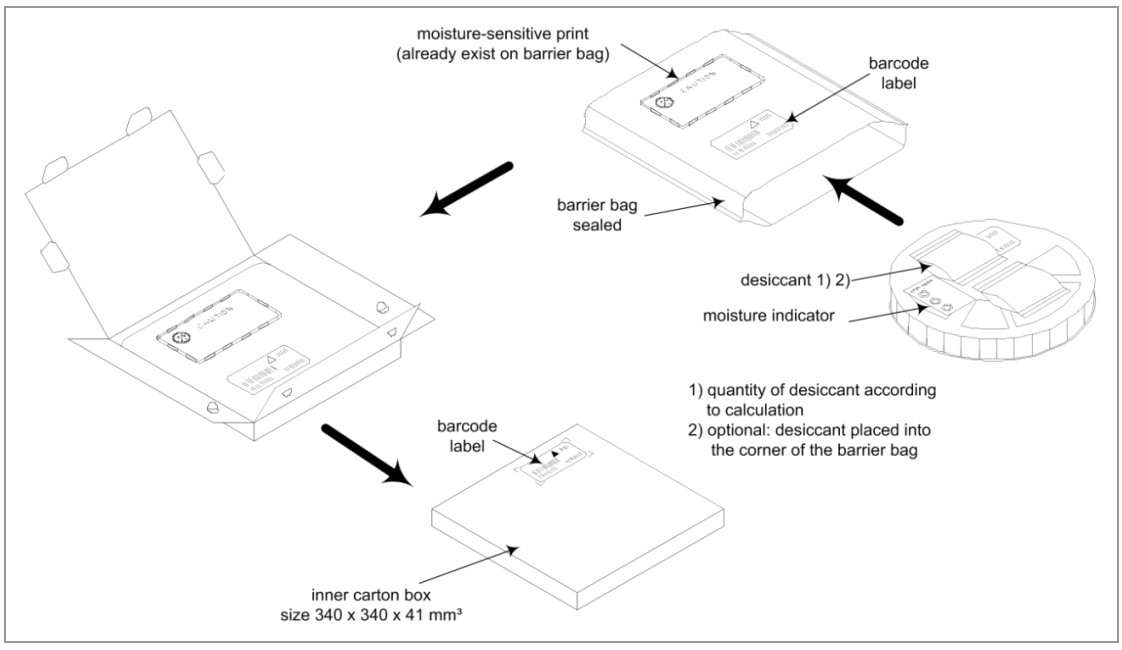
3.3.5 Package Label

Example:



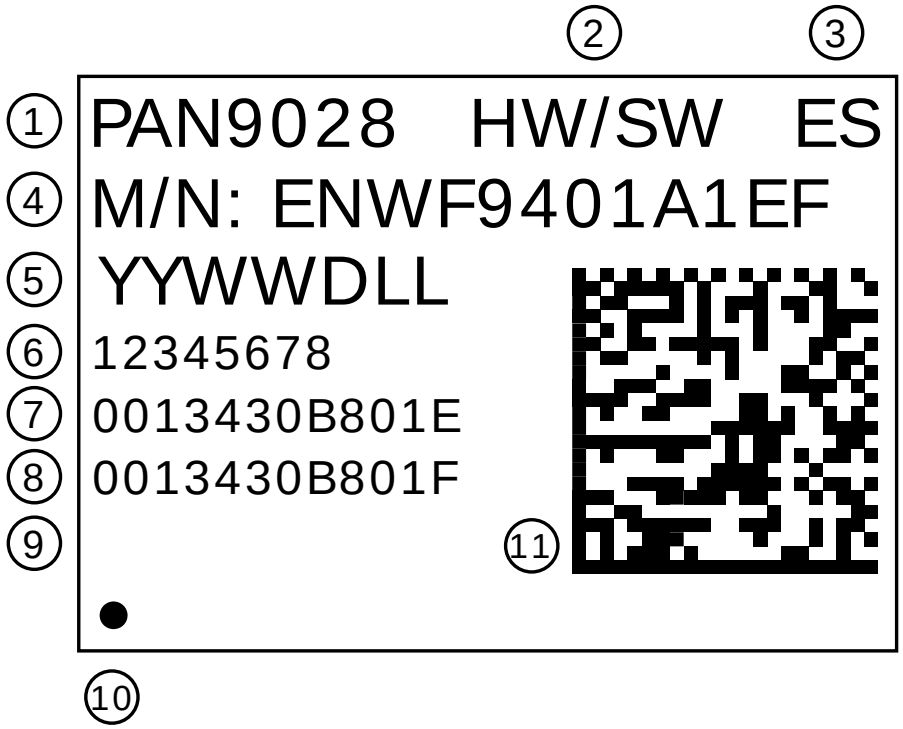
(1T)	Lot code
(1P)	Customer order number, if applicable
(2P)	Order number
(9D)	Date code
(Q)	Quantity
(HW/SW)	Hardware/software version

3.3.6 Total Package



3.4 Case Marking

Example:



1	Brand name
2	Hardware/software version
3	Engineering Sample (optional)
4	Order number
5	Lot code
6	Serial number
7	WLAN MAC address
8	BD address
9	(Reserved)
10	Marking for Pin 1
11	2D barcode, for internal usage only

4 Specification

All specifications are over temperature and process, unless indicated otherwise.

4.1 Default Test Conditions

Temperature:	25 °C ± 10 °C
Humidity:	40 to 85 % RH
Supply Voltage:	+3.3 V (for module variant ENWF490xA1EF)
Supply Voltage:	+3.3 V / +2.2 V / +1.8 V / +1.1 V (for module variant ENWF490xA2EF)

4.2 Absolute Maximum Ratings

The maximum ratings may not be exceeded under any circumstances, not even momentarily or individually, as permanent damage to the module may result.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
T_{STOR}	Storage temperature		-40		+85	°C
V_{ESD}	ESD robustness	All pads, according to human body model (HBM), JEDEC STD 22, method A114			1 000	V
		According to charged device model (CDM), JEDEC STD 22, method C101			500	V
P_{RF}	RF input level				+2	dBm
V_{DD3V3}	Maximum voltage	Maximum power supply voltage from any pin with respect to V_{SS} (GND)		3.3	4	V
V_{DD2V2}				2.2	2.3	V
V_{DD1V8}				1.8	1.98	V
V_{DD1V1}				1.1	1.21	V
V_{IOSD}				1.8	2.2	V
				3.3	4	V
V_{IO}				1.8	2.2	V
				3.3	4	V
$V_{RF\_SW1/2}$				3.3	4	V

4.3 Recommended Operating Conditions

The maximum ratings may not be exceeded under any circumstances, not even momentarily or individually, as permanent damage to the module may result.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
T_A	Ambient operating temperature range	Extended grade	-30		+85	°C
V_{DD3V3}	3.3 V supply voltage	V_{DD} voltage on pins F2, F3	3.07	3.3	3.53	V
V_{DD2V2}	2.2 V supply voltage	V_{DD} voltage on pins G1, G2 (only for module variant ENWF940[x]A2EF)	2.09	2.2	2.26	V
V_{DD1V8}	1.8 V supply voltage	V_{DD} voltage on pin G4 (only for module variant ENWF940[x]A2EF)	1.71	1.8	1.89	V
V_{DD1V1}	1.1 V supply voltage	V_{DD} voltage on pin A3 (only for module variant ENWF940[x]A2EF)	1.05	1.1	1.15	V
V_{IOSD}	Digital I/O VIOSD supply voltage[7]	Pin F4 with 1.8 V operation ⇨ SDIO Pin Functions	1.67	1.8	1.92	V
		Pin F4 with 3.3 V operation ⇨ SDIO Pin Functions	3.07	3.3	3.53	V
V_{IO}	Digital I/O VIO supply voltage[7]	Pin G3 with 1.8 V operation	1.67	1.8	1.92	V
		Pin G3 with 3.3 V operation	3.07	3.3	3.53	V
$V_{RF\_SW1/2}$	VRF_SW1/2 switch voltage	Pin A11, B11 with 3.3 V logical level switch operation ⇨ RF-Switch Pin Function	3.07	3.3	3.6	V

[7] 1.8 V or 3.3 V supply voltage possible.

Digital Pin Characteristics

V_{IO} with 1.8 V Operation[8]

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IH}	High level input voltage	1.8 V operation (V_{IO} = 1.8 V)	0.7 V_{IO}		V_{IO} + 0.4	V
V_{IL}	Low level input voltage	1.8 V operation (V_{IO} = 1.8 V)	-0.4		0.3 V_{IO}	V
V_{HYS}	Input hysteresis		100			mV
V_{OH}	High level output voltage	1.8 V operation (V_{IO} = 1.8 V)	V_{IO} - 0.4			V
V_{HO}	Low level output voltage	1.8 V operation (V_{IO} = 1.8 V)			0.4	V

V_{IO} with 3.3 V Operation[8]

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IH}	High level input voltage	3.3 V operation (V_{IO} = 3.3 V)	0.7 V_{IO}		V_{IO} + 0.4	V
V_{IL}	Low level input voltage	3.3 V operation (V_{IO} = 3.3 V)	-0.4		0.3 V_{IO}	V
V_{HYS}	Input hysteresis		100			mV
V_{OH}	High level output voltage	3.3 V operation (V_{IO} = 3.3 V)	V_{IO} - 0.4			V
V_{HO}	Low level output voltage	3.3 V operation (V_{IO} = 3.3 V)			0.4	V

V_{IOSD} with 1.8 V Operation for SDIO I/F[8]

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IH}	High level input voltage	1.8 V operation (V_{IOSD} = 1.8 V)	0.7 V_{IO}		V_{IO} + 0.4	V
V_{IL}	Low level input voltage	1.8 V operation (V_{IOSD} = 1.8 V)	-0.4		0.3 V_{IO}	V
V_{HYS}	Input hysteresis		100			mV
V_{OH}	High level output voltage	1.8 V operation (V_{IOSD} = 1.8 V)	V_{IO} - 0.4			V
V_{HO}	Low level output voltage	1.8 V operation (V_{IOSD} = 1.8 V)			0.4	V

[8] The capacitive load should not be larger than 50 pF for all I/Os when using the default driver strength settings. Large capacitive loads increase the overall current consumption.

V_{IOSD} with 3.3 V Operation for SDIO I/F[8]

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IH}	High level input voltage	3.3 V operation (V_{IOSD} = 3.3 V)	0.7 V_{IO}		V_{IO} + 0.4	V
V_{IL}	Low level input voltage	3.3 V operation (V_{IOSD} = 3.3 V)	-0.4		0.3 V_{IO}	V
V_{HYS}	Input hysteresis		100			mV
V_{OH}	High level output voltage	3.3 V operation (V_{IOSD} = 3.3 V)	V_{IO} - 0.4			V
V_{HO}	Low level output voltage	3.3 V operation (V_{IOSD} = 3.3 V)			0.4	V

4.4 Current Consumption

4.4.1 For ENWF940[x]A1EF

The current consumption depends on the user scenario and on the setup and timing in the power modes. Following current consumptions are valid for module variant ENWF940[x]A1EF.

Assume V_{DD} = 3.3 V, T_{amb} = 25 °C, if nothing else stated.

Parameter	Condition		Min.	Typ.	Max.	Unit
$I_{VDD3V3 @ PMIC\_EN}$	Power Down	Grounding of PMIC_EN pin		TBD		mA
$I_{VDD3V3 @ DeepSleep}$	Deep Sleep	Low-power state used in sleep state		TBD		mA
$I_{VDD3V3 @ Firmware Init}$	Firmware Initialization	Device Initialization			TBD	mA

WLAN Current Consumption

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$I_{VDD3V3 @ TX}$	Active Transmit[9]	P_{TX} = +TBD dBm for 5 GHz band 802.11a at 6 Mbps		TBD		mA
		P_{TX} = +TBD dBm for 5 GHz band 802.11n 20 MHz at 72 Mbps		TBD		mA
		P_{TX} = +TBD dBm for 5 GHz band 802.11ac 80 MHz at 433 Mbps		TBD		mA
		P_{TX} = +TBD dBm for 2.4 GHz band 802.11b at 11 Mbps		TBD		mA
		P_{TX} = +TBD dBm for 2.4 GHz band 802.11g at 54 Mbps		TBD		mA

[9] Peak values for specified output power level and data rate with UDP traffic between the AP and Device (STA).

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
		P_{TX} = +TBD dBm for 2.4 GHz band 802.11n 40 MHz at 150 Mbps		TBD		mA
$I_{VDD3V3 @ RX}$	Active Receive[9]	5 GHz band 802.11a at 6 Mbps		TBD		mA
		5 GHz band 802.11n 20 MHz at 72 Mbps		TBD		mA
		5 GHz band 802.11ac 80 MHz at 433 Mbps		TBD		mA
		2.4 GHz band 802.11b at 11 Mbps		TBD		mA
		2.4 GHz band 802.11g at 54 Mbps		TBD		mA
		2.4 GHz band 802.11n 40 MHz at 150 Mbps		TBD		mA
$I_{VDD3V3 @ IEEE-PS}$	IEEE Power Save[10]	DTIM = 1 with beacon interval 100 ms		TBD		mA

Bluetooth Current Consumption

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$I_{VDD3V3 @ TX}$	Peak BR	P_{TX} = +TBD dBm		TBD		mA
	Peak EDR	P_{TX} = +TBD dBm		TBD		mA
	Peak LE	P_{TX} = +TBD dBm		TBD		mA
$I_{VDD3V3 @ RX}$	Peak BR			TBD		mA
	Peak EDR			TBD		mA
	Peak LE			TBD		mA
$I_{SCAN BT}$	Page/Inquiry Scan	1.28 s at normal mode		TBD		mA
$I_{A2DP BT}$	A2DP	BR/EDR at 330 kbps (3M baud rate)		TBD		mA

4.4.2 For ENWF940[x]A2EF

The current consumption depends on the user scenario, on the setup, and timing in the power modes. Following current consumptions are valid for module variant ENWF940[x]A2EF.

Assume V_{DD3V3} = 3.3 V, V_{DD2V2} = 2.2 V, V_{DD1V8} = 1.8 V, V_{DD1V1} = 1.1 V and T_{amb} = 25 °C, if nothing else stated.

[10] In IEEE Power Save the device automatically wakes up on beacons. This is dependent on the DTIM value of the AP it is connected to. If it is a DTIM value of 1 along with a beacon interval of 100 ms, the device wakes up every 100 ms.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{VDD3V3}	Deep Sleep	Low-power state used in sleep state		TBD		mA
I_{VDD2V2}		Low-power state used in sleep state		TBD		mA
I_{VDD1V8}		Low-power state used in sleep state		TBD		mA
I_{VDD1V1}		Low-power state used in sleep state		TBD		mA
I_{VDD3V3}	Firmware Initialization	Device Initialization			TBD	mA
I_{VDD2V2}		Device Initialization			TBD	mA
I_{VDD1V8}		Device Initialization			TBD	mA
I_{VDD1V1}		Device Initialization			TBD	mA

WLAN Current Consumption

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$I_{VDD3V3\ @\ TX}$	Active Transmit[9]	P_{TX} = +TBD dBm for 5 GHz band 802.11a at 6 Mbps		TBD		mA
		P_{TX} = +TBD dBm for 5 GHz band 802.11n 20 MHz at 72 Mbps		TBD		mA
		P_{TX} = +TBD dBm for 5 GHz band 802.11ac 80 MHz at 433 Mbps		TBD		mA
		P_{TX} = +TBD dBm for 2.4 GHz band 802.11b at 11 Mbps		TBD		mA
		P_{TX} = +TBD dBm for 2.4 GHz band 802.11g at 54 Mbps		TBD		mA
		P_{TX} = +TBD dBm for 2.4 GHz band 802.11n 40 MHz at 150 Mbps		TBD		mA
$I_{VDD3V3\ @\ RX}$	Active Receive[9]	5 GHz band 802.11a at 6 Mbps		TBD		mA
		5 GHz band 802.11n 20 MHz at 72 Mbps		TBD		mA
		5 GHz band 802.11ac 80 MHz at 433 Mbps		TBD		mA
		2.4 GHz band 802.11b at 11 Mbps		TBD		mA
		2.4 GHz band 802.11g at 54 Mbps		TBD		mA
		2.4 GHz band 802.11n 40 MHz at 150 Mbps		TBD		mA
$I_{VDD3V3\ @\ IEEE-PS}$	IEEE Power Save[10]	DTIM = 1 with beacon interval 100 ms		TBD		mA
$I_{VDD2V2\ @\ TX}$	Active Transmit[9]	P_{TX} = +TBD dBm for 5 GHz band 802.11a at 6 Mbps		TBD		mA
		P_{TX} = +TBD dBm for 5 GHz band 802.11n 20 MHz at 72 Mbps		TBD		mA
		P_{TX} = +TBD dBm for 5 GHz band 802.11ac 80 MHz at 433 Mbps		TBD		mA
		P_{TX} = +TBD dBm for 2.4 GHz band 802.11b at 11 Mbps		TBD		mA
		P_{TX} = +TBD dBm for 2.4 GHz band 802.11g at 54 Mbps		TBD		mA

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
		P_{TX} = +TBD dBm for 2.4 GHz band 802.11n 40 MHz at 150 Mbps		TBD		mA
$I_{VDD2V2 @ RX}$	Active Receive[9]	5 GHz band 802.11a at 6 Mbps		TBD		mA
		5 GHz band 802.11n 20 MHz at 72 Mbps		TBD		mA
		5 GHz band 802.11ac 80 MHz at 433 Mbps		TBD		mA
		2.4 GHz band 802.11b at 11 Mbps		TBD		mA
		2.4 GHz band 802.11g at 54 Mbps		TBD		mA
		2.4 GHz band 802.11n 40 MHz at 150 Mbps		TBD		mA
$I_{VDD2V2 @ IEEE-PS}$	IEEE Power Save[10]	DTIM = 1 with beacon interval 100 ms		TBD		mA
$I_{VDD1V8 @ TX}$	Active Transmit[9]	P_{TX} = +TBD dBm for 5 GHz band 802.11a at 6 Mbps		TBD		mA
		P_{TX} = +TBD dBm for 5 GHz band 802.11n 20 MHz at 72 Mbps		TBD		mA
		P_{TX} = +TBD dBm for 5 GHz band 802.11ac 80 MHz at 433 Mbps		TBD		mA
		P_{TX} = +TBD dBm for 2.4 GHz band 802.11b at 11 Mbps		TBD		mA
		P_{TX} = +TBD dBm for 2.4 GHz band 802.11g at 54 Mbps		TBD		mA
		P_{TX} = +TBD dBm for 2.4 GHz band 802.11n 40 MHz at 150 Mbps		TBD		mA
$I_{VDD1V8 @ RX}$	Active Receive[9]	5 GHz band 802.11a at 6 Mbps		TBD		mA
		5 GHz band 802.11n 20 MHz at 72 Mbps		TBD		mA
		5 GHz band 802.11ac 80 MHz at 433 Mbps		TBD		mA
		2.4 GHz band 802.11b at 11 Mbps		TBD		mA
		2.4 GHz band 802.11g at 54 Mbps		TBD		mA
		2.4 GHz band 802.11n 40 MHz at 150 Mbps		TBD		mA
$I_{VDD1V8 @ IEEE-PS}$	IEEE Power Save[10]	DTIM = 1 with beacon interval 100 ms		TBD		mA
$I_{VDD1V1 @ TX}$	Active Transmit[9]	P_{TX} = +TBD dBm for 5 GHz band 802.11a at 6 Mbps		TBD		mA
		P_{TX} = +TBD dBm for 5 GHz band 802.11n 20 MHz at 72 Mbps		TBD		mA
		P_{TX} = +TBD dBm for 5 GHz band 802.11ac 80 MHz at 433 Mbps		TBD		mA
		P_{TX} = +TBD dBm for 2.4 GHz band 802.11b at 11 Mbps		TBD		mA
		P_{TX} = +TBD dBm for 2.4 GHz band 802.11g at 54 Mbps		TBD		mA

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
		P_{TX} = +TBD dBm for 2.4 GHz band 802.11n 40 MHz at 150 Mbps		TBD		mA
$I_{VDD1V1 @ RX}$	Active Receive[9]	5 GHz band 802.11a at 6 Mbps		TBD		mA
		5 GHz band 802.11n 20 MHz at 72 Mbps		TBD		mA
		5 GHz band 802.11ac 80 MHz at 433 Mbps		TBD		mA
		2.4 GHz band 802.11b at 11 Mbps		TBD		mA
		2.4 GHz band 802.11g at 54 Mbps		TBD		mA
		2.4 GHz band 802.11n 40 MHz at 150 Mbps		TBD		mA
$I_{VDD1V1 @ IEEE-PS}$	IEEE Power Save[10]	DTIM = 1 with beacon interval 100 ms		TBD		mA

Bluetooth Current Consumption

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$I_{VDD3V3 @ TX}$	Peak BR	P_{TX} = +TBD dBm		TBD		mA
	Peak EDR	P_{TX} = +TBD dBm		TBD		mA
	Peak LE	P_{TX} = +TBD dBm		TBD		mA
$I_{VDD3V3 @ RX}$	Peak BR			TBD		mA
	Peak EDR			TBD		mA
	Peak LE			TBD		mA
$I_{VDD2V2 @ TX}$	Peak BR	P_{TX} = +TBD dBm		TBD		mA
	Peak EDR	P_{TX} = +TBD dBm		TBD		mA
	Peak LE	P_{TX} = +TBD dBm		TBD		mA
$I_{VDD2V2 @ RX}$	Peak BR			TBD		mA
	Peak EDR			TBD		mA
	Peak LE			TBD		mA
$I_{VDD1V8 @ TX}$	Peak BR	P_{TX} = +TBD dBm		TBD		mA
	Peak EDR	P_{TX} = +TBD dBm		TBD		mA
	Peak LE	P_{TX} = +TBD dBm		TBD		mA
$I_{VDD1V8 @ RX}$	Peak BR			TBD		mA
	Peak EDR			TBD		mA
	Peak LE			TBD		mA
$I_{VDD1V1 @ TX}$	Peak BR	P_{TX} = +TBD dBm		TBD		mA
	Peak EDR	P_{TX} = +TBD dBm		TBD		mA
	Peak LE	P_{TX} = +TBD dBm		TBD		mA
$I_{VDD1V1 @ RX}$	Peak BR			TBD		mA
	Peak EDR			TBD		mA
	Peak LE			TBD		mA
$I_{VDD3V3 SCAN BT}$	Page/Inquiry Scan	1.28 s at normal mode		TBD		mA

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$I_{VDD2V2\ SCAN\ BT}$	Page/Inquiry Scan	1.28 s at normal mode		TBD		mA
$I_{VDD1V8\ SCAN\ BT}$	Page/Inquiry Scan	1.28 s at normal mode		TBD		mA
$I_{VDD1V1\ SCAN\ BT}$	Page/Inquiry Scan	1.28 s at normal mode		TBD		mA
$I_{VDD3V3\ A2DP\ BT}$	A2DP	BR/EDR at 330 kbps (3M baud rate)		TBD		mA
$I_{VDD2V2\ A2DP\ BT}$	A2DP	BR/EDR at 330 kbps (3M baud rate)		TBD		mA
$I_{VDD1V8\ A2DP\ BT}$	A2DP	BR/EDR at 330 kbps (3M baud rate)		TBD		mA
$I_{VDD1V1\ A2DP\ BT}$	A2DP	BR/EDR at 330 kbps (3M baud rate)		TBD		mA

4.5 Internal Operating Frequencies

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$f_{SYSCLK1}$	CPU1/System/ Encryption clock speed	Refers to clock speed of SoC's CPU1			256	MHz
$f_{SYSCLK2}$	CPU2	Refers to clock speed of SoC's CPU2			64	MHz
$f_{REFCLK1}$	Crystal fundamental frequency	Frequency tolerance < ±10 ppm over operating temperature and process		26		MHz
$f_{SLEEPCLK}$ (only for module variant ENWF940[x]A1EF)	Sleep Clock frequency	Frequency tolerance < ±30 ppm over operating temperature, aging and process, CMOS input clock signal type		32.768		kHz

4.6 External Sleep Clock Specifications (only for Module Variant ENWF940[x]A2EF)

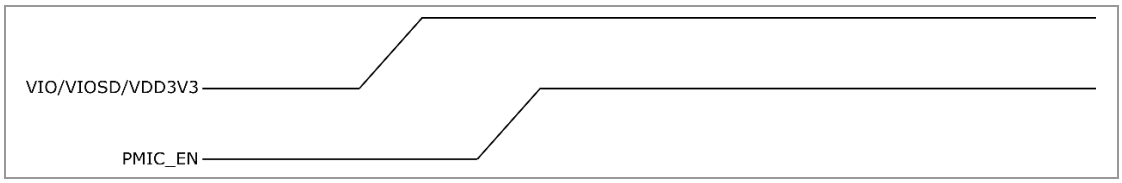
An external sleep clock of 32.768 kHz can be used for lowest current consumption in sleep mode. Voltage level of external sleep clock must be the same value which is used for Pin G4 (V_{IO}).

Parameter	Min.	Typ.	Max.	Units
Clock frequency range/accuracy • CMOS input clock signal type • ±250 ppm (initial, aging, temperature)		32.768		kHz
Phase noise requirement (at 100 kHz)		-125		dBc/Hz
Cycle jitter		1.5		ns (RMS)
Slew rate limit (10 % to 90 %)			100	ns
Duty cycle tolerance	20		80	%

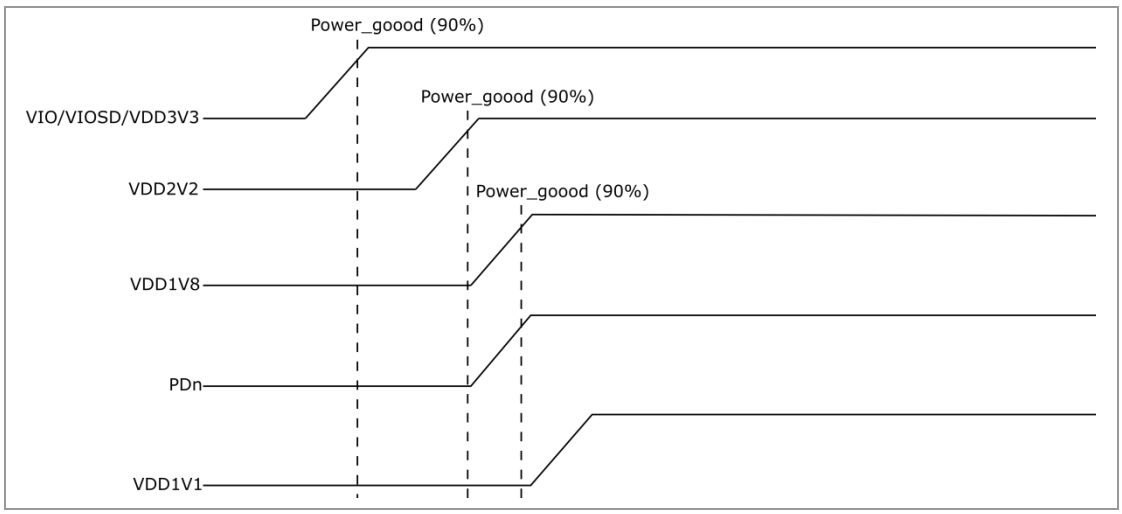
4.7 Power-up Sequence

For Module Variant ENWF940[x]A1EF:

A minimum time of 100 ms is required after PMIC_EN is de-asserted (low) and before it is asserted (high).



For Module Variant ENWF940[x]A2EF:



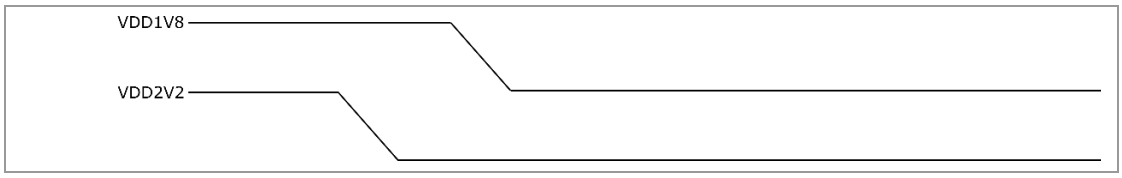
- $V_{IO}/V_{IOSD}/V_{DD3V3}$ must be good (90 %) before or at the same time all other power supplies start ramping up.
- $V_{IO}/V_{IOSD}/V_{DD3V3}$ must be good (90%) before or at the same time PDn starts ramping up.
- V_{DD2V2} must be good (90 %) before or at the same time V_{DD1V8} starts ramping up.
- It is recommended to start ramping up VDD1V8 ≤ 1ms after V_{DD2V2} ramps up.
- V_{DD1V8} must be good (90 %) before or at the same time VDD1V1 starts ramping up.
- Ramp-up time of $V_{IO}/V_{IOSD}/V_{DD3V3}$ must be < 100 ms.
- Ramp-up time of V_{DD2V2} / V_{DD1V8} must be < 100 ms.
- Ramp-up time of V_{DD1V1} must be < 5ms.
- All supplies must be monotonic.

4.8 Power-down Sequence

For Module Variant ENWF940[x]A1EF:

Power down sequencing is performed from internal power management IC after PMIC_EN pin is pulled to low state.

For Module Variant ENWF940[x]A2EF:



- It is recommended to ramp down VDD1V8 after VDD2V2 ramps down.
- It is recommended to discharge all of the power supplies to less than 0.2V to reduce leakage
- PDn must be asserted when powering down the module

4.9 Power Good (only for Module Variant ENWF940[x]A1EF)

Do not connect the power good outputs (PG1, PG2, and PGLDO) if they are not used.

The PAN9028 contains power good comparators, which pull the signal to a logical low level, when the associated output voltage drops below 90 % of its regulated value. Also, when the associated rising output voltage is above 95 % of its regulated value, the power good comparators pull the signal to a logical low level.

No.	Pin Name	Pin Type	Logical Level	
			Low (typ. 0 V)	High (typ. 3.3 V)
B1	PG1	Output signal	1.1 V voltage supply not stabilized	1.1 V voltage supply stabilized
D1	PG2	Output signal	2.2 V voltage supply not stabilized	2.2 V voltage supply stabilized
C1	PGLDO	Output signal	1.8 V voltage supply not stabilized	1.8 V voltage supply stabilized

4.10 Interfaces

4.10.1 Host Interface

4.10.1.1 SDIO Interface

The SDIO Interface pins are powered from the V_{IOSD} voltage supply with either 3.3 V or 1.8 V. The SDIO electrical specifications are identical for the 1-bit and 4-bit SDIO modes.

For DC specifications please refer to “Digital Pin Characteristics” ⇨ 4.3 Recommended Operating Conditions.

SDIO Timing Data – Default and High-Speed Modes (V_{IOSD} 3.3 V)[11,12]

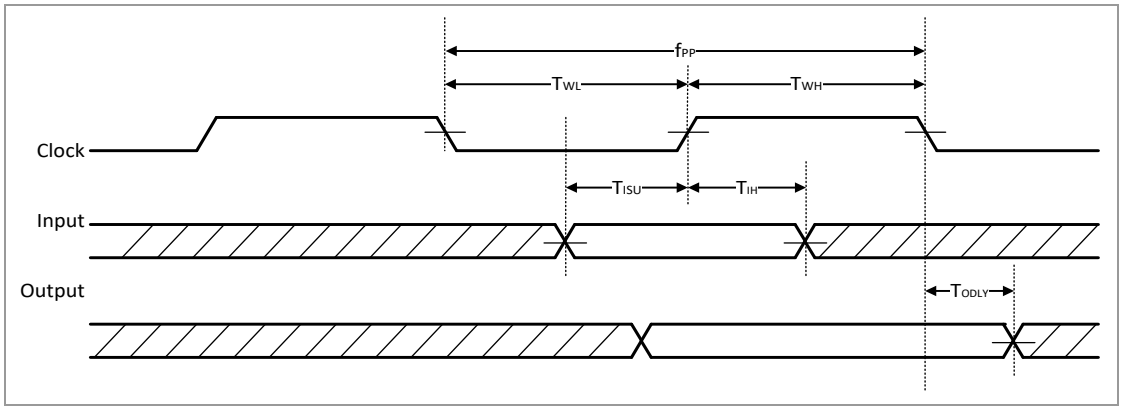
Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
f_{PP}	Clock frequency	Normal	0		25	MHz
		High-speed	0		50	MHz
T_{WL}	Clock low time	Normal	10			ns
		High-speed	7			ns

[11] For SDIO 2.0 running at 50 MHz clock frequency, a supply voltage VIOSD of 1.8 V is recommended.

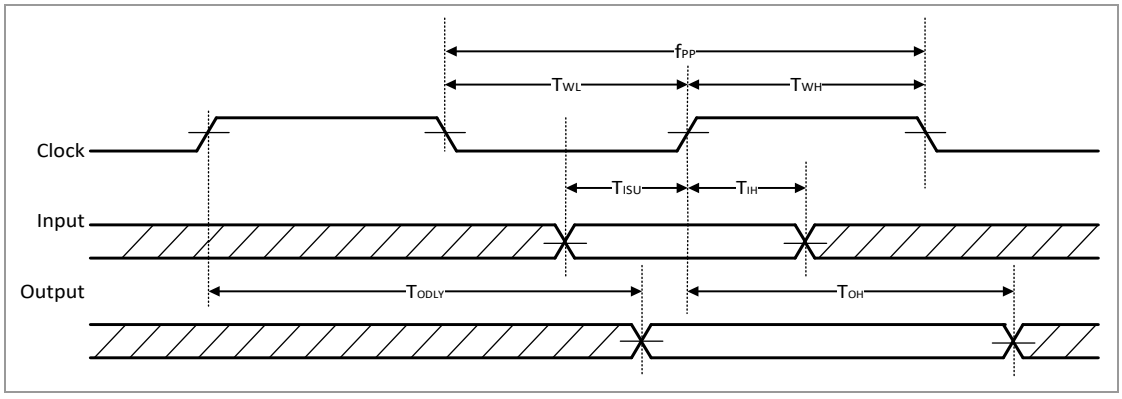
[12] For SDIO 2.0 running at 25 MHz clock frequency, either 1.8 V or 3.3 V can be used.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
T_{WH}	Clock high time	Normal	10			ns
		High-speed	7			ns
T_{ISU}	Input setup time	Normal	5			ns
		High-speed	6			ns
T_{IH}	Input hold time	Normal	5			ns
		High-speed	2			ns
T_{ODLY}	Output delay time	Normal			14	ns
	CL ≤ 40 pF (1 card)	High-speed			14	ns
T_{OH}	Output hold time	High-speed	2.5			ns

SDIO Protocol Timing Diagram – Default Speed Mode (V_{IOSD} 3.3 V)



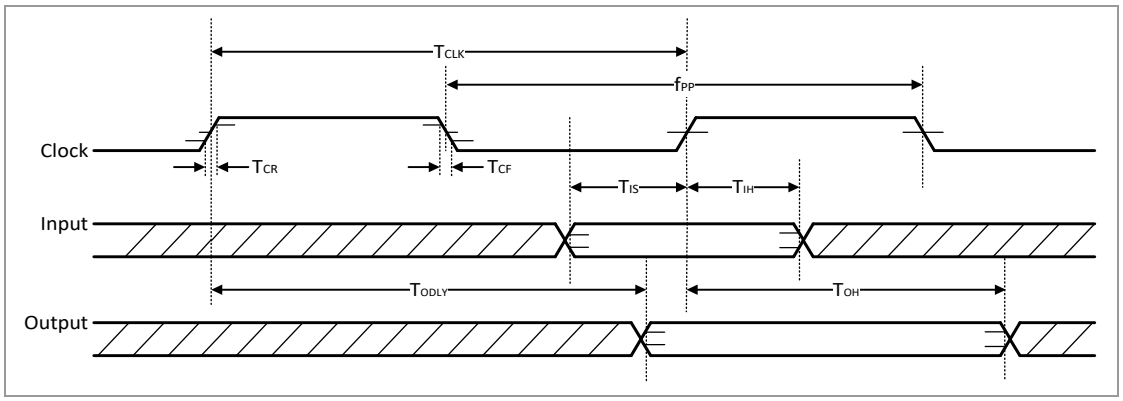
SDIO Protocol Timing Diagram – High-Speed Mode (V_{IOSD} 3.3 V)



SDIO Timing Data – SDR12, SDR25, SDR50 Modes (VIOSD 1.8 V)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
f_{PP}	Clock frequency	SDR12/SDR25/SDR50	25		100	MHz
T_{IS}	Input setup time	SDR12/SDR25/SDR50	3			ns
T_{IH}	Input hold time	SDR12/SDR25/SDR50	0.8			ns
T_{CLK}	Clock time	SDR12/SDR25/SDR50	10		40	ns
T_{CR}, T_{CF}	Rise time, fall time T_{CR}, T_{CF} < 2 ns (max) at 100 MHz C_{CARD} = 10 pF	SDR12/SDR25/SDR50			0.2 T_{CLK}	ns
T_{ODLY}	Output delay time CL ≤ 30 pF	SDR12/SDR25/SDR50			7.5	ns
T_{OH}	Output hold time CL ≤ 15 pF	SDR12/SDR25/SDR50	1.5			ns

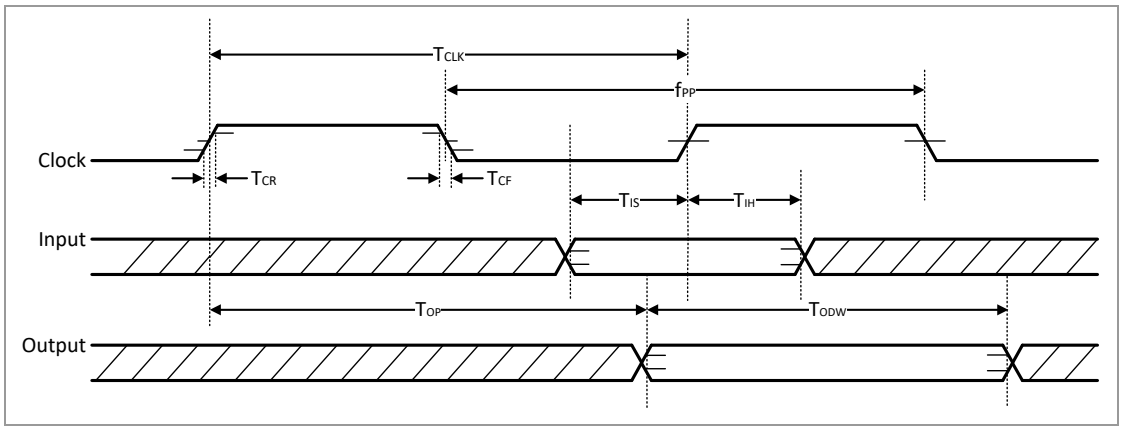
SDIO Protocol Timing Diagram – SDR12, SDR25, SDR50 Modes (V_{IOSD} 1.8 V)



SDIO Timing Data – SDR104 Mode (V_{IOSD} 1.8 V)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
f_{PP}	Clock frequency	SDR104	0		208	MHz
T_{IS}	Input setup time	SDR104	1.4			ns
T_{IH}	Input hold time	SDR104	0.8			ns
T_{CLK}	Clock time	SDR104	4.8			ns
T_{CR}, T_{CF}	Rise time, fall time T_{CR}, T_{CF} < 0.96 ns (max) at 208 MHz C_{CARD} = 10 pF	SDR104			0.2 T_{CLK}	ns
T_{OP}	Card output phase	SDR104	0		10	ns
T_{ODW}	Output timing of variable data window	SDR104	2.88			ns

SDIO Protocol Timing Diagram – SDR104 Mode (V_{IOSD} 1.8 V)

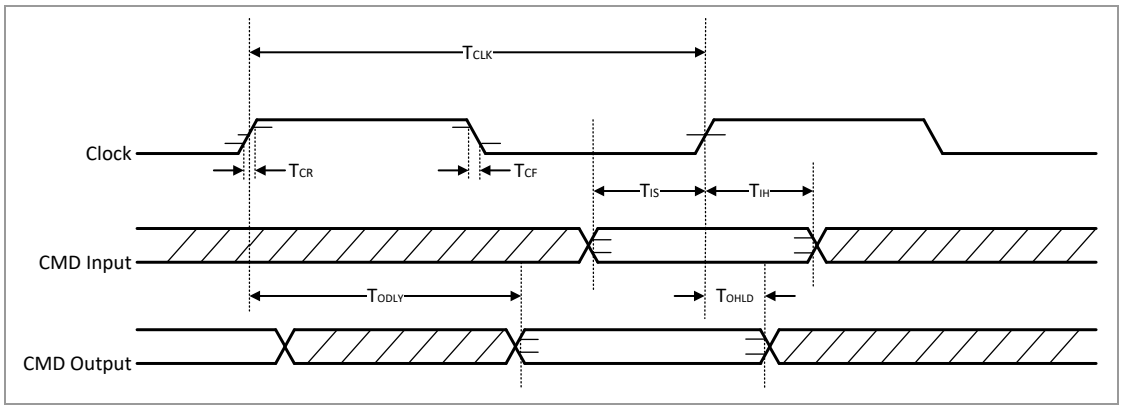


SDIO Timing Data – DDR50 Mode (V_{IOSD} 1.8 V)

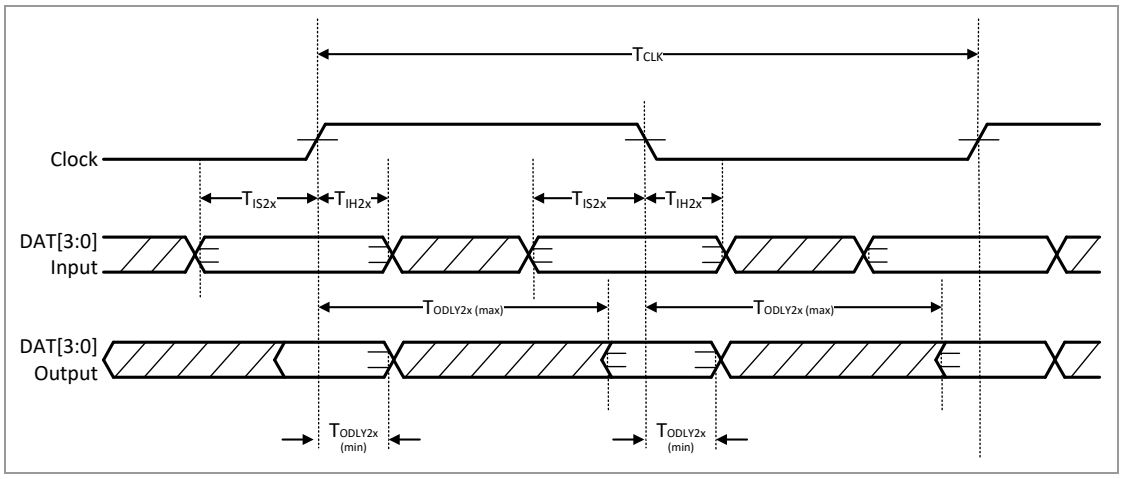
Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Clock						
T_{CLK}	Clock time 50 MHz (max) between rising edges	DDR50	20			ns
T_{CR}, T_{CF}	Rise time, fall time T_{CR}, T_{CF} < 4.00 ns (max) at 50 MHz C_{CARD} = 10 pF	DDR50			0.2 T_{CLK}	ns
Clock Duty		DDR50	45		55	%
CMD Input (referenced to clock rising edge)						
T_{IS}	Input setup time C_{CARD} ≤ 10 pF (1 card)	DDR50	6			ns
T_{IH}	Input hold time C_{CARD} ≤ 10 pF (1 card)	DDR50	0.8			ns
CMD Output (referenced to clock rising edge)						
T_{OLDY}	Output delay time during data transfer mode C_L ≤ 30 pF (1 card)	DDR50			13.7	ns
T_{OHLD}	Output hold time C_L ≤ 15 pF (1 card)	DDR50	1.5			ns
DAT[3:0] Input (referenced to clock rising and falling edges)						
T_{IS2x}	Input setup time C_{CARD} ≤ 10 pF (1 card)	DDR50	3			ns
T_{IH2x}	Input hold time C_{CARD} ≤ 10 pF (1 card)	DDR50	0.8			ns

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
DAT[3:0] Output (referenced to clock rising and falling edges)						
TODLY2x (max)	Output delay time during data transfer mode $C_L \leq 25$ pF (1 card)	DDR50			7.0	ns
TODLY2x (min)	Output hold time $C_L \leq 15$ pF (1 card)	DDR50	1.5			ns

SDIO CMD Timing Diagram – DDR50 Mode (V_{IOSD} 1.8 V, 50 MHz)



SDIO DAT[3:0] Timing Diagram – DDR50 Mode (V_{IOSD} 1.8 V, 50 MHz)



4.10.1.2 High-Speed UART Interface

The High-Speed UART Interface pins are powered from the V_{IO} voltage supply with either 3.3 V or 1.8 V.

For DC specifications please refer to “Digital Pin Characteristics” ⇨ 4.3 Recommended Operating Conditions.

The UART interface operation includes:

- Support data input/output operations for peripheral devices connected through a standard UART interface
- 4-wire data transfer (RxD, TxD, RTS and CTS) or 6-wire data transfer (RxD, TxD, RTS, CTS, DSR, and DTR)
- Programmable baud rate (1 200 bps to 4 Mbps)
- Data format (LSB first)
- Data bit: (5 bit to 8 bit)
- Parity bit: (0 bit to 4 bit)
- Stop bit: (1 bit to 2 bit)

Interface Signals

Pin No.	Signal Name	Specification Name	Type	Description
B8	UART_SOUT	TxD	Host Controller Interface (HCI)	Transmit data output
A8	UART_SIN	RxD		Receive data input
A7	UART_RTS	RTS		Request to send (active low)
A6	UART_CTS	CTS		Clear to send (active low)
B6	UART_DSR	DSR	optional	Data set ready (active low)
B7	UART_DTR	DTR		Data terminal ready (active low)

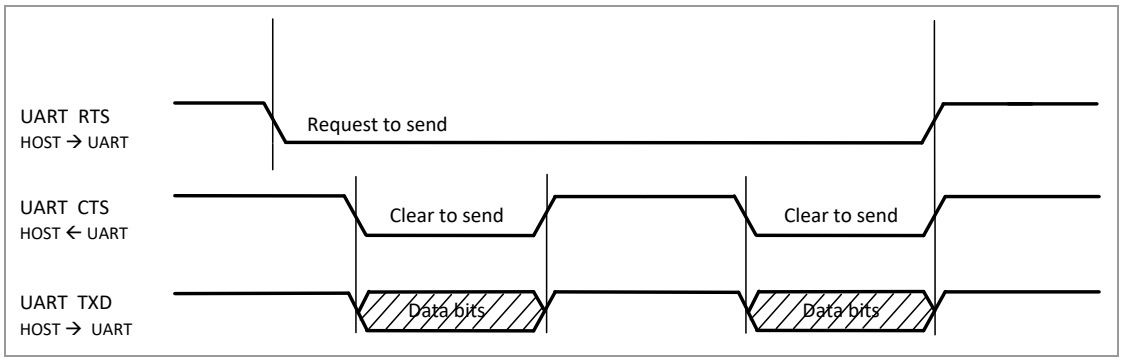
Interface Transport Settings

Item	Range	Default	Comment
Baud Rate	1 200 ~ 4 000 000	3 000 000	Baud
Data Bits	5 ~ 8	8	LSB first
Parity Bits	0 ~ 4	0	
Stop Bits	1/1.5/2	1	

Supported Baud Rates

Baud Rate				
1 200	2 400	4 800	9 600	19 200
38 400	57 600	76 800	115 200	230 400
460 800	500 000	921 600	1 000 000	1 382 400
1 500 000	1 843 200	2 000 000	2 100 000	2 764 800
3 000 000	3 250 000	3 692 300	4 000 000	

UART Timing Diagram



4.10.2 Peripheral Interface

The Peripheral Interface pins are powered from the V_{IO} voltage supply with either 3.3 V or 1.8 V.

For DC specifications please refer to “Digital Pin Characteristics” ⇨ 4.3 Recommended Operating Conditions.

GPIO Interface

The General-Purpose I/O (GPIO) interface is used to implement user-defined input and output signals to and from the device, such as external interrupts and other user-defined I/Os.

Configurable GPIOs

Function	GPIO Pin Name									
	IO0	IO1	IO2	IO3	IO4	IO5	IO6	IO7	IO8	IO9
GPIO IN	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES
GPIO OUT	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES
IRQ IN	YES	YES	YES	YES	YES	YES	YES	YES	YES	YES
LED	NO	NO	YES	YES	NO	NO	NO	NO	NO	NO

Function	GPIO Pin Name								
	IO10	IO11	IO12	IO13	IO14	IO15	IO16	IO17	IO20
GPIO IN	YES	YES	YES	YES	YES	YES	YES	YES	YES
GPIO OUT	YES	YES	YES	YES	YES	YES	YES	YES	YES
IRQ IN	YES	YES	YES	YES	YES	YES	YES	YES	YES
LED	NO	NO	NO	NO	NO	NO	NO	NO	NO

LED Mode

Symbol	Parameter	Condition	Typ.	Units
I_{OH}	Switching current high	Tristate on pin (requires pull-up)	Tristate when driving high	mA
I_{OL}	Switching current low	At 0.4 V	10	mA

4.10.3 Audio Interface: PCM Interface

Interface Signals

Pin No.	Signal Name	Specification Name	Type	Description
F7	PCM_DOUT	DOUT	Output	PCM data
E1	PCM_CLK	CLK	Input/Output	PCM clock signal, output if PCM master, input if PCM slave
E1	PCM_MCLK	MCLK	Output	PCM clock signal (optional), optional clock used for some codecs, derived from PCM_CLK
E11	PCM_DIN	DIN	Input	PCM data
F6	PCM_SYNC	SYNC	Input/Output	PCM Sync pulse signal, output if PCM master, input if PCM slave

Modes of Operation

The PCM Interface supports two modes of operation:

- PCM master
- PCM slave

When in PCM master mode, the interface generates a 2 MHz or a 2.048 MHz PCM_CLK and a 8 kHz PCM_SYNC signal. An alternative PCM master mode is available that uses an externally generated PCM_CLK, but still generate the 8 kHz PCM_SYNC. The external PCM_CLK must have a frequency that is an integer multiple of 8 kHz. Supported frequencies are in the 512 kHz to 4 MHz range.

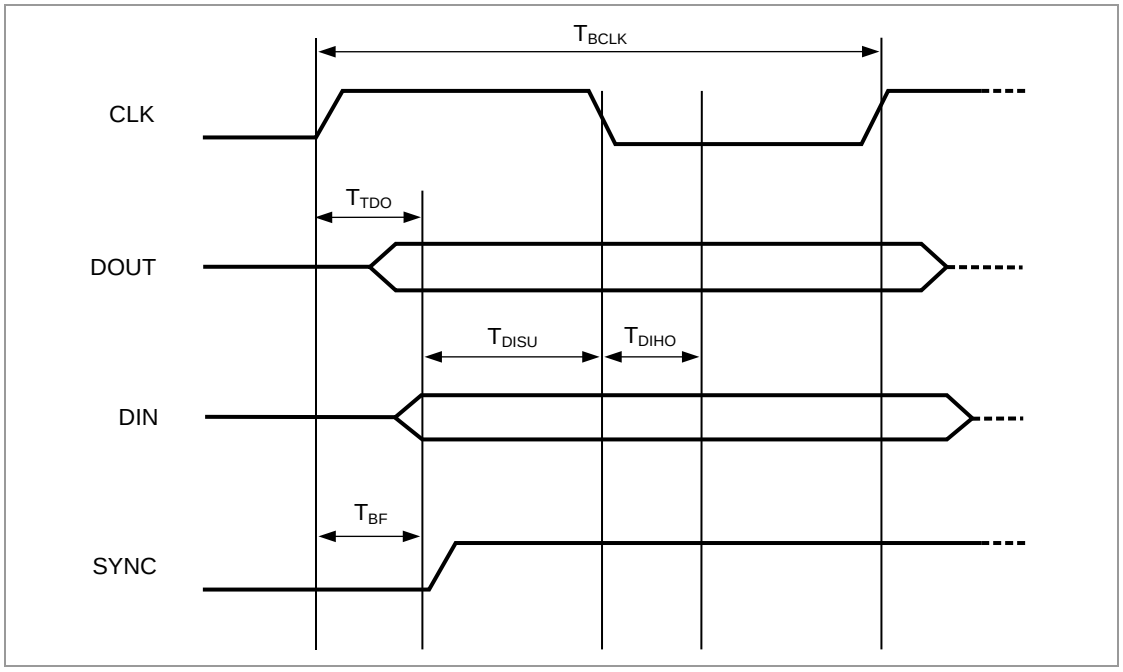
When in PCM slave mode, the interface has both PCM_CLK and PCM_SYNC as inputs, thereby letting another unit on the PCM bus generate the signals.

The PCM interface consists of up to four PCM slots (time-divided) preceded by a PCM sync signal. Each PCM slot can be either 8 bits or 16 bits wide. The slots can be separated in time, but they are not required to follow immediately after another. The timing is relative to PCM_SYNC.

PCM Timing Data – Master Mode

Symbol	Min.	Typ.	Max.	Units
F_{BCLK}		2/2.048		MHz
Duty $Cycle_{BLCK}$	0.4	0.5	0.6	
$T_{BCLK\ rise/fall}$		3		ns
T_{DO}			15	ns
T_{DISU}	20			ns
T_{DIHO}	15			ns
T_{BF}			15	ns

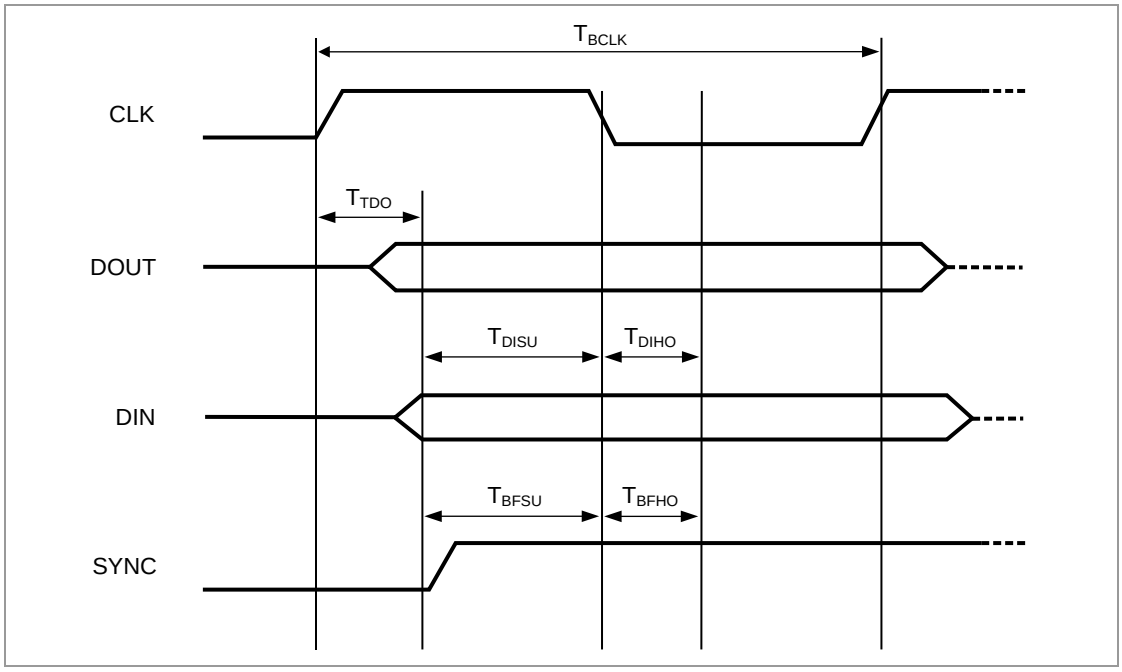
PCM Timing Diagram – Master Mode



PCM Timing Data – Slave Mode

Symbol	Min.	Typ.	Max.	Units
F_{BCLK}		2/2.048		MHz
Duty $Cycle_{BLCK}$	0.4	0.5	0.6	
$T_{BCLK\ rise/fall}$		3		ns
T_{DO}			30	ns
T_{DISU}	15			ns
T_{DIHO}	10			ns
T_{BFSU}	15			ns
T_{BFHO}	10			

PCM Timing Diagram – Slave Mode



4.10.4 Coexistence Interface

The Peripheral Interface pins are powered from the V_{IO} voltage supply with either 3.3 V or 1.8 V.

For DC specifications please refer to “Digital Pin Characteristics” ⇨ 4.3 Recommended Operating Conditions.

4.11 RF Electrical Characteristics

4.11.1 WLAN Radio Specification

Receive Mode

Parameter	Condition	Min.	Typ.	Max.	Units
RF frequency range	2.4 GHz – IEEE 802.11b/g/n	2 400		2 500	MHz
	5 GHz – IEEE 802.11a/n/ac	4 900		5 925	MHz

Transmit Mode

Parameter	Condition	Min.	Typ.	Max.	Units
RF frequency range	2.4 GHz – IEEE 802.11b/g/n	2 400		2 500	MHz
	5 GHz – IEEE 802.11a/n/ac	4 900		5 925	MHz

4.11.2 WLAN RF Characteristics

4.11.2.1 RF Characteristics for IEEE 802.11b

For module variant ENWF940[x]A1EF assume V_{DD3V3} = 3.3 V, V_{IOSD} = 3.3 V, V_{IO} = 3.3 V and T_{amb} = 25 °C, if nothing else stated.

For module variant ENWF940[x]A2EF assume V_{DD3V3} = 3.3 V, V_{DD2V2} = 2.2 V, V_{DD1V8} = 1.8 V, V_{DD1V1} = 1.1 V, V_{IOSD} = 3.3 V, V_{IO} = 3.3 V and T_{amb} = 25 °C, if nothing else stated.

50 Ω terminal load connected to the RF connector.

Parameter		Condition	Min.	Typ.	Max.	Units
RF frequency range			2 400		2 483.5	MHz
Carrier frequency tolerance			-25		+25	ppm
Transmit output power				+16		dBm
Spectrum mask	f_C ± 11 MHz				-30	dBr
	f_C ± 22 MHz				-50	dBr
Power-on/Power-down ramp					2	µs
RF Carrier suppression					-15	dB
Error Vector Magnitude (EVM)	Peak				35	%
Minimum receive sensitivity	1 Mbps (DSSS)	FER ≤ 8 %		-97		dBm
	2 Mbps (DSSS)	FER ≤ 8 %		-93	-80	dBm
	5.5 Mbps (CCK)	FER ≤ 8 %		-91		dBm
	11 Mbps (CCK)	FER ≤ 8 %		-88	-76	dBm
Maximum input level		FER ≤ 8 %			-10	dBm
Adjacent channel rejection		FER ≤ 8 %	35			dB

4.11.2.2 RF Characteristics for IEEE 802.11g

For module variant ENWF940[x]A1EF assume V_{DD3V3} = 3.3 V, V_{IOSD} = 3.3 V, V_{IO} = 3.3 V and T_{amb} = 25 °C, if nothing else stated.

For module variant ENWF940[x]A2EF assume V_{DD3V3} = 3.3 V, V_{DD2V2} = 2.2 V, V_{DD1V8} = 1.8 V, V_{DD1V1} = 1.1 V, V_{IOSD} = 3.3 V, V_{IO} = 3.3 V and T_{amb} = 25 °C, if nothing else stated.

50 Ω terminal load connected to the RF connector.

Parameter		Condition	Min.	Typ.	Max.	Units
RF frequency range	2.4 GHz		2 400		2 483.5	MHz
Carrier frequency tolerance			-25		+25	ppm
Transmit output power	6 Mbps ~ 36 Mbps			+16		dBm
	48 Mbps ~ 54 Mbps			+16		dBm
Spectrum mask	f_C ± 11 MHz				-20	dBr
	f_C ± 20 MHz				-28	dBr
	f_C ± 30 MHz				-40	dBr
Transmitter center frequency leakage					-15	dB
Transmitter Spectral Flatness			-4		+4	dB
EVM Constellation Error (EVM)	BPSK, CR 1/2 (6 Mbps)				-5	dB
	BPSK, CR 3/4 (9 Mbps)				-8	dB
	QPSK, CR 1/2 (12 Mbps)				-10	dB
	QPSK, CR 3/4 (18 Mbps)				-13	dB
	16-QAM, CR 1/2 (24 Mbps)				-16	dB
	16-QAM, CR 3/4 (36 Mbps)				-19	dB
	64-QAM, CR 2/3 (48 Mbps)				-22	dB
	64-QAM, CR 3/4 (54 Mbps)				-25	dB
Minimum receive sensitivity	BPSK, CR 1/2 (6 Mbps)	PER ≤ 10 %		-89	-82	dBm
	BPSK, CR 3/4 (9 Mbps)	PER ≤ 10 %		-89	-81	dBm
	QPSK, CR 1/2 (12 Mbps)	PER ≤ 10 %		-88	-79	dBm
	QPSK, CR 3/4 (18 Mbps)	PER ≤ 10 %		-86	-77	dBm
	16-QAM, CR 1/2 (24 Mbps)	PER ≤ 10 %		-83	-74	dBm
	16-QAM, CR 3/4 (36 Mbps)	PER ≤ 10 %		-80	-70	dBm
	64-QAM, CR 2/3 (48 Mbps)	PER ≤ 10 %		-76	-66	dBm
	64-QAM, CR 3/4 (54 Mbps)	PER ≤ 10 %		-74	-65	dBm
Maximum input level		PER ≤ 10 %			-20	dBm
Adjacent channel rejection		PER ≤ 10 %	16			dB
		PER ≤ 10 %	-1			dB

4.11.2.3 RF Characteristics for IEEE 802.11n (BW 20 MHz, 2.4 GHz)

For module variant ENWF940[x]A1EF assume V_{DD3V3} = 3.3 V, V_{IOSD} = 3.3 V, V_{IO} = 3.3 V and T_{amb} = 25 °C, if nothing else stated.

For module variant ENWF940[x]A2EF assume V_{DD3V3} = 3.3 V, V_{DD2V2} = 2.2 V, V_{DD1V8} = 1.8 V, V_{DD1V1} = 1.1 V, V_{IOSD} = 3.3 V, V_{IO} = 3.3 V and T_{amb} = 25 °C, if nothing else stated.

50 Ω terminal load connected to the RF connector.

Parameter		Condition	Min.	Typ.	Max.	Units
RF frequency range	2.4 GHz		2 400		2 483.5	MHz
Carrier frequency tolerance			-25		+25	ppm
Transmit output power	MCS0 ~ MCS2			+16		dBm
	MCS3 ~ MCS4			+16		dBm
	MCS5 ~ MCS7			+16		dBm
Spectrum mask	f_C ± 11 MHz				-20	dBr
	f_C ± 20 MHz				-28	dBr
	f_C ± 30 MHz				-45	dBr
Transmitter center frequency leakage					-15	dB
Transmitter spectral flatness			-4		+4	dB
Constellation Error (EVM)	BPSK, CR 1/2 (MCS0)				-5	dB
	QPSK, CR 1/2 (MCS1)				-10	dB
	QPSK, CR 3/4 (MCS2)				-13	dB
	16-QAM, CR 1/2 (MCS3)				-16	dB
	16-QAM, CR 3/4 (MCS4)				-19	dB
	64-QAM, CR 2/3 (MCS5)				-22	dB
	64-QAM, CR 3/4 (MCS6)				-25	dB
	64-QAM, CR 5/6 (MCS7)				-27	dB
Minimum receive sensitivity[13]	6.5 Mbps (MCS0)	PER ≤ 10 %		-89	-82	dBm
	13 Mbps (MCS1)	PER ≤ 10 %		-87	-79	dBm
	19.5 Mbps (MCS2)	PER ≤ 10 %		-84	-77	dBm
	26 Mbps (MCS3)	PER ≤ 10 %		-81	-74	dBm
	39 Mbps (MCS4)	PER ≤ 10 %		-78	-70	dBm
	52 Mbps (MCS5)	PER ≤ 10 %		-75	-66	dBm
	58.5 Mbps (MCS6)	PER ≤ 10 %		-73	-65	dBm
	65 Mbps (MCS7)	PER ≤ 10 %		-71	-64	dBm

[13] The minimum sensitivity levels apply only to non-STBC modes, MCS 0~7, 800 ns LGI, and BCC.

Parameter		Condition	Min.	Typ.	Max.	Units
Maximum input level		PER ≤ 10 %			-20	dBm
Adjacent channel rejection[14]	65 Mbps (MCS7)	PER ≤ 10 %	-2			dB

4.11.2.4 RF Characteristics for IEEE 802.11n (BW 40 MHz, 2.4 GHz)

For module variant ENWF940[x]A1EF assume V_{DD3V3} = 3.3 V, V_{IOSD} = 3.3 V, V_{IO} = 3.3 V and T_{amb} = 25 °C, if nothing else stated.

For module variant ENWF940[x]A2EF assume V_{DD3V3} = 3.3 V, V_{DD2V2} = 2.2 V, V_{DD1V8} = 1.8 V, V_{DD1V1} = 1.1 V, V_{IOSD} = 3.3 V, V_{IO} = 3.3 V and T_{amb} = 25 °C, if nothing else stated.

50 Ω terminal load connected to the RF connector.

Parameter		Condition	Min.	Typ.	Max.	Units
RF frequency range	2.4 GHz		2 400		2 483.5	MHz
Carrier frequency tolerance			-25		+25	ppm
Transmit output power	MCS0 ~ MCS2			+14		dBm
	MCS3 ~ MCS4			+14		dBm
	MCS5 ~ MCS7			+13		dBm
Spectrum mask	f_C ± 21 MHz				-20	dBr
	f_C ± 40 MHz				-28	dBr
	f_C ± 60 MHz				-45	dBr
Transmitter center frequency leakage					-20	dB
Transmitter spectral flatness			-4		+4	dB
Constellation Error (EVM)	BPSK, CR 1/2 (MCS0)				-5	dB
	QPSK, CR 1/2 (MCS1)				-10	dB
	QPSK, CR 3/4 (MCS2)				-13	dB
	16-QAM, CR 1/2 (MCS3)				-16	dB
	16-QAM, CR 3/4 (MCS4)				-19	dB
	64-QAM, CR 2/3 (MCS5)				-22	dB
	64-QAM, CR 3/4 (MCS6)				-25	dB
	64-QAM, CR 5/6 (MCS7)				-27	dB
Minimum receive sensitivity[13]	13.5 Mbps (MCS0)	PER ≤ 10 %		-83	-79	dBm
	27 Mbps (MCS1)	PER ≤ 10 %		-83	-76	dBm
	40.5 Mbps (MCS2)	PER ≤ 10 %		-80	-74	dBm
	54 Mbps (MCS3)	PER ≤ 10 %		-78	-71	dBm

[14] The adjacent channel rejection levels apply only to non-STBC modes, MCS 0~7, 800 ns LGI, and BCC.

Parameter		Condition	Min.	Typ.	Max.	Units
	81 Mbps (MCS4)	PER ≤ 10 %		-73	-67	dBm
	108 Mbps (MCS5)	PER ≤ 10 %		-70	-63	dBm
	121.5 Mbps (MCS6)	PER ≤ 10 %		-68	-62	dBm
	135 Mbps (MCS7)	PER ≤ 10 %		-66	-61	dBm
Maximum input level		PER ≤ 10 %			-20	dBm
Adjacent channel rejection[14]	135 Mbps (MCS7)	PER ≤ 10 %	-2			dB

4.11.2.5 RF Characteristics for IEEE 802.11n (BW 20 MHz, 5 GHz)

For module variant ENWF940[x]A1EF assume V_{DD3V3} = 3.3 V, V_{IOSD} = 3.3 V, V_{IO} = 3.3 V and T_{amb} = 25 °C, if nothing else stated.

For module variant ENWF940[x]A2EF assume V_{DD3V3} = 3.3 V, V_{DD2V2} = 2.2 V, V_{DD1V8} = 1.8 V, V_{DD1V1} = 1.1 V, V_{IOSD} = 3.3 V, V_{IO} = 3.3 V and T_{amb} = 25 °C, if nothing else stated.

50 Ω terminal load connected to the RF connector.

Parameter		Condition	Min.	Typ.	Max.	Units
RF frequency range	5 GHz U-NII-1		5 150		5 250	MHz
	5 GHz U-NII-2A		5 250		5 350	MHz
	5 GHz U-NII-2C		5 470		5 725	MHz
	5 GHz U-NII-3		5 725		5 825	MHz
Carrier frequency tolerance			-20		+20	ppm
Transmit output power	MCS0 ~ MCS2			+16		dBm
	MCS3 ~ MCS4			+16		dBm
	MCS5 ~ MCS7			+15		dBm
Spectrum mask	f_C ± 11 MHz				-20	dBr
	f_C ± 20 MHz				-28	dBr
	f_C ± 30 MHz				-40	dBr
Transmitter center frequency leakage					-15	dB
Transmitter spectral flatness			-4		+4	dB
Constellation Error (EVM)	BPSK, CR 1/2 (MCS0)				-5	dB
	QPSK, CR 1/2 (MCS1)				-10	dB
	QPSK, CR 3/4 (MCS2)				-13	dB
	16-QAM, CR 1/2 (MCS3)				-16	dB
	16-QAM, CR 3/4 (MCS4)				-19	dB
	64-QAM, CR 2/3 (MCS5)				-22	dB
	64-QAM, CR 3/4 (MCS6)				-25	dB
	64-QAM, CR 5/6 (MCS7)				-27	dB

Parameter		Condition	Min.	Typ.	Max.	Units
Minimum receive sensitivity[13]	6.5 Mbps (MCS0)	PER ≤ 10 %		-90	-82	dBm
	13 Mbps (MCS1)	PER ≤ 10 %		-87	-79	dBm
	19.5 Mbps (MCS2)	PER ≤ 10 %		-85	-77	dBm
	26 Mbps (MCS3)	PER ≤ 10 %		-82	-74	dBm
	39 Mbps (MCS4)	PER ≤ 10 %		-80	-70	dBm
	52 Mbps (MCS5)	PER ≤ 10 %		-75	-66	dBm
	58.5 Mbps (MCS6)	PER ≤ 10 %		-74	-65	dBm
	65 Mbps (MCS7)	PER ≤ 10 %		-72	-64	dBm
Maximum input level		PER ≤ 10 %			-30	dBm
Adjacent channel rejection[14]	65 Mbps (MCS7)	PER ≤ 10 %	-2			dB

4.11.2.6 RF Characteristics for IEEE 802.11n (BW 40 MHz, 5 GHz)

For module variant ENWF940[x]A1EF assume V_{DD3V3} = 3.3 V, V_{IOSD} = 3.3 V, V_{IO} = 3.3 V and T_{amb} = 25 °C, if nothing else stated.

For module variant ENWF940[x]A2EF assume V_{DD3V3} = 3.3 V, V_{DD2V2} = 2.2 V, V_{DD1V8} = 1.8 V, V_{DD1V1} = 1.1 V, V_{IOSD} = 3.3 V, V_{IO} = 3.3 V and T_{amb} = 25 °C, if nothing else stated.

50 Ω terminal load connected to the RF connector.

Parameter		Condition	Min.	Typ.	Max.	Units
RF frequency range	5 GHz U-NII-1		5 150		5 250	MHz
	5 GHz U-NII-2A		5 250		5 350	MHz
	5 GHz U-NII-2C		5 470		5 725	MHz
	5 GHz U-NII-3		5 725		5 825	MHz
Carrier frequency tolerance			-20		+20	ppm
Transmit output power	MCS0 ~ MCS2			+16		dBm
	MCS3 ~ MCS4			+16		dBm
	MCS5 ~ MCS7			+15		dBm
Spectrum mask	f_C ± 21 MHz				-20	dBr
	f_C ± 40 MHz				-28	dBr
	f_C ± 60 MHz				-40	dBr
Transmitter center frequency leakage					-20	dB
Transmitter spectral flatness			-4		+4	dB
Constellation Error (EVM)	BPSK, CR 1/2 (MCS0)				-5	dB
	QPSK, CR 1/2 (MCS1)				-10	dB
	QPSK, CR 3/4 (MCS2)				-13	dB
	16-QAM, CR 1/2 (MCS3)				-16	dB

Parameter		Condition	Min.	Typ.	Max.	Units
	16-QAM, CR 3/4 (MCS4)				-19	dB
	64-QAM, CR 2/3 (MCS5)				-22	dB
	64-QAM, CR 3/4 (MCS6)				-25	dB
	64-QAM, CR 5/6 (MCS7)				-27	dB
Minimum receive sensitivity[13]	13.5 Mbps (MCS0)	PER ≤ 10 %		-87	-79	dBm
	27 Mbps (MCS1)	PER ≤ 10 %		-84	-76	dBm
	40.5 Mbps (MCS2)	PER ≤ 10 %		-82	-74	dBm
	54 Mbps (MCS3)	PER ≤ 10 %		-79	-71	dBm
	81 Mbps (MCS4)	PER ≤ 10 %		-77	-67	dBm
	108 Mbps (MCS5)	PER ≤ 10 %		-73	-63	dBm
	121.5 Mbps (MCS6)	PER ≤ 10 %		-71	-62	dBm
	135 Mbps (MCS7)	PER ≤ 10 %		-70	-61	dBm
Maximum input level		PER ≤ 10 %			-30	dBm
Adjacent channel rejection[14]	135 Mbps (MCS7)	PER ≤ 10 %	-2			dB

4.11.2.7 RF Characteristics for IEEE 802.11ac (BW 20 MHz)

For module variant ENWF940[x]A1EF assume V_{DD3V3} = 3.3 V, V_{IOSD} = 3.3 V, V_{IO} = 3.3 V and T_{amb} = 25 °C, if nothing else stated.

For module variant ENWF940[x]A2EF assume V_{DD3V3} = 3.3 V, V_{DD2V2} = 2.2 V, V_{DD1V8} = 1.8 V, V_{DD1V1} = 1.1 V, V_{IOSD} = 3.3 V, V_{IO} = 3.3 V and T_{amb} = 25 °C, if nothing else stated.

50 Ω terminal load connected to the RF connector.

Parameter		Condition	Min.	Typ.	Max.	Units
RF frequency range	5 GHz U-NII-1		5 150		5 250	MHz
	5 GHz U-NII-2A		5 250		5 350	MHz
	5 GHz U-NII-2C		5 470		5 725	MHz
	5 GHz U-NII-3		5 725		5 825	MHz
Carrier frequency tolerance			-20		+20	ppm
Transmit output power	MCS0 ~ MCS2			+16		dBm
	MCS3 ~ MCS4			+16		dBm
	MCS5 ~ MCS7			+15		dBm
	MCS8			+15		dBm
Spectrum mask	f_C ± 11 MHz				-20	dBr
	f_C ± 20 MHz				-28	dBr
	f_C ± 30 MHz				-40	dBr
Transmitter center frequency leakage	P is transmit power per antenna in dBm				P-17.48	dB

Parameter		Condition	Min.	Typ.	Max.	Units
Transmitter spectral flatness			-4		+4	dB
Constellation Error (EVM)	BPSK, CR 1/2 (MCS0)				-5	dB
	QPSK, CR 1/2 (MCS1)				-10	dB
	QPSK, CR 3/4 (MCS2)				-13	dB
	16-QAM, CR 1/2 (MCS3)				-16	dB
	16-QAM, CR 3/4 (MCS4)				-19	dB
	64-QAM, CR 2/3 (MCS5)				-22	dB
	64-QAM, CR 3/4 (MCS6)				-25	dB
	64-QAM, CR 5/6 (MCS7)				-27	dB
	256-QAM, CR 3/4 (MCS8)				-30	dB
Minimum receive sensitivity[13]	6.5 Mbps (MCS0)	PER ≤ 10 %		-90	-82	dBm
	13 Mbps (MCS1)	PER ≤ 10 %		-87	-79	dBm
	19.5 Mbps (MCS2)	PER ≤ 10 %		-85	-77	dBm
	26 Mbps (MCS3)	PER ≤ 10 %		-82	-74	dBm
	39 Mbps (MCS4)	PER ≤ 10 %		-80	-70	dBm
	52 Mbps (MCS5)	PER ≤ 10 %		-75	-66	dBm
	58.5 Mbps (MCS6)	PER ≤ 10 %		-74	-65	dBm
	65 Mbps (MCS7)	PER ≤ 10 %		-72	-64	dBm
	78 Mbps (MCS 8)	PER ≤ 10 %		-68	-59	dBm
Maximum input level		PER ≤ 10 %			-30	dBm
Adjacent channel rejection[14]	78 Mbps (MCS8)	PER ≤ 10 %	-7			dB

4.11.2.8 RF Characteristics for IEEE 802.11ac (BW 40 MHz)

For module variant ENWF940[x]A1EF assume V_{DD3V3} = 3.3 V, V_{IOSD} = 3.3 V, V_{IO} = 3.3 V and T_{amb} = 25 °C, if nothing else stated.

For module variant ENWF940[x]A2EF assume V_{DD3V3} = 3.3 V, V_{DD2V2} = 2.2 V, V_{DD1V8} = 1.8 V, V_{DD1V1} = 1.1 V, V_{IOSD} = 3.3 V, V_{IO} = 3.3 V and T_{amb} = 25 °C, if nothing else stated.

50 Ω terminal load connected to the RF connector.

Parameter		Condition	Min.	Typ.	Max.	Units
RF frequency range	5 GHz U-NII-1		5 150		5 250	MHz
	5 GHz U-NII-2A		5 250		5 350	MHz
	5 GHz U-NII-2C		5 470		5 725	MHz
	5 GHz U-NII-3		5 725		5 825	MHz
Carrier frequency tolerance			-20		+20	ppm
Transmit output power	MCS0 ~ MCS2			+16		dBm

Parameter		Condition	Min.	Typ.	Max.	Units
	MCS3 ~ MCS4			+16		dBm
	MCS5 ~ MCS7			+15		dBm
	MCS8 ~ MCS9			+14		dBm
Spectrum mask	f_C ± 21 MHz				-20	dBr
	f_C ± 40 MHz				-28	dBr
	f_C ± 60 MHz				-40	dBr
Transmitter center frequency leakage	P is transmit power per antenna in dBm				P-20.57	dB
Transmitter spectral flatness			-4		+4	dB
Constellation Error (EVM)	BPSK, CR 1/2 (MCS0)				-5	dB
	QPSK, CR 1/2 (MCS1)				-10	dB
	QPSK, CR 3/4 (MCS2)				-13	dB
	16-QAM, CR 1/2 (MCS3)				-16	dB
	16-QAM, CR 3/4 (MCS4)				-19	dB
	64-QAM, CR 2/3 (MCS5)				-22	dB
	64-QAM, CR 3/4 (MCS6)				-25	dB
	64-QAM, CR 5/6 (MCS7)				-27	dB
	256-QAM, CR 3/4 (MCS8)				-30	dB
	256-QAM, CR 5/6 (MCS9)				-32	dB
Minimum receive sensitivity[13]	13.5 Mbps (MCS0)	PER ≤ 10 %		-87	-79	dBm
	27 Mbps (MCS1)	PER ≤ 10 %		-84	-76	dBm
	40.5 Mbps (MCS2)	PER ≤ 10 %		-82	-74	dBm
	54 Mbps (MCS3)	PER ≤ 10 %		-79	-71	dBm
	81 Mbps (MCS4)	PER ≤ 10 %		-77	-67	dBm
	108 Mbps (MCS5)	PER ≤ 10 %		-73	-63	dBm
	121.5 Mbps (MCS6)	PER ≤ 10 %		-71	-62	dBm
	135 Mbps (MCS7)	PER ≤ 10 %		-70	-61	dBm
	162 Mbps (MCS8)	PER ≤ 10 %		-65	-56	dBm
	180 Mbps (MCS9)	PER ≤ 10 %		-64	-54	dBm
Maximum input level		PER ≤ 10 %			-30	dBm
Adjacent channel rejection[14]	180 Mbps (MCS9)	PER ≤ 10 %	-9			dB

4.11.2.9 RF Characteristics for IEEE 802.11ac (BW 80 MHz)

For module variant ENWF940[x]A1EF assume V_{DD3V3} = 3.3 V, V_{IOSD} = 3.3 V, V_{IO} = 3.3 V and T_{amb} = 25 °C, if nothing else stated.

For module variant ENWF940[x]A2EF assume V_{DD3V3} = 3.3 V, V_{DD2V2} = 2.2 V, V_{DD1V8} = 1.8 V, V_{DD1V1} = 1.1 V, V_{IOSD} = 3.3 V, V_{IO} = 3.3 V and T_{amb} = 25 °C, if nothing else stated.

50 Ω terminal load connected to the RF connector.

Parameter		Condition	Min.	Typ.	Max.	Units
RF frequency range	5 GHz U-NII-1		5 150		5 250	MHz
	5 GHz U-NII-2A		5 250		5 350	MHz
	5 GHz U-NII-2C		5 470		5 725	MHz
	5 GHz U-NII-3		5 725		5 825	MHz
Carrier frequency tolerance			-20		+20	ppm
Transmit output power	MCS0 ~ MCS2			+14		dBm
	MCS3 ~ MCS4			+14		dBm
	MCS5 ~ MCS7			+12		dBm
	MCS8 ~ MCS9			+6		dBm
Spectrum mask	f_C ± 41 MHz				-20	dBr
	f_C ± 80 MHz				-28	dBr
	f_C ± 120 MHz				-40	dBr
Transmitter center frequency leakage	P is transmit power per antenna in dBm				P-23.84	dB
Transmitter spectral flatness			-4		+4	dB
Constellation Error (EVM)	BPSK, CR 1/2 (MCS0)				-5	dB
	QPSK, CR 1/2 (MCS1)				-10	dB
	QPSK, CR 3/4 (MCS2)				-13	dB
	16-QAM, CR 1/2 (MCS3)				-16	dB
	16-QAM, CR 3/4 (MCS4)				-19	dB
	64-QAM, CR 2/3 (MCS5)				-22	dB
	64-QAM, CR 3/4 (MCS6)				-25	dB
	64-QAM, CR 5/6 (MCS7)				-27	dB
	256-QAM, CR 3/4 (MCS8)				-30	dB
	256-QAM, CR 5/6 (MCS9)				-32	dB
Minimum receive sensitivity[13]	29.3 Mbps (MCS0)	PER ≤ 10 %		-83	-76	dBm
	58.5 Mbps (MCS1)	PER ≤ 10 %		-81	-73	dBm
	87.8 Mbps (MCS2)	PER ≤ 10 %		-78	-71	dBm
	117 Mbps (MCS3)	PER ≤ 10 %		-76	-68	dBm
	175.5 Mbps (MCS4)	PER ≤ 10 %		-74	-64	dBm

Parameter		Condition	Min.	Typ.	Max.	Units
	234 Mbps (MCS5)	PER ≤ 10 %		-69	-60	dBm
	263.3 Mbps (MCS6)	PER ≤ 10 %		-68	-59	dBm
	292.5 Mbps (MCS7)	PER ≤ 10 %		-66	-58	dBm
	351 Mbps (MCS8)	PER ≤ 10 %		-62	-53	dBm
	390 Mbps (MCS9)	PER ≤ 10 %		-59	-51	dBm
Maximum input level		PER ≤ 10 %			-30	dBm
Adjacent channel rejection[14]	390 Mbps (MCS9)	PER ≤ 10 %	-9			dB

4.11.2.10 RF Characteristics for IEEE 802.11a

For module variant ENWF940[x]A1EF assume V_{DD3V3} = 3.3 V, V_{IOSD} = 3.3 V, V_{IO} = 3.3 V and T_{amb} = 25 °C, if nothing else stated.

For module variant ENWF940[x]A2EF assume V_{DD3V3} = 3.3 V, V_{DD2V2} = 2.2 V, V_{DD1V8} = 1.8 V, V_{DD1V1} = 1.1 V, V_{IOSD} = 3.3 V, V_{IO} = 3.3 V and T_{amb} = 25 °C, if nothing else stated.

50 Ω terminal load connected to the RF connector.

Parameter		Condition	Min.	Typ.	Max.	Units
RF frequency range	5 GHz U-NII-1		5 150		5 250	MHz
	5 GHz U-NII-2A		5 250		5 350	MHz
	5 GHz U-NII-2C		5 470		5 725	MHz
	5 GHz U-NII-3		5 725		5 825	MHz
Carrier frequency tolerance			-20		+20	Ppm
Transmit output power	6 Mbps ~ 36 Mbps			+16		dBm
	48 Mbps ~ 54 Mbps			+16		dBm
Spectrum mask	f_C ± 11 MHz				-20	dBr
	f_C ± 20 MHz				-28	dBr
	f_C ± 30 MHz				-40	dBr
Transmitter center frequency leakage					-15	dB
Transmitter spectral flatness			-4		+4	dB
Constellation Error (EVM)	BPSK, CR 1/2 (6 Mbps)				-5	dB
	BPSK, CR 3/4 (9 Mbps)				-8	dB
	QPSK, CR 1/2 (12 Mbps)				-10	dB
	QPSK, CR 3/4 (18 Mbps)				-13	dB
	16-QAM, CR 1/2 (24 Mbps)				-16	dB
	16-QAM, CR 3/4 (36 Mbps)				-19	dB
	64-QAM, CR 2/3 (48 Mbps)				-22	dB
	64-QAM, CR 3/4 (54 Mbps)				-25	dB

Parameter		Condition	Min.	Typ.	Max.	Units
Minimum receive sensitivity	BPSK, CR 1/2 (6 Mbps)	PER ≤ 10 %		-90	-82	dBm
	BPSK, CR 3/4 (9 Mbps)	PER ≤ 10 %		-90	-79	dBm
	QPSK, CR 1/2 (12 Mbps)	PER ≤ 10 %		-89	-77	dBm
	QPSK, CR 3/4 (18 Mbps)	PER ≤ 10 %		-87	-74	dBm
	16-QAM, CR 1/2 (24 Mbps)	PER ≤ 10 %		-85	-70	dBm
	16-QAM, CR 3/4 (36 Mbps)	PER ≤ 10 %		-81	-66	dBm
	64-QAM, CR 2/3 (48 Mbps)	PER ≤ 10 %		-77	-65	dBm
	64-QAM, CR 3/4 (54 Mbps)	PER ≤ 10 %		-75	-64	dBm
Maximum input level		PER ≤ 10 %			-30	dBm
Adjacent channel rejection	BPSK, CR 1/2 (6 Mbps)	PER ≤ 10 %	16			dB
	64-QAM, CR 3/4 (54 Mbps)	PER ≤ 10 %	-1			dB

4.11.3 Bluetooth RF Characteristics

For module variant ENWF940[x]A1EF assume V_{DD3V3} = 3.3 V, V_{IOSD} = 3.3 V, V_{IO} = 3.3 V and T_{amb} = 25 °C, if nothing else stated.

For module variant ENWF940[x]A2EF assume V_{DD3V3} = 3.3 V, V_{DD2V2} = 2.2 V, V_{DD1V8} = 1.8 V, V_{DD1V1} = 1.1 V, V_{IOSD} = 3.3 V, V_{IO} = 3.3 V and T_{amb} = 25 °C, if nothing else stated.

50 Ω terminal load connected to the RF connector.

4.11.3.1 Receiver Section RF Characteristics

Parameter	Condition		Min.	Typ.	Max.	Units
RF frequency range			2 400		2 483.5	MHz
Interference Performance (Basic Rate) C/I Ratio	GFSK RSL = -67 dBm BER ≤ 0.1 %	C/I (Co-channel)			11	dB
		C/I (1 MHz)			0	dB
		C/I (2 MHz)			-30	dB
		C/I (3 MHz)			-40	dB
		C/I (Image)			-9	dB
		C/I (Image ± 1 MHz)			-20	dB

Parameter	Condition		Min.	Typ.	Max.	Units
Interference Performance (Enhanced Data Rate) C/I Ratio	π/4-DQPSK RSL= -67 dBm BER ≤ 0.01 %	C/I (Co-channel)			13	dB
		C/I (1 MHz)			0	dB
		C/I (2 MHz)			-30	dB
		C/I (3 MHz)			-40	dB
		C/I (Image)			-7	dB
		C/I (Image ± 1 MHz)			-20	dB
	8-DPSK RSL = -67 dBm BER ≤ 0.01 %	C/I (Co-channel)			21	dB
		C/I (1 MHz)			5	dB
		C/I (2 MHz)			-25	dB
		C/I (3 MHz)			-33	dB
		C/I (Image)			0	dB
		C/I (Image ± 1 MHz)			-13	dB
Interference Performance (Low Energy) C/I Ratio	GFSK RSL = -67 dBm BER ≤ 0.1 % 1 Mbps	C/I (Co-channel)			21	dB
		C/I (1 MHz)			15	dB
		C/I (2 MHz)			-17	dB
		C/I (3 MHz)			-27	dB
		C/I (Image)			-9	dB
		C/I (Image ± 1 MHz)			-15	dB
	GFSK RSL = -67 dBm BER ≤ 0.1 % 2 Mbps	C/I (Co-channel)			21	dB
		C/I (2 MHz)			15	dB
		C/I (3 MHz)			-17	dB
		C/I (6 MHz)			-27	dB
		C/I (Image)			-9	dB
		C/I (Image ± 2 MHz)			-15	dB
Minimum Receive Sensitivity	BR, DH1	BER ≤ 0.1 %		-94	-70	dBm
	EDR, 2DH1	BER ≤ 0.01 %		-90	-70	dBm
	LE, GFSK	BER ≤ 0.1 %		-90	-70	dBm
Out-of-band blocking (Basic Rate) Interfering Signal Power	GFSK RSL = -67 dBm BER ≤ 0.1 %	30 MHz to 2 000 MHz			-10	dB
		2 GHz to 2.399 GHz			-27	dB
		2.484 GHz to 3 GHz			-27	dB
		3 GHz to 12.75 GHz			-10	dB
Out-of-band blocking (Low Energy) Interfering Signal Power	GFSK RSL = -67 dBm BER ≤ 0.1 %	30 MHz to 2 000 MHz			-30	dB
		2 GHz to 2.399 GHz			-35	dB
		2.484 GHz to 3 GHz			-35	dB
		3 GHz to 12.75 GHz			-30	dB
RSSI Range	Resolution = 1 dB			-90	0	dB

4.11.3.2 Transmitter Section RF Characteristics

Parameter	Condition		Min.	Typ.	Max.	Units
RF frequency range			2 400		2 483.5	MHz
Maximum output power	Basic Rate (BR)			+8		dBm
	Enhanced Data Rate (EDR)			+6		dBm
	Low energy (LE)			+6		dBm
Gain range	Gain Control			30		dB
Gain resolution				0.5		dB
Spurious emission (BR) (in-band)	± 500 kHz				-20	dBc
	± 2 MHz, |M-N| = 2				-20	dBm
	± 3 MHz or greater, |M-N| ≥ 3				-40	dBm
Spurious emission (EDR) (in-band)	± 1 MHz				-26	dBc
	± 1.5 MHz				-20	dBm
	± 2.5 MHz				-40	dBm
Spurious emission (LE) (in-band)	1 Mbps	± 2 MHz, |M-N| = 2			-20	dBm
		± 3 MHz or greater, |M-N| ≥ 3			-30	dBm
	2 Mbps	± 4 MHz, |M-N| = 4			-20	dBm
		± 5 MHz, |M-N| = 5			-20	dBm
		± 6 MHz or greater, |M-N| ≥ 6			-30	dBm

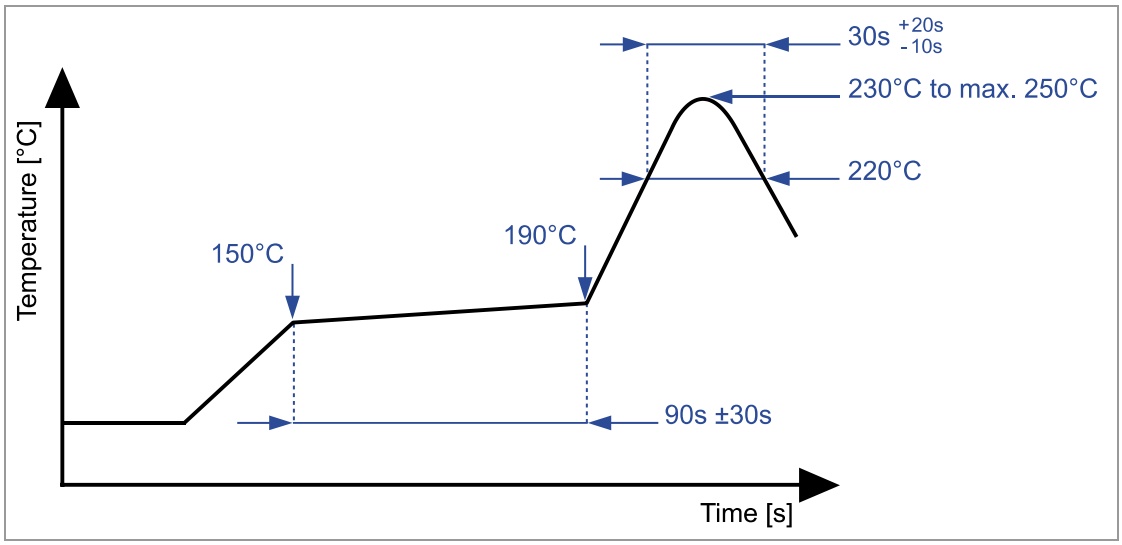
4.12 Reliability Tests

The measurement should be done after the test device has been exposed to room temperature and humidity for one hour.

No.	Item	Limit	Condition
1	Vibration test	Electrical parameter are in specification	Freq.: 10~50 Hz; Amplitude: 1.5 mm; 20 min./cycle, 1 h each of XYZ axis
2	Shock test		Dropped 3 times onto hard wood from a height of 1 m
3	Heat cycle test		-30 °C for 30 min. and 85 °C for 30 min.; each temperature 300 cycles
4	Moisture test		60 °C, 90 % RH, 300 h
5	Low temperature test		-40 °C, 300 h
6	High temp. test		85 °C, 300 h

4.13 Recommended Soldering Profile

- Reflow permissible cycles: 2
- Opposite side reflow is prohibited due to module weight
- More than 75 percent of the soldering area shall be coated by solder
- The soldering profiles should be adhered to in order to prevent electrical or mechanical damage
- Soldering profile assumes lead-free soldering



5 Cautions

Failure to follow the guidelines set forth in this document may result in degrading of the module functions and damage to the module.

5.1 Design Notes

1. Follow the conditions written in this specification, especially the control signals of this module.
2. The supply voltage should abide by the maximum ratings (⇨ 4.2 Absolute Maximum Ratings).
3. The supply voltage must be free of AC ripple voltage (for example from a battery or a low noise regulator output). For noisy supply voltages, provide a decoupling circuit (for example a ferrite in series connection and a bypass capacitor to ground of at least 47 µF directly at the module).
4. This module should not be mechanically stressed when installed.
5. Keep this module away from heat. Heat is the major cause of decreasing the life time of these modules.
6. Avoid assembly and use of the target equipment in conditions where the module temperature may exceed the maximum tolerance.
7. Keep this module away from other high frequency circuits.
8. Refer to the recommended pattern when designing a board.

5.2 Installation Notes

1. Reflow soldering is possible twice based on the conditions set forth in ⇨ 4.13 Recommended Soldering Profile. Set up the temperature at the soldering portion of this module according to this reflow profile.
2. Carefully position the module so that the heat will not burn into printed circuit boards or affect other components that are susceptible to heat.
3. Carefully locate the module, to avoid an increased temperature caused by heat generated by neighboring components.
4. If a vinyl-covered wire comes into contact with the module, the wire cover will melt and generate toxic gas, damaging the insulation. Never allow contact between a vinyl cover and these modules to occur.
5. This module should not be mechanically stressed or vibrated when reflowed.
6. To repair the board by hand soldering, follow the conditions set forth in this chapter.
7. Do not wash this product.
8. Pressing on parts of the metal cover or fastening objects to the metal will cause damage to the module.

5.3 Usage Condition Notes

1. Take measures to protect the module against static electricity.
   If pulses or transient loads (a large load, which is suddenly applied) are applied to the modules, check and evaluate their operation before assembly of the final products.
2. Do not use dropped modules.
3. Do not touch, damage, or soil the pins.
4. Follow the recommended condition ratings about the power supply applied to this module.
5. Electrode peeling strength: Do not apply a force of more than 4.9 N in any direction on the soldered module.
6. Pressing on parts of the metal cover or fastening objects to the metal cover will cause damage.
7. These modules are intended for general purpose and standard use in general electronic equipment, such as home appliances, office equipment, information, and communication equipment.

5.4 Storage Notes

1. The module should not be stressed mechanically during storage.
2. Do not store these modules in the following conditions or the performance characteristics of the module, such as RF performance will be adversely affected:

– Storage in salty air or in an environment with a high concentration of corrosive gas, such as Cl_2, H_2S, NH_3, SO_2, or NO_X,

– Storage in direct sunlight,

– Storage in an environment where the temperature may be outside the range of 5 °C to 35 °C, or where the humidity may be outside the 45 % to 85 % range,

– Storage of the modules for more than one year after the date of delivery storage period: Please check the adhesive strength of the embossed tape and soldering after 6 months of storage.

3. Keep this module away from water, poisonous gas, and corrosive gas.
4. This module should not be stressed or shocked when transported.
5. Follow the specification when stacking packed crates (max. 10).

5.5 Safety Cautions

These specifications are intended to preserve the quality assurance of products and individual components.

Before use, check and evaluate the operation when mounted on your products. Abide by these specifications without deviation when using the products. These products may short-circuit. If electrical shocks, smoke, fire, and/or accidents involving human life are anticipated when a short circuit occurs, provide the following failsafe functions as a minimum:

1. Ensure the safety of the whole system by installing a protection circuit and a protection device.
2. Ensure the safety of the whole system by installing a redundant circuit or another system to prevent a single fault causing an unsafe status.

5.6 Other Cautions

1. Do not use the module for other purposes than those listed in section ⇨ 5.3 Usage Condition Notes.
2. Be sure to provide an appropriate fail-safe function on your product to prevent any additional damage that may be caused by the abnormal function or the failure of the module.
3. This module has been manufactured without any ozone chemical controlled under the Montreal Protocol.
4. These modules are not intended for use under the special conditions shown below. Before using these modules under such special conditions, carefully check their performance and reliability under the said special conditions to determine whether or not they can be used in such a manner:

– In liquid, such as water, salt water, oil, alkali, or organic solvent, or in places where liquid may splash,
– In direct sunlight, outdoors, or in a dusty environment,
– In an environment where condensation occurs,
– In an environment with a high concentration of harmful gas (e. g. salty air, HCl, Cl_2, SO_2, H_2S, NH_3, and NO_X).

5. If an abnormal voltage is applied due to a problem occurring in other components or circuits, replace these modules with new modules, because they may not be able to provide normal performance even if their electronic characteristics and appearances appear satisfactory.

For further information please refer to the Panasonic website ⇨ 7.2.2 Product Information.

5.7 Restricted Use

5.7.1 Life Support Policy

This Panasonic Industrial Devices Europe GmbH product is not designed for use in life support appliances, devices, or systems where malfunction can reasonably be expected to result in a significant personal injury to the user, or as a critical component in any life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

Panasonic customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Panasonic Industrial Devices Europe GmbH for any damages resulting.

5.7.2 Restricted End Use

This Panasonic Industrial Devices Europe GmbH product is not designed for any restricted activity that supports the development, production, handling usage, maintenance, storage, inventory or proliferation of any weapons or military use.

Transfer, export, re-export, usage or reselling of this product to any destination, end user or any end use prohibited by the European Union, United States or any other applicable law is strictly prohibited.

6 Regulatory and Certification Information

TBD

7 Appendix

7.1 Ordering Information

Variants and Versions

Order Number	Brand Name	Description	MOQ[15]
ENWF9408A1EF[16]	PAN9028	Wi-Fi/Bluetooth radio module IEEE 802.11 a/b/g/n/ac Bluetooth/Bluetooth LE 5 with a ceramic chip-antenna, Multi-region version certified for US, EU, and CA[17]	1 000
ENWF9408A2EF[16]	PAN9028	Wi-Fi/Bluetooth radio module IEEE 802.11 a/b/g/n/ac Bluetooth/Bluetooth LE 5 with a ceramic chip-antenna, without PMIC 88PG823 and without 32 kHz crystal, Multi-region version certified for US, EU, and CA[17]	1 000
ENWF9408AXEF	PAN9028-IMX	i.MX6+PAN9028 Development Kit: 1× PAN9028 MicroSD Adapter, 1× Wandboard WBIMX6U, 1× MicroSD Card, 1× Adapter cable USB-A to DC 5.5/2.5mm plug	1
ENWF9408AWEF	PAN9028-MSD	PAN9028 MicroSD Adapter with module ENWF9408A1EF	1

[15] Abbreviation for Minimum Order Quantity (MOQ). The default MOQ for mass production is 1000 pieces, fewer only on customer demand. Samples for evaluation can be delivered at any quantity via the distribution channels.

[16] Samples are available on customer demand.

[17] The multi-region version is restricted to FCC, European ETSI, and Canadian ISED regulatory domain with blocked Tx power table, which is stored on the OTP memory of device. The device does not support the channels 12 to13 in the 2.4 GHz band. DFS and passive scanning mechanism are not necessary as only the non-DFS channels in the 5 GHz band are supported.

7.2 Contact Details

7.2.1 Contact Us

Please contact your local Panasonic Sales office for details on additional product options and services:

For Panasonic Sales assistance in the **EU**, visit
https://eu.industrial.panasonic.com/about-us/contact-us
Email: wireless@eu.panasonic.com

For Panasonic Sales assistance in **North America**, visit the Panasonic website "Sales & Support" to find assistance near you at
https://na.industrial.panasonic.com/distributors

Please visit the **Panasonic Wireless Technical Forum** to submit a question at
https://forum.na.industrial.panasonic.com

7.2.2 Product Information

Please refer to the Panasonic Wireless Connectivity website for further information on our products and related documents:

For complete Panasonic product details in the **EU**, visit
http://pideu.panasonic.de/products/wireless-modules.html

For complete Panasonic product details in **North America**, visit
http://www.panasonic.com/rfmodules