



PNTC143/114/124/144EQC-Q series

50 V, 100 mA NPN resistor-equipped transistors

Rev. 1 — 1 October 2021

Product data sheet

1. General description

100 mA NPN Resistor-Equipped Transistor (RET) family in an ultra small DFN1412D-3 (SOT8009) leadless Surface-Mounted Device (SMD) plastic package with side-wettable flanks.

Table 1. Product overview

Type number	R1	R2	Package		PNP complement:
	k Ω	k Ω	Nexperia	JEDEC	
PNTC143EQC-Q	4.7	4.7	SOT8009	MO-340CA	PNTA143EQC-Q
PNTC114EQC-Q	10	10			PNTA114EQC-Q
PNTC124EQC-Q	22	22			PNTA124EQC-Q
PNTC144EQC-Q	47	47			PNTA144EQC-Q

2. Features and benefits

- 100 mA output current capability
- Built-in resistors
- Simplifies circuit design
- Reduces component count
- Reduces pick and place costs
- Low package height of 0.5 mm
- Suitable for Automatic Optical Inspection (AOI) of solder joint
- Qualified according to AEC-Q101 and recommended for use in automotive applications

3. Applications

- Digital applications
- Cost saving alternative for BC847-Q series in digital applications
- Controlling IC inputs
- Switching loads

4. Quick reference data

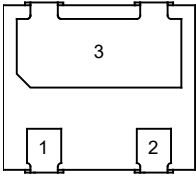
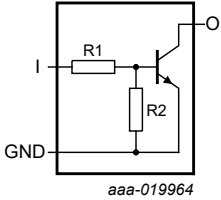
Table 2. Quick reference data

$T_{amb} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CE0}	collector-emitter voltage	open base	-	-	50	V
I_O	output current		-	-	100	mA

5. Pinning information

Table 3. Pinning

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	I	input (base)	 Transparent top view	 aaa-019964
2	GND	GND (emitter)		
3	O	output (collector)		

6. Ordering information

Table 4. Ordering information

Type number	Package		
	Name	Description	Version
PDTC143EQC-Q	DFN1412D-3	plastic leadless ultra small outline package with side-wettable flanks (SWF); 3 terminals; 0.8 mm pitch; body: 1.4 x 1.2 x 0.48 mm	SOT8009
PDTC114EQC-Q			
PDTC124EQC-Q			
PDTC144EQC-Q			

7. Marking

Table 5. Marking

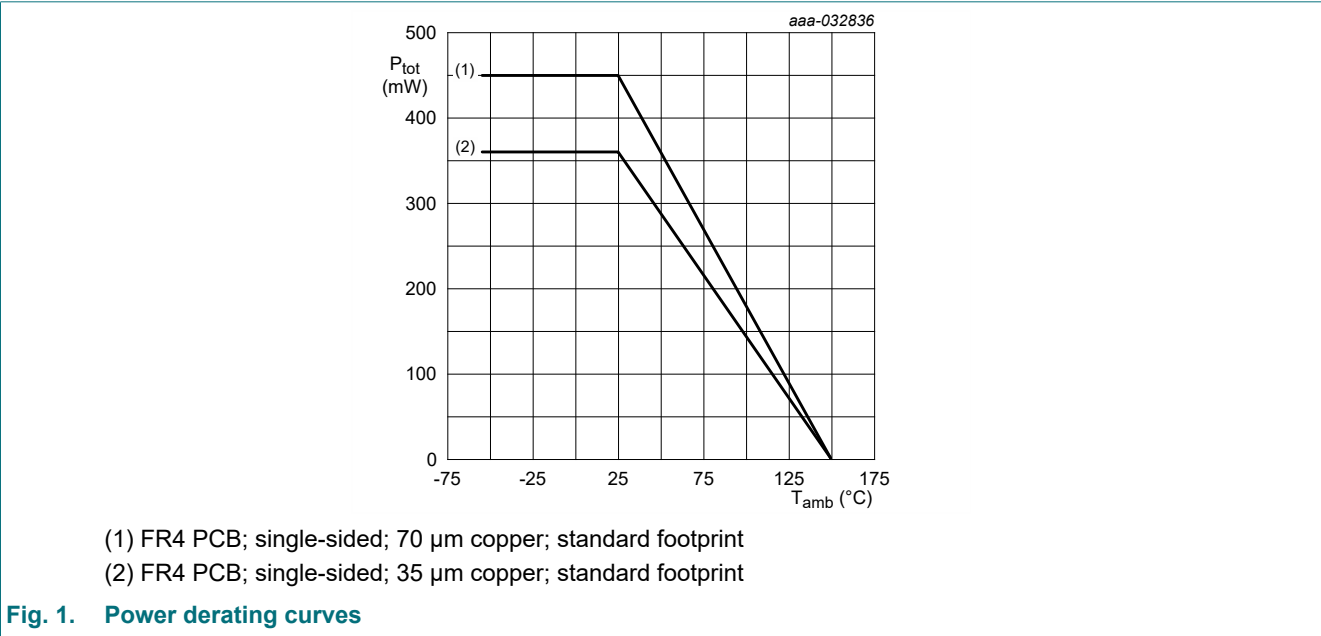
Type number	Marking code
PDTC143EQC-Q	8N
PDTC114EQC-Q	8J
PDTC124EQC-Q	8M
PDTC144EQC-Q	8R

8. Limiting values

Table 6. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134).
T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CBO}	collector-base voltage	open emitter	-	50	V
V _{CEO}	collector-emitter voltage	open base	-	50	V
V _{EBO}	emitter-base voltage	open collector	-	10	V
V _I	input voltage				
	PDTC143EQC-Q		-10	+30	V
	PDTC114EQC-Q		-10	+40	V
	PDTC124EQC-Q		-10	+40	V
	PDTC144EQC-Q		-10	+40	V
I _O	output current		-	100	mA
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C	[1] -	360	mW
			[2] -	450	mW
T _j	junction temperature		-	150	°C
T _{amb}	ambient temperature		-55	150	°C
T _{stg}	storage temperature		-65	150	°C

- [1] Device mounted on an FR4 Printed-Circuit-Board (PCB); single-sided; 35 µm copper; tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB; single-sided; 70 µm copper; tin-plated and standard footprint.



9. Thermal characteristics

Table 7. Thermal characteristics

$T_{amb} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	348	K/W
			[2]	-	-	278	K/W

- [1] Device mounted on an FR4 PCB; single-sided; 35 μm copper; tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB; single-sided; 70 μm copper; tin-plated and standard footprint.

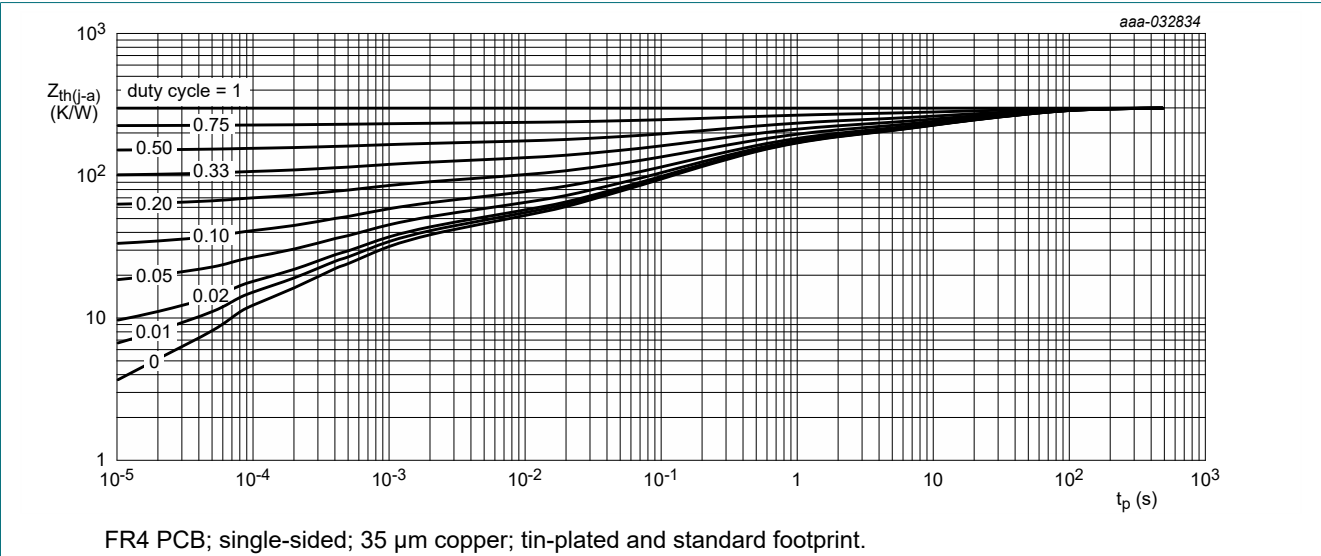


Fig. 2. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

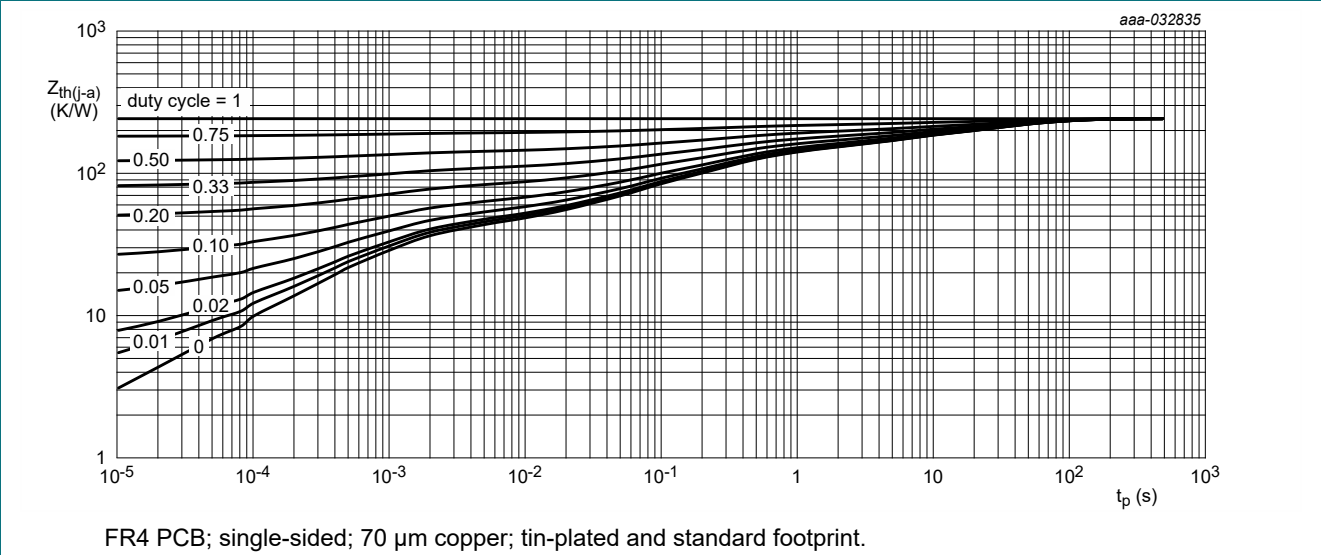


Fig. 3. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

10. Characteristics

Table 8. Characteristics

$T_{amb} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V _{(BR)CBO}	collector-base breakdown voltage	I _C = 100 μA; I _E = 0 A		50	-	-	V
V _{(BR)CEO}	collector-emitter breakdown voltage	I _C = 2 mA; I _B = 0 A		50	-	-	V
I _{CBO}	collector-base cut-off current	V _{CB} = 50 V; I _E = 0 A		-	-	100	nA
I _{CEO}	collector-emitter cut-off current	V _{CE} = 30 V; I _B = 0 A		-	-	100	nA
		V _{CE} = 30 V; I _B = 0 A; T _j = 150 °C		-	-	5	μA
I _{EBO}	emitter-base cut-off current						
	PDTC143EQC-Q	V _{EB} = 5 V; I _C = 0 A		-	-	900	μA
	PDTC114EQC-Q			-	-	400	μA
	PDTC124EQC-Q			-	-	180	μA
	PDTC144EQC-Q					90	μA
h _{FE}	DC current gain						
	PDTC143EQC-Q	V _{CE} = 5 V; I _C = 10 mA		30	-	-	
	PDTC114EQC-Q	V _{CE} = 5 V; I _C = 5 mA		30	-	-	
	PDTC124EQC-Q			60	-	-	
	PDTC144EQC-Q			80	-	-	
V _{CEsat}	collector-emitter saturation voltage	I _C = 10 mA; I _B = 0.5 mA		-	-	100	mV
V _{I(off)}	off-state input voltage						
	PDTC143EQC-Q	V _{CE} = 5 V ; I _C = 100 μA		-	1.1	0.5	V
	PDTC114EQC-Q			-	1.1	0.8	V
	PDTC124EQC-Q			-	1.1	0.8	V
	PDTC144EQC-Q			-	1.2	0.8	V
V _{I(on)}	on-state input voltage						
	PDTC143EQC-Q	V _{CE} = 0.3 V ; I _C = 20 mA		2.5	1.9	-	V
	PDTC114EQC-Q	V _{CE} = 0.3 V ; I _C = 10 mA		2.5	1.8	-	V
	PDTC124EQC-Q	V _{CE} = 0.3 V ; I _C = 5 mA		2.5	1.7	-	V
	PDTC144EQC-Q	V _{CE} = 0.3 V ; I _C = 2 mA		3.0	1.6	-	V
R1	bias resistor 1 (input)						
	PDTC143EQC-Q		[1]	3.3	4.7	6.1	kΩ
	PDTC114EQC-Q			7	10	13	kΩ
	PDTC124EQC-Q			15.4	22	28.6	kΩ
	PDTC144EQC-Q			33	47	61	kΩ
R2/R1	bias resistor ratio			0.8	1	1.2	
f _T	transition frequency	V _{CE} = 5 V; I _C = 10 mA; f = 100 MHz	[2]	-	230	-	MHz
C _c	collector capacitance	V _{CB} = 10 V; I _E = i _e = 0 A; f = 1 MHz		-	-	2.5	pF

[1] See "Section 11: Test information" for resistor calculation and test conditions

[2] Characteristics of built-in transistor

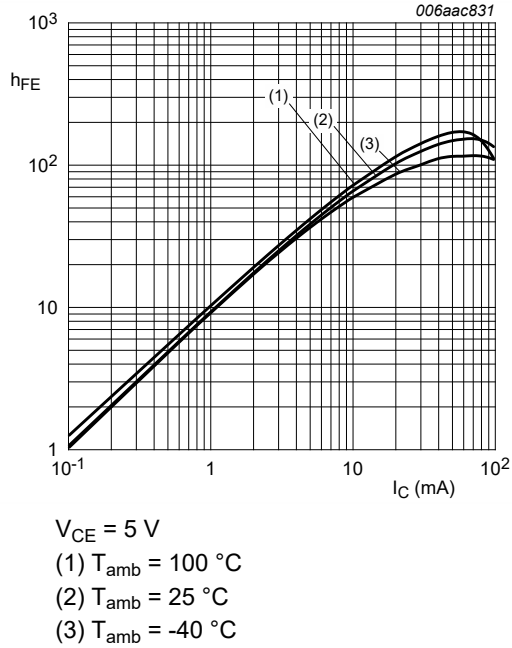


Fig. 4. PDTC143EQC-Q: DC current gain as a function of collector current; typical values

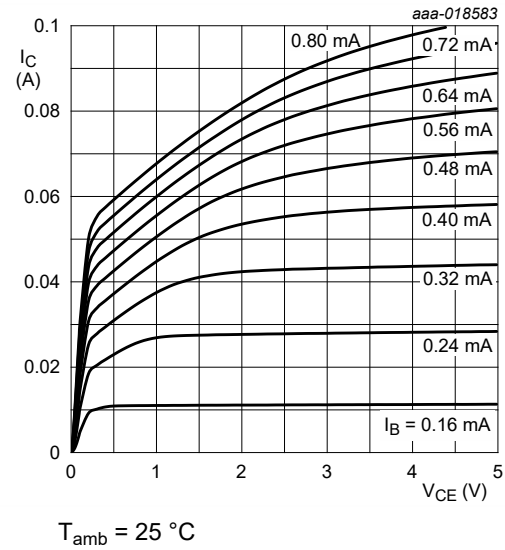


Fig. 5. PDTC143EQC-Q: Collector current as a function of collector-emitter voltage; typical values

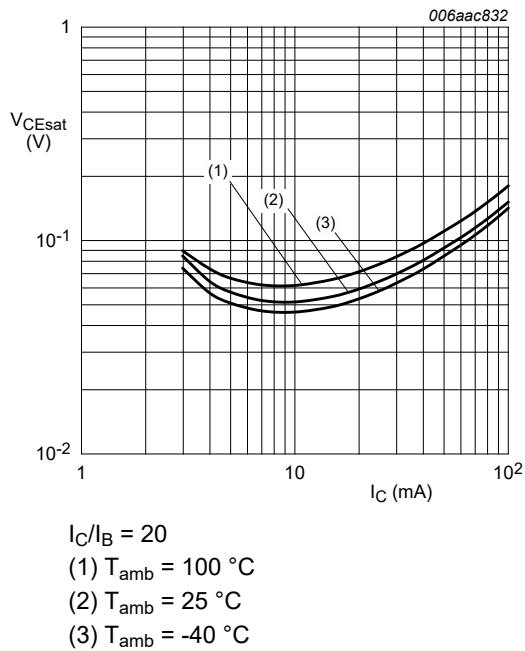


Fig. 6. PDTC143EQC-Q: Collector-emitter saturation voltage as a function of collector current; typical values

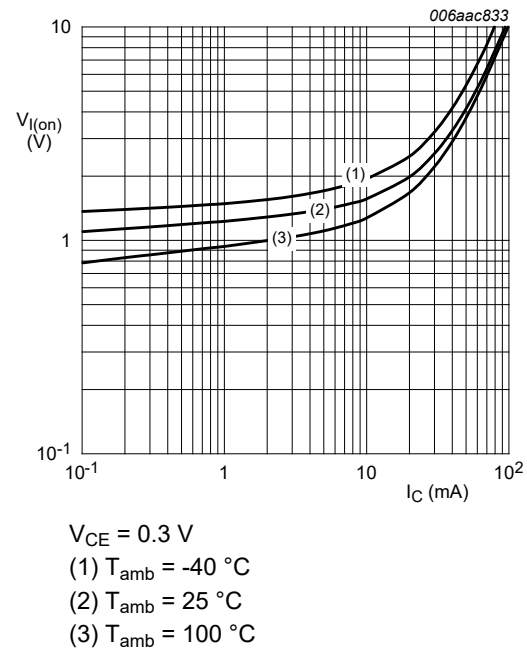


Fig. 7. PDTC143EQC-Q: On-state input voltage as a function of collector current; typical values

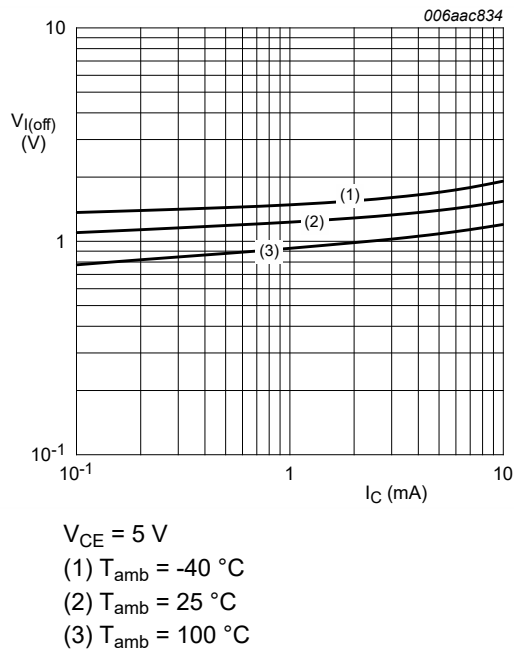


Fig. 8. PDTC143EQC-Q: Off-state input voltage as a function of collector current; typical values

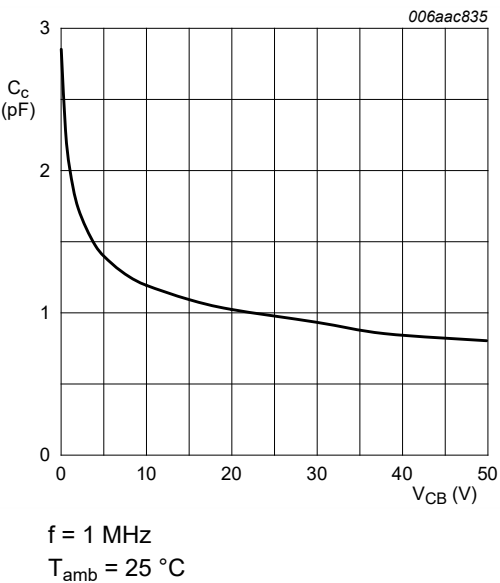


Fig. 9. PDTC143EQC-Q: Collector capacitance as a function of collector-base voltage; typical values

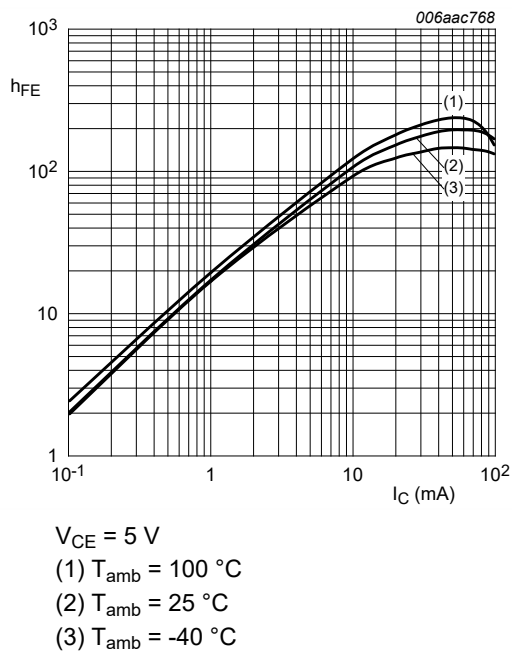


Fig. 10. PDTC114EQC-Q: DC current gain as a function of collector current; typical values

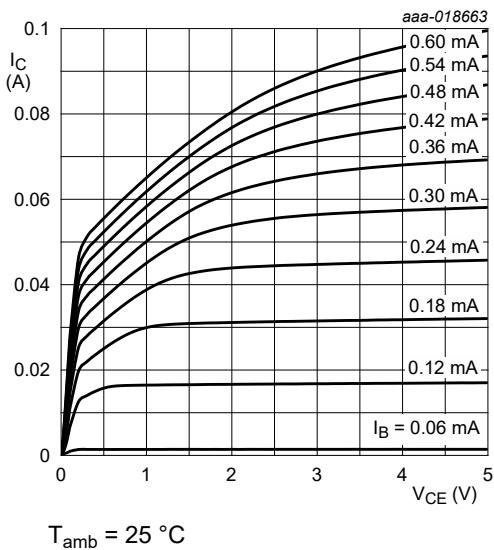


Fig. 11. PDTC114EQC-Q: Collector current as a function of collector-emitter voltage; typical values

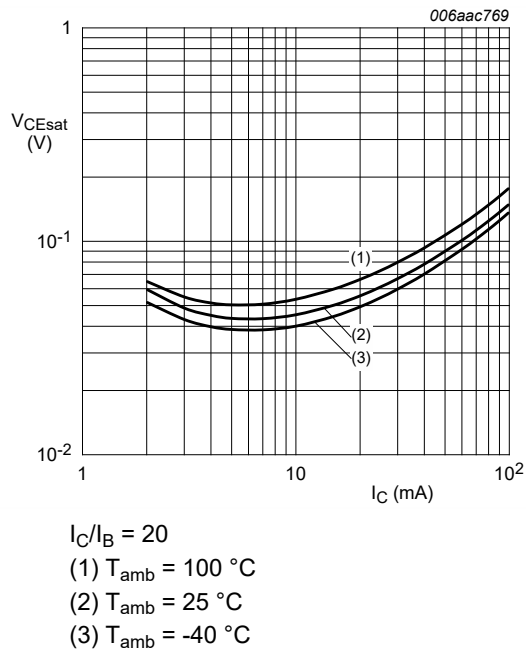


Fig. 12. PDTC114EQC-Q: Collector-emitter saturation voltage as a function of collector current; typical values

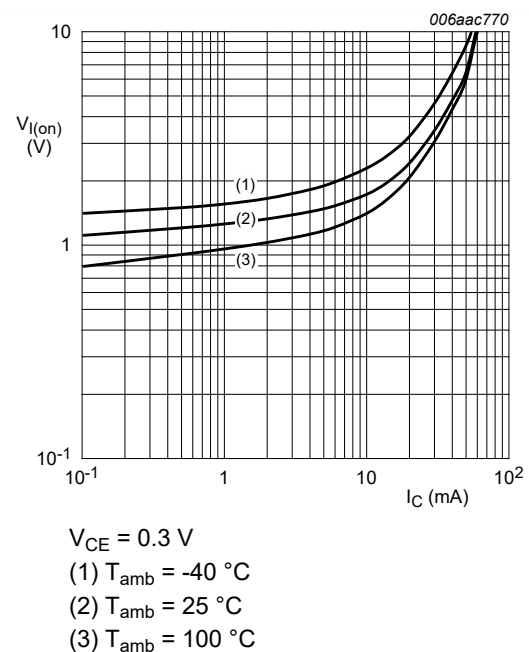


Fig. 13. PDTC114EQC-Q: On-state input voltage as a function of collector current; typical values

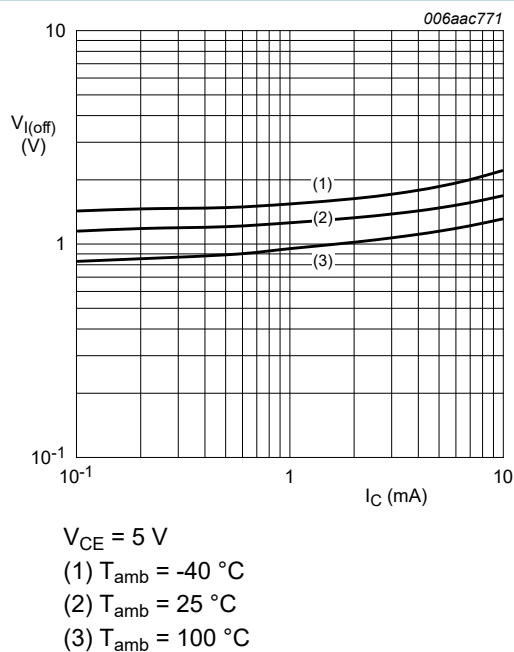


Fig. 14. PDTC114EQC-Q: Off-state input voltage as a function of collector current; typical values

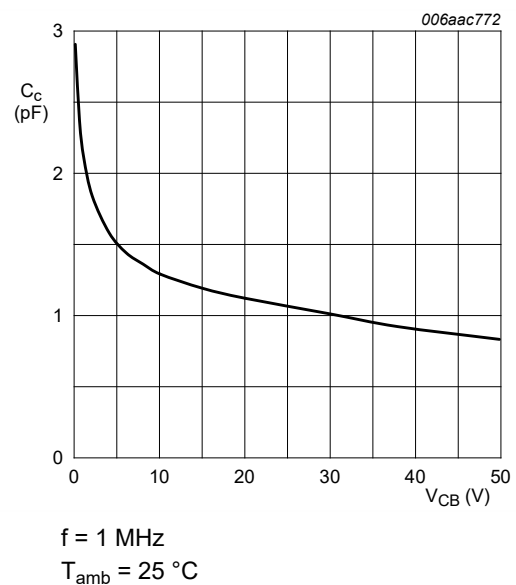


Fig. 15. PDTC114EQC-Q: Collector capacitance as a function of collector-base voltage; typical values

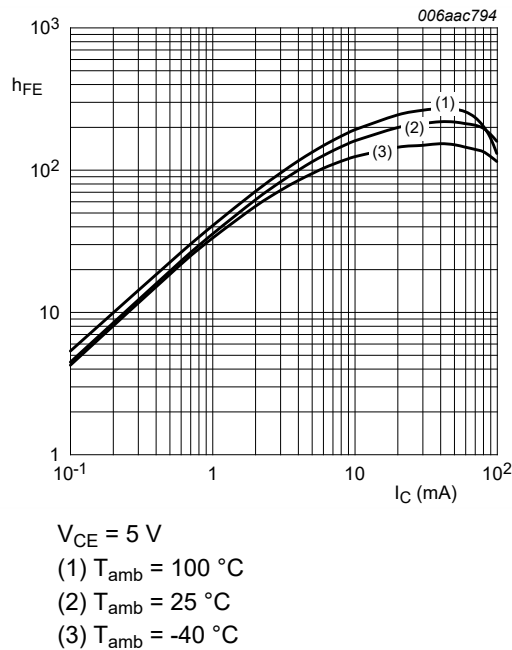


Fig. 16. PDTC124EQC-Q: DC current gain as a function of collector current; typical values

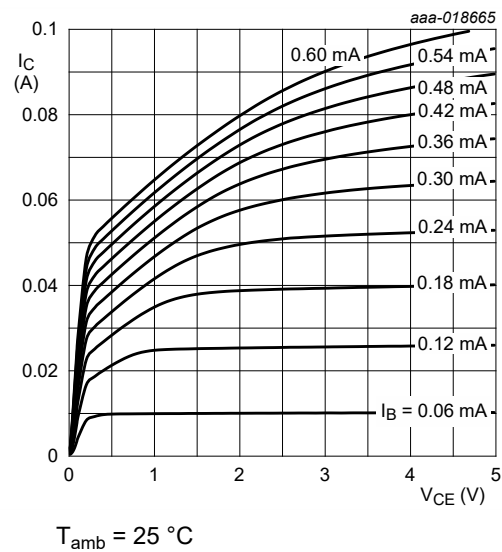


Fig. 17. PDTC124EQC-Q: Collector current as a function of collector-emitter voltage; typical values

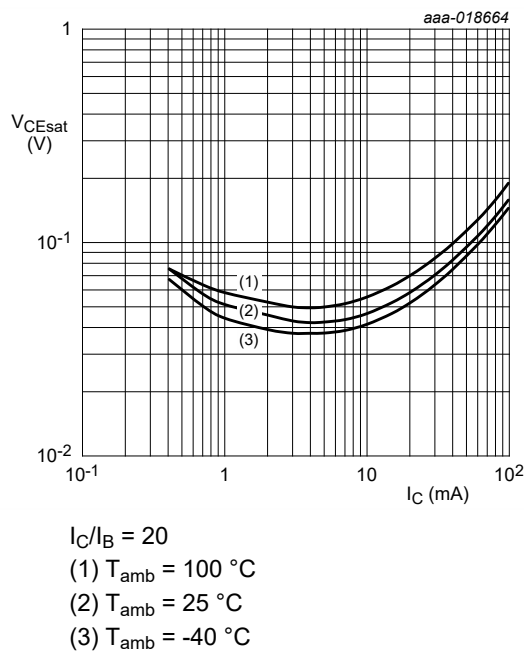


Fig. 18. PDTC124EQC-Q: Collector-emitter saturation voltage as a function of collector current; typical values

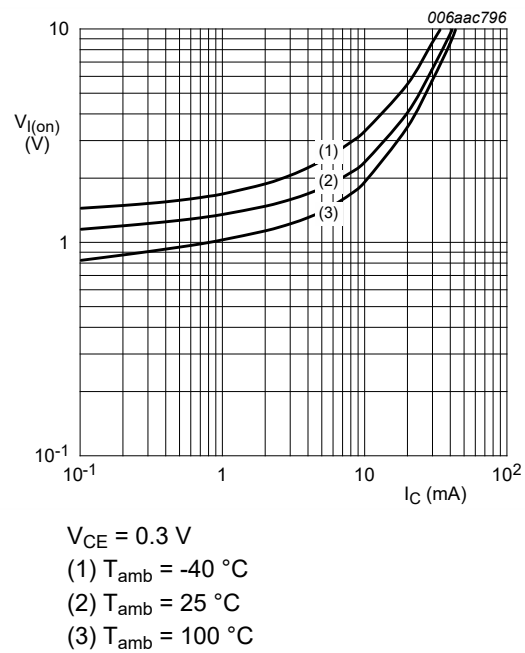


Fig. 19. PDTC124EQC-Q: On-state input voltage as a function of collector current; typical values

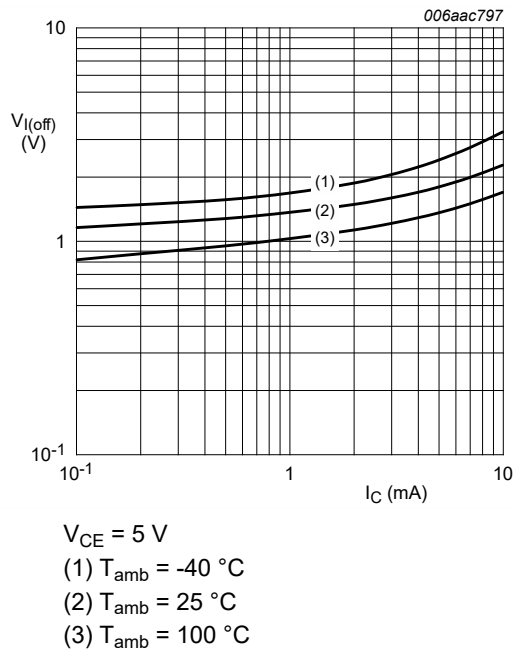


Fig. 20. PDTC124EQC-Q: Off-state input voltage as a function of collector current; typical values

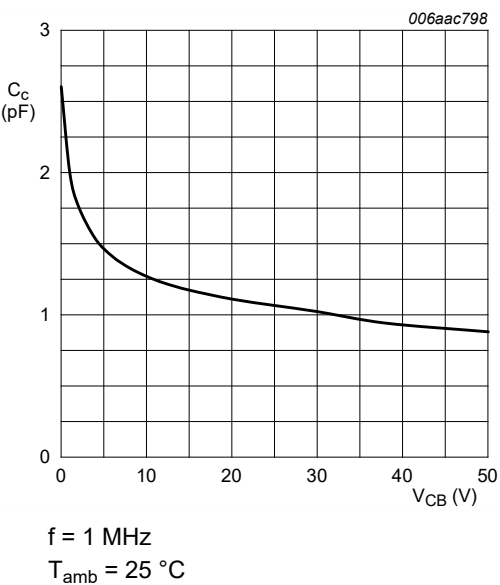


Fig. 21. PDTC124EQC-Q: Collector capacitance as a function of collector-base voltage; typical values

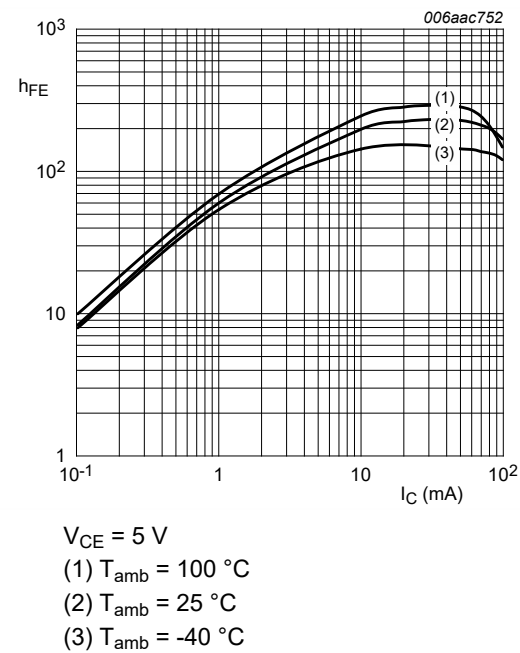


Fig. 22. PDTC144EQC-Q: DC current gain as a function of collector current; typical values

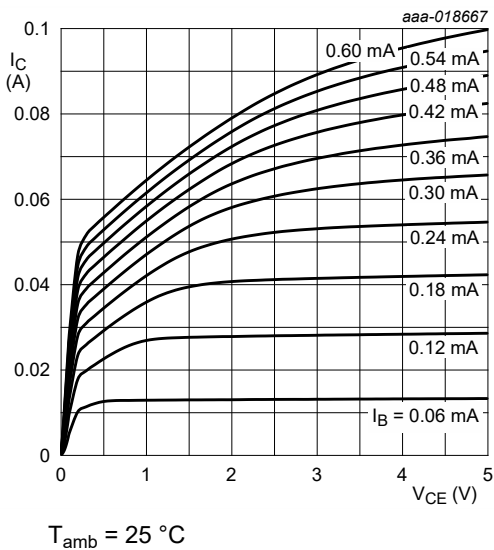


Fig. 23. PDTC144EQC-Q: Collector current as a function of collector-emitter voltage; typical values

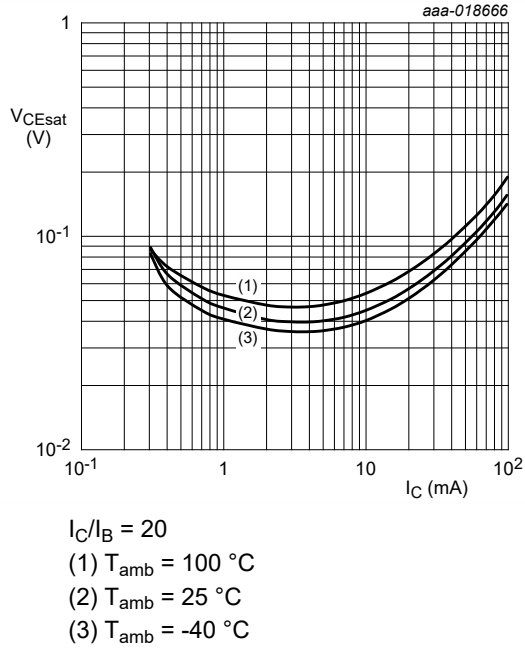


Fig. 24. PDTC144EQC-Q: Collector-emitter saturation voltage as a function of collector current; typical values

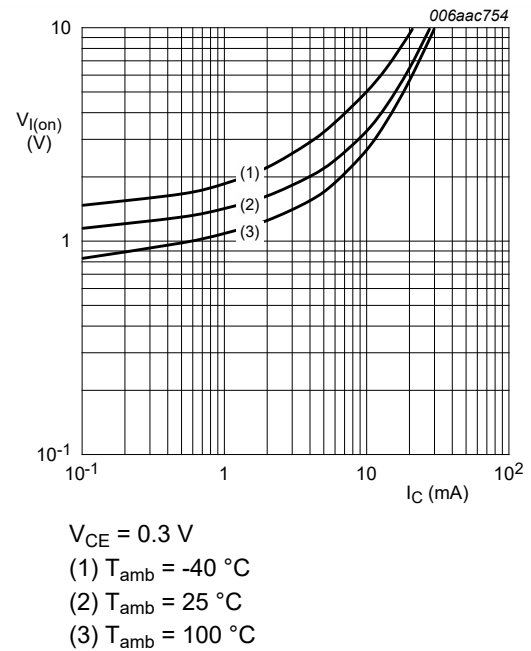


Fig. 25. PDTC144EQC-Q: On-state input voltage as a function of collector current; typical values

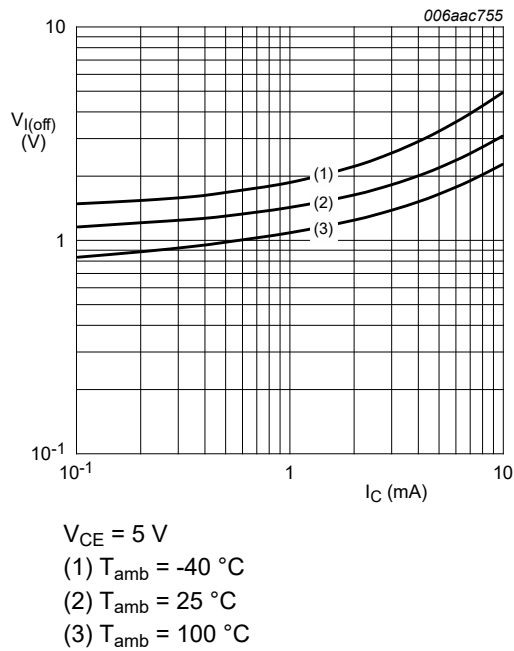


Fig. 26. PDTC144EQC-Q: Off-state input voltage as a function of collector current; typical values

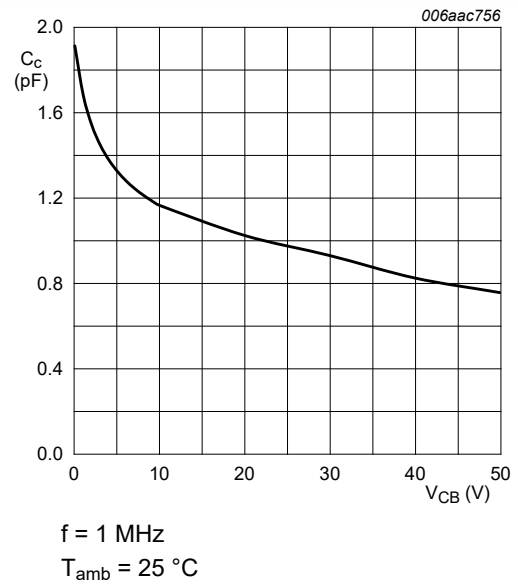
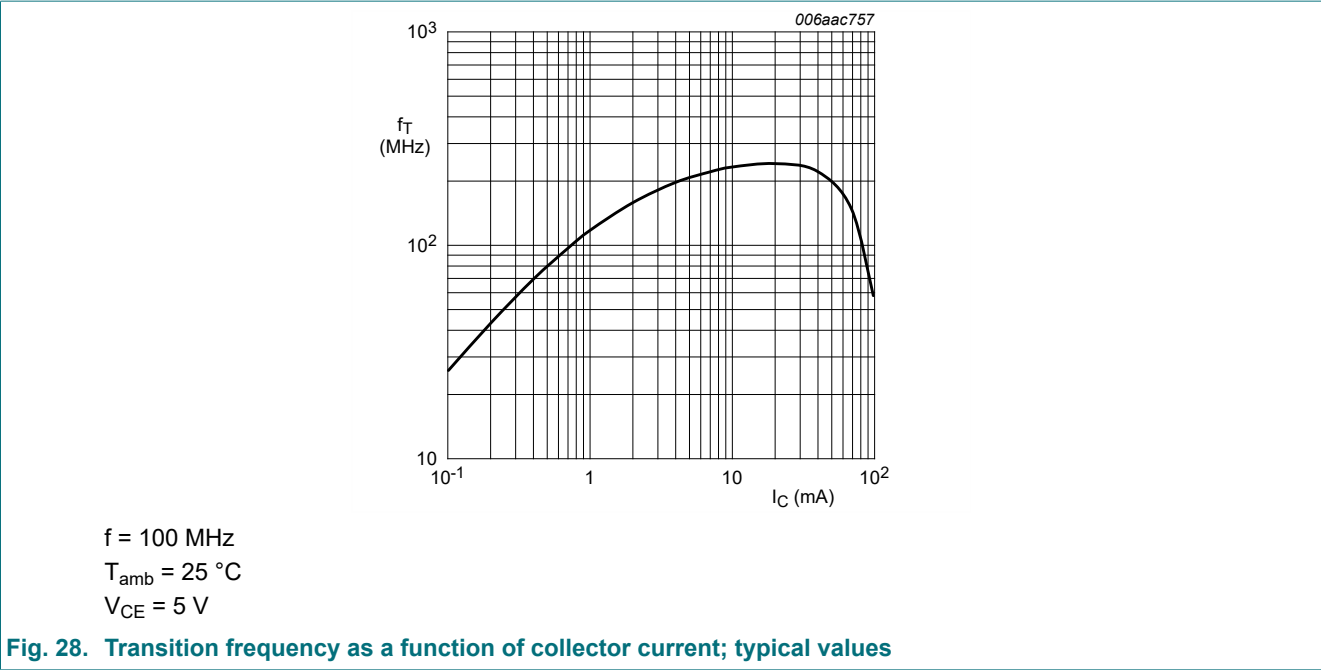


Fig. 27. PDTC144EQC-Q: Collector capacitance as a function of collector-base voltage; typical values



11. Test information

Resistor calculation

- Calculation of bias resistor 1 (R1)

$$R1 = \frac{V(I12) - V(I11)}{I12 - I11}$$
- Calculation of bias resistor ratio (R2/R1)

$$\frac{R2}{R1} = \frac{V(I14) - V(I13)}{R1 \cdot (I14 - I13)} - 1$$

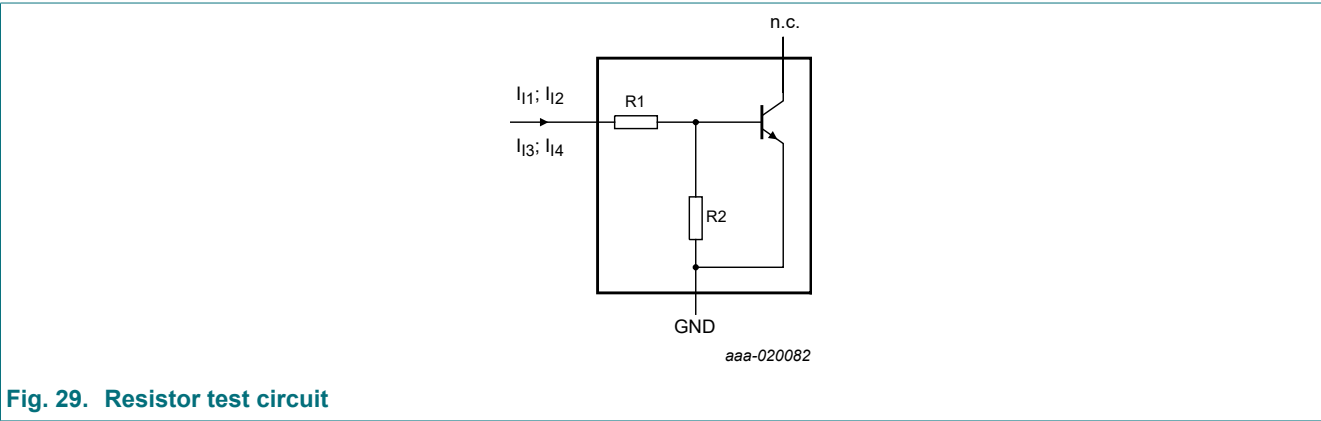


Fig. 29. Resistor test circuit

Resistor test conditions

Table 9. Resistor test conditions

Type number	R1 (kΩ)	R2 (kΩ)	Test conditions			
			I11	I12	I13	I14
PDTC143EQC-Q	4.7	4.7	600 μA	700 μA	-600 μA	-700 μA
PDTC114EQC-Q	10	10	350 μA	450 μA	-350 μA	-450 μA
PDTC124EQC-Q	22	22	150 μA	230 μA	-150 μA	-230 μA
PDTC144EQC-Q	47	47	55 μA	105 μA	-55 μA	-105 μA

11.1. Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - Stress test qualification for discrete semiconductors, and is suitable for use in automotive applications.

12. Package outline

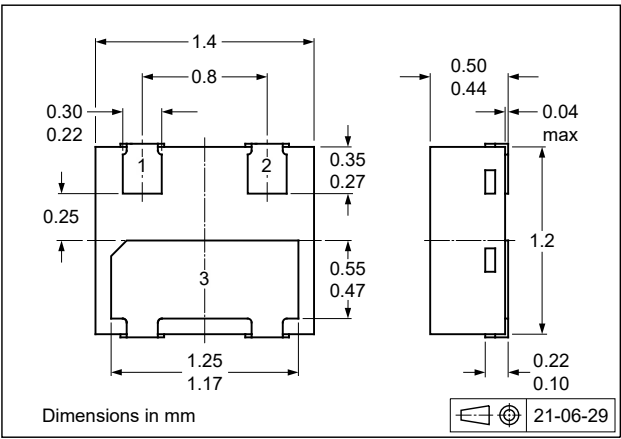


Fig. 30. Package outline DFN1412D-3 (SOT8009)

13. Soldering

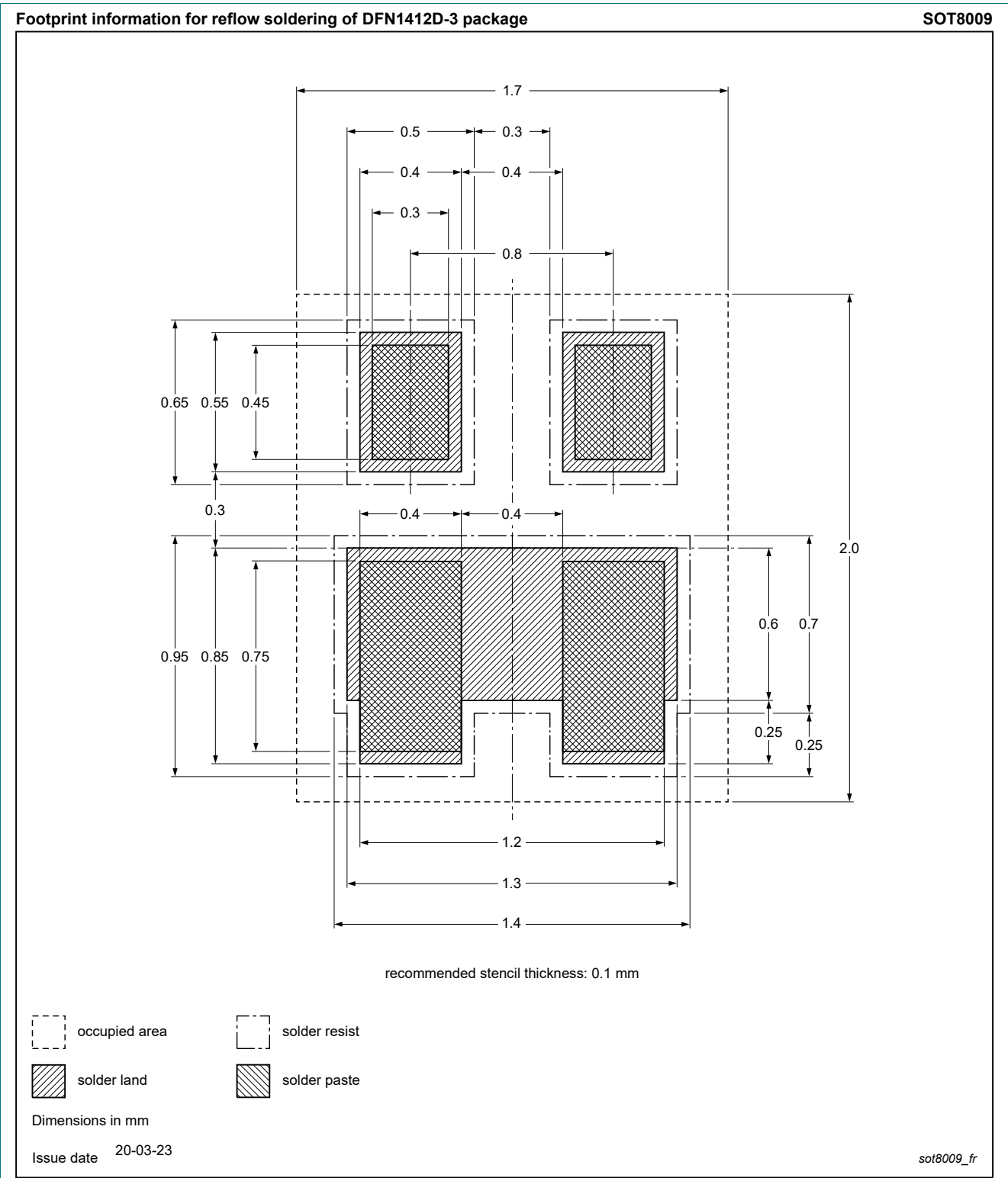


Fig. 31. Reflow soldering footprint DFN1412D-3 (SOT8009)

14. Revision history

Table 10. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PDTC143_114_124_144EQC-Q_SER v.1	20211001	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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