CRYSTAL OSCILLATOR (SPXO)

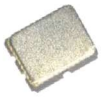
OUTPUT : LV-PECL, LVDS

Pb Free RoHS Compliant

Product Number
SG2520EGN: X1G005881xxxx15
SG2520VGN: X1G005901xxxx15

SG2520EGN
SG2520VGN

- Frequency range : 25 MHz to 500 MHz
- Supply voltage : 1.8 V Typ. (LVDS only) / 2.5 V Typ. / 3.3 V Typ.
- Frequency tolerance : ±25 × 10^{-6}, ±30 × 10^{-6}, ±50 × 10^{-6}
- Operating temperature : -40 °C to +85 °C, -40 °C to +105 °C
- Function : Output enable (OE) or Standby ($\overline{ST}$)
- Phase jitter : 50 fs Max. (fo = 491.52 MHz)



(2.5 × 2.0 × 0.74 mm)

Specifications (characteristics)

Item	Symbol	Specifications			Conditions / Remarks	
		LV-PECL	LVDS			
		SG2520EGN	SG2520VGN			
Output frequency range	fo	25 MHz to 500 MHz			Please contact us for available frequencies.	
Supply voltage	V_{CC}	C: 3.3 V ± 5 % D: 2.5 V ± 5 %		E: 1.8 V ± 5 %		
Storage temperature	T_stg	-55 °C to +125 °C				
Operating temperature	T_use	G: -40 °C to +85 °C, H: -40 °C to +105 °C				
Frequency tolerance	f_tol	D: ±25 × 10^{-6} Max.			Includes initial frequency tolerance, frequency / temperature characteristics, frequency / voltage coefficient and 10 years aging (+25 °C)	
		E: ±30 × 10^{-6} Max.				
		J: ±50 × 10^{-6} Max.				
Current consumption	I_{CC}	60 mA Max.	–		OE or $\overline{ST}$ = V_{CC}, L_ECL = 50 Ω	
		–	25 mA / 30 mA / 25 mA Max.	25 mA / – / 25 mA Max.	25 MHz ≤ fo < 212 MHz	OE or $\overline{ST}$ = V_{CC}, Output option: A / B / C
			28 mA / 35 mA / 28 mA Max.	–	212 MHz ≤ fo < 392 MHz	
			28 mA / 35 mA / 30 mA Max.	–	392 MHz ≤ fo ≤ 500 MHz	
Disable current	I_dis	35 mA Max.	20 mA Max.		OE = GND	
Stand-by current	I_std	30 µA Max.			$\overline{ST}$ = GND, T_use Max. = +85 °C	
		60 µA Max.			$\overline{ST}$ = GND, T_use Max. = +105 °C	
Symmetry	SYM	45 % to 55 %			At output crossing point	
Output voltage (LV-PECL)	V_{OH}	V_{CC} - 1.1 V Min.	–		Output option: A, DC characteristic	
	V_{OL}	V_{CC} - 1.5 V Max.				
Differential swing	V_{SW}	0.8 V to 2.0 V	500 mV to 900 mV	500 mV to 900 mV	Output option: A	
		–	800 mV to 1 600 mV	–	Output option: B	
		–	600 mV to 1 200 mV	600 mV to 1 200 mV	Output option: C	
Output voltage (LVDS)	V_{OD}	–	250 mV to 450 mV	250 mV to 450 mV	Output option: A	Differential output voltage, V_{OD1}, V_{OD2}
			400 mV to 800 mV	–	Output option: B	
			300 mV to 600 mV	300 mV to 600 mV	Output option: C	
	dV_{OD}	–	50 mV Max.		dV_{OD} = | V_{OD1} - V_{OD2} |	
	V_{OS}	–	1.15 V to 1.35 V	0.65 V to 0.85 V	Offset voltage, V_{OS1}, V_{OS2}	
	dV_{OS}	–	50 mV Max.		dV_{OS} = | V_{OS1} - V_{OS2} |	
Output load condition	L_ECL	50 Ω	–		Terminated to V_{CC} - 2.0 V	
	L_LVDS	–	100 Ω		Connected between OUT and $\overline{OUT}$	
Input voltage	V_{IH} V_{IL}	70 % V_{CC} Min. 30 % V_{CC} Max.			OE or $\overline{ST}$ terminal	
Rise/Fall times	tr/tf	0.35 ns Max.			LV-PECL: 20 % - 80 % (V_{OH} - V_{OL}) LVDS: 20 % - 80 % differential output peak to peak	
Start-up time	t_str	10 ms Max.			t = 0 at 90 % V_{CC}	
Phase jitter	t_{PJ}	250 fs Max.	250 fs Max.	400 fs Max.	25 MHz ≤ fo < 100 MHz	Offset frequency fo < 50 MHz: 12 kHz to 5 MHz fo ≥ 50 MHz: 12 kHz to 20 MHz
		90 fs Max.	100 fs Max.	130 fs Max.	100 MHz ≤ fo ≤ 156 MHz	
		70 fs Max.	60 fs Max.	70 fs Max.	156 MHz < fo ≤ 212 MHz	
		60 fs Max.	50 fs Max.	60 fs Max.	212 MHz < fo ≤ 391 MHz	
		50 fs Max.	50 fs Max.	60 fs Max.	391 MHz < fo ≤ 500 MHz	

Product Name (Standard form): SG2520 EGN 156.250000MHz C D H P Z A
① ② ③ ④⑤⑥⑦⑧⑨

①Model ②Output (E: LV-PECL, V: LVDS) ③Frequency ④Supply voltage ⑤Frequency tolerance ⑥Operating temperature ⑦Function ⑧Output disable type (Z: High impedance) ⑨Output option

④Supply voltage	
C	3.3 V Typ.
D	2.5 V Typ.
E*	1.8 V Typ.

* "E" is only for SG2520VGN

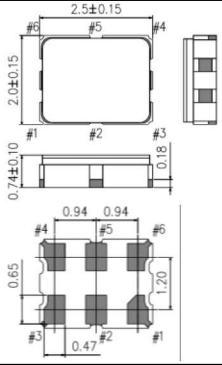
⑤Freq. tolerance	
D	±25 × 10^{-6}
E	±30 × 10^{-6}
J	±50 × 10^{-6}

⑥Operating temp.	
G	-40 °C to +85 °C
H	-40 °C to +105 °C

⑦Function	
P	OE
S	$\overline{ST}$

⑨Output option		
	SG2520EGN	SG2520VGN
A	Default	V_{SW} = 500 mV to 900 mV
B	-	V_{SW} = 800 mV to 1 600 mV
C	-	V_{SW} = 600 mV to 1 200 mV

External dimensions (Unit:mm)

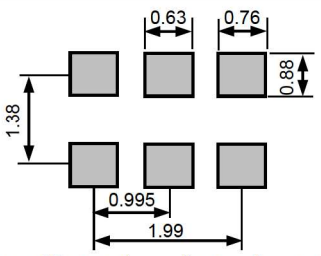


Pin map

Pin	Connection
1	OE
2	N.C. (Open or V_{CC})
3	GND
4	OUT
5	$\overline{OUT}$
6	V_{CC}

Note:
OE pin = HIGH or "Open": Specified frequency output.
OE pin = LOW: Output is high impedance

Footprint (Recommended) (Unit:mm)



In order to achieve optimum jitter performance, it is recommended that 0.1 µF and 10 µF bypass capacitors should be connected between V_{CC} and GND and placed as close to the V_{CC} pin as possible.

PROMOTION OF ENVIRONMENTAL MANAGEMENT SYSTEM CONFORMING TO INTERNATIONAL STANDARDS

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All of our major manufacturing and non-manufacturing sites, in Japan and overseas, completed the acquisition of ISO 14001 certification.

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	►Designed for automotive applications such as Car Multimedia, Body Electronics, Remote Keyless Entry etc.
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