

AUTOMOTIVE N-Channel 40V 175°C MOSFET

FEATURES

- AEC-Q101 Qualified
- 100% UIS and R_g Tested
- 175°C Operating Junction Temperature
- Wettable Flank Package
- RoHS Compliant
- Halogen-free according to IEC 61249-2-21

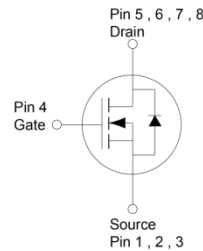
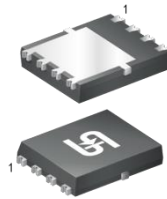
APPLICATIONS

- 12V Automotive Systems
- Solenoid and Motor Control
- Automotive Transmission Control
- DC-DC Converters

PRODUCT SUMMARY		
PARAMETER	VALUE	UNIT
V _{DS}	40	V
R _{DS(on)} (max)	V _{GS} = 10V	15
	V _{GS} = 7V	21
Q _g	20	nC



PDFN56U



Note: MSL 1 (Moisture Sensitivity Level) per J-STD-020

ABSOLUTE MAXIMUM RATINGS (T _A = 25°C unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V _{DS}	40	V
Gate-Source Voltage	V _{GS}	±20	V
Continuous Drain Current ^(Note 1)	I _D	T _C = 25°C	41
		T _A = 25°C	10
Pulsed Drain Current	I _{DM}	164	A
Single Pulse Avalanche Current ^(Note 2)	I _{AS}	16	A
Single Pulse Avalanche Energy ^(Note 2)	E _{AS}	38	mJ
Total Power Dissipation	P _D	T _C = 25°C	56
		T _C = 125°C	19
Total Power Dissipation	P _D	T _A = 25°C	3.1
		T _A = 125°C	1
Operating Junction and Storage Temperature Range	T _J , T _{STG}	- 55 to +175	°C

THERMAL RESISTANCE			
PARAMETER	SYMBOL	MAXIMUM	UNIT
Thermal Resistance – Junction to Case	R _{θJC}	2.7	°C/W
Thermal Resistance – Junction to Ambient	R _{θJA}	48	°C/W

Thermal Performance Note: R_{θJA} is the sum of the junction-to-case and case-to-ambient thermal resistances. The case-thermal reference is defined at the solder mounting surface of the drain pins. R_{θJC} is guaranteed by design while R_{θCA} is determined by the user's board design. The R_{θJA} limit presented here is based on mounting on a 1 in² pad of 2 oz copper.

ELECTRICAL CHARACTERISTICS (T _A = 25°C unless otherwise noted)						
PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Static						
Drain-Source Breakdown Voltage	V _{GS} = 0V, I _D = 250μA	BV _{DSS}	40	--	--	V
Gate Threshold Voltage	V _{GS} = V _{DS} , I _D = 250μA	V _{GS(TH)}	1.8	2.5	3.8	V
Gate-Source Leakage Current	V _{GS} = ±20V, V _{DS} = 0V	I _{GSS}	--	--	±100	nA
Drain-Source Leakage Current	V _{GS} = 0V, V _{DS} = 40V	I _{DSS}	--	--	1	μA
	V _{GS} = 0V, V _{DS} = 40V T _J = 125°C		--	--	100	
	V _{GS} = 0V, V _{DS} = 40V T _J = 175°C		--	--	500	
Drain-Source On-State Resistance (Note 3)	V _{GS} = 10V, I _D = 10A	R _{DS(on)}	--	9	15	mΩ
	V _{GS} = 10V, I _D = 10A, T _J = 125°C		--	16	26	
	V _{GS} = 10V, I _D = 10A, T _J = 175°C		--	20	33	
	V _{GS} = 7V, I _D = 8A		--	10	21	
Forward Transconductance (Note 3)	V _{DS} = 10V, I _D = 10A	g _{fs}	--	38	--	S
Dynamic (Note 4)						
Total Gate Charge	V _{GS} = 10V, V _{DS} = 20V, I _D = 10A	Q _g	--	20	--	nC
Total Gate Charge	V _{GS} = 7V, V _{DS} = 20V, I _D = 8A	Q _g	--	15	--	
Gate-Source Charge		Q _{gs}	--	5.4	--	
Gate-Drain Charge		Q _{gd}	--	4.7	--	
Input Capacitance	V _{GS} = 0V, V _{DS} = 20V, f = 1.0MHz	C _{iss}	--	1044	--	pF
Output Capacitance		C _{oss}	--	122	--	
Reverse Transfer Capacitance		C _{rss}	--	64	--	
Gate Resistance	f = 1.0MHz	R _g	0.8	2.5	5	Ω
Switching (Note 4)						
Turn-On Delay Time	V _{GS} = 10V, V _{DS} = 20V, I _D = 10A, R _G = 2Ω	t _{d(on)}	--	5	--	ns
Rise Time		t _r	--	6	--	
Turn-Off Delay Time		t _{d(off)}	--	14	--	
Fall Time		t _f	--	5	--	
Source-Drain Diode						
Diode Forward Voltage (Note 3)	V _{GS} = 0V, I _S = 10A	V _{SD}	--	--	1.2	V
Reverse Recovery Time	I _S = 10A,	t _{rr}	--	14	--	ns
Reverse Recovery Charge	di/dt = 100A/μs	Q _{rr}	--	7	--	nC

Notes:

- Silicon limited current only.
- $L = 0.3\text{mH}$, $V_{GS} = 10\text{V}$, $V_{DD} = 25\text{V}$, $R_G = 50\Omega$, $I_{AS} = 16\text{A}$, Starting $T_J = 25^\circ\text{C}$
- Pulse test: Pulse Width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$.
- Switching time is essentially independent of operating temperature.

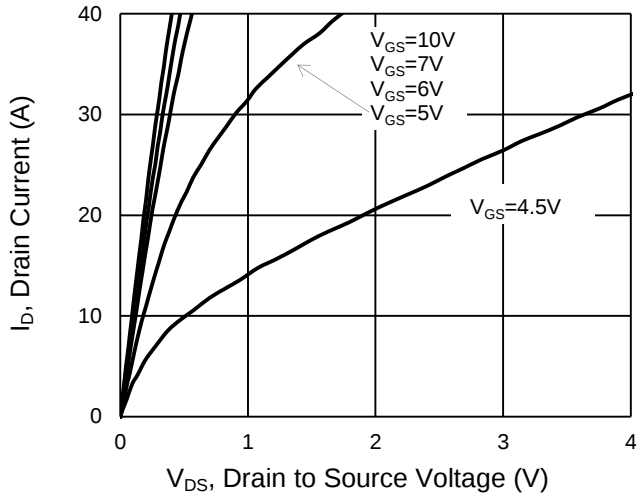
ORDERING INFORMATION

ORDERING CODE	PACKAGE	PACKING
TQM150NB04CR RLG	PDFN56U	2,500pcs / 13" Reel

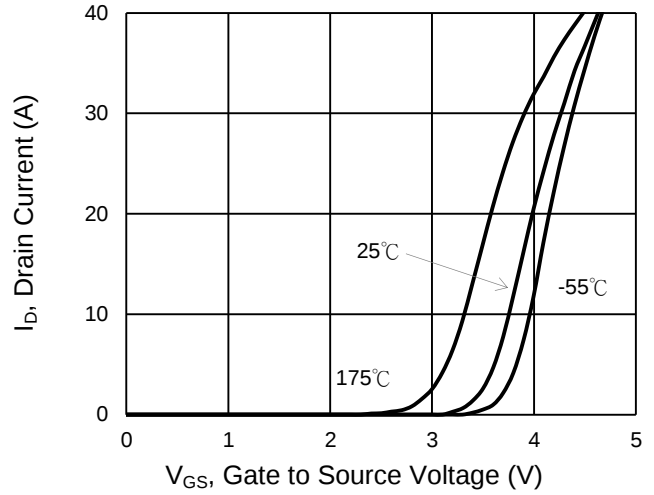
CHARACTERISTICS CURVES

($T_A = 25^\circ\text{C}$ unless otherwise noted)

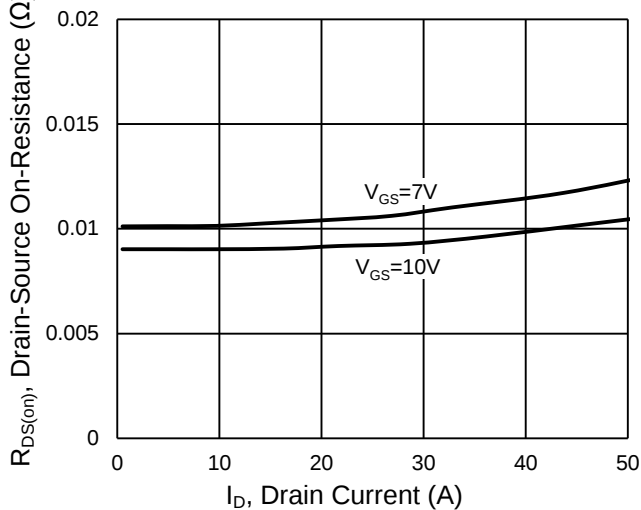
Output Characteristics



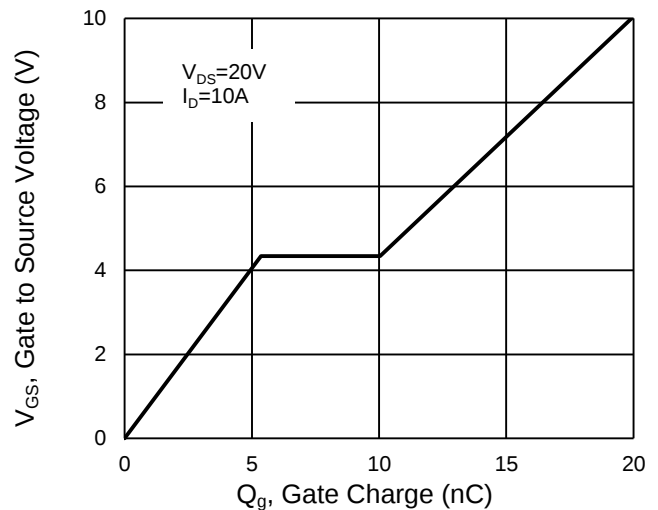
Transfer Characteristics



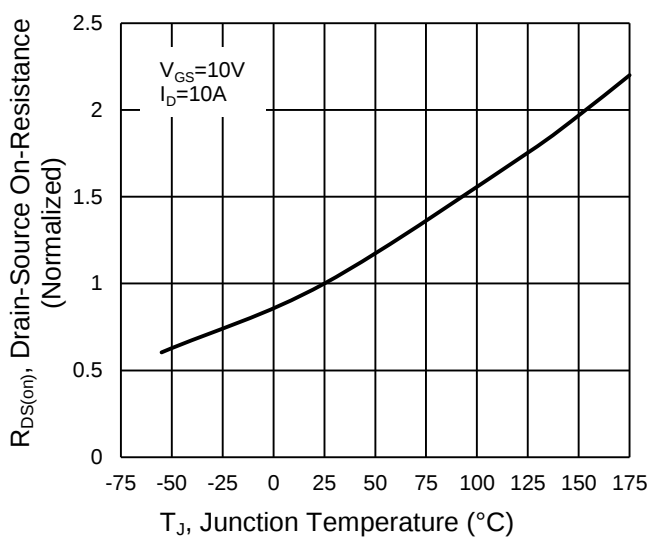
On-Resistance vs. Drain Current



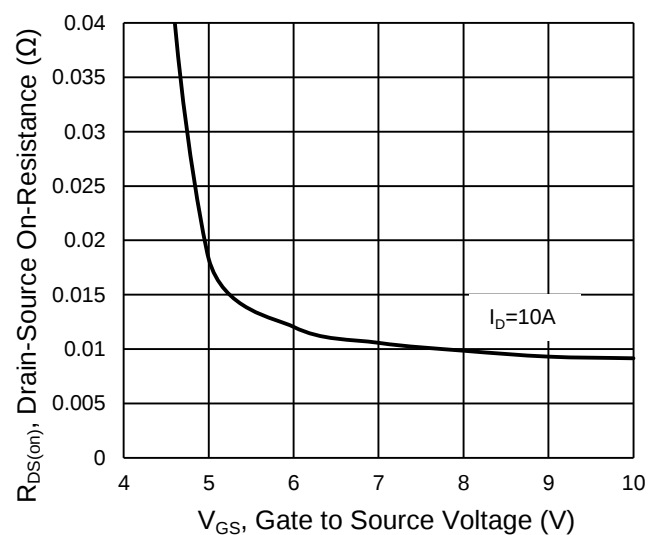
Gate-Source Voltage vs. Gate Charge



On-Resistance vs. Junction Temperature

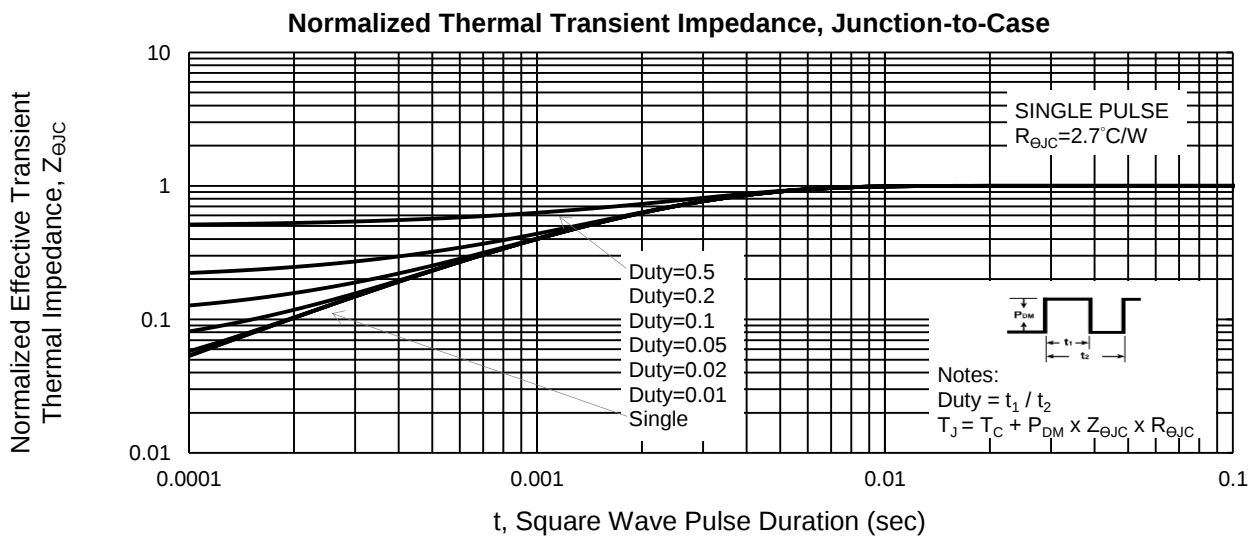
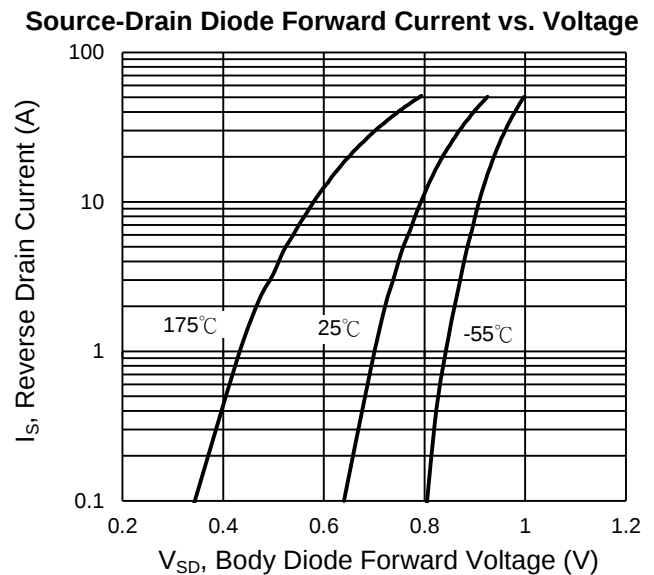
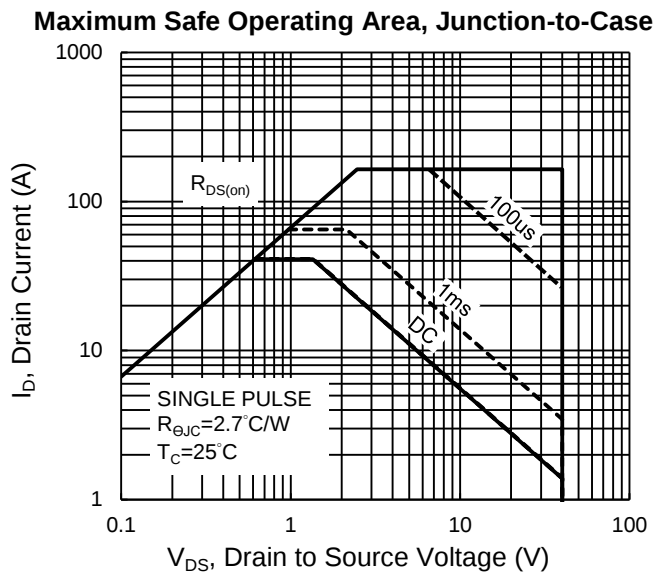
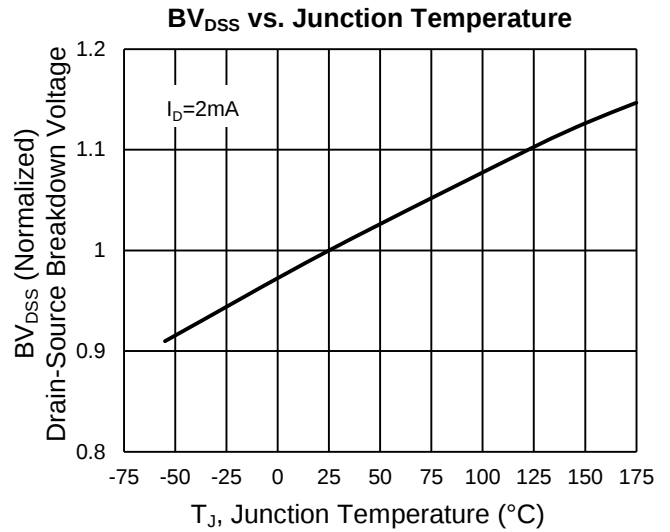
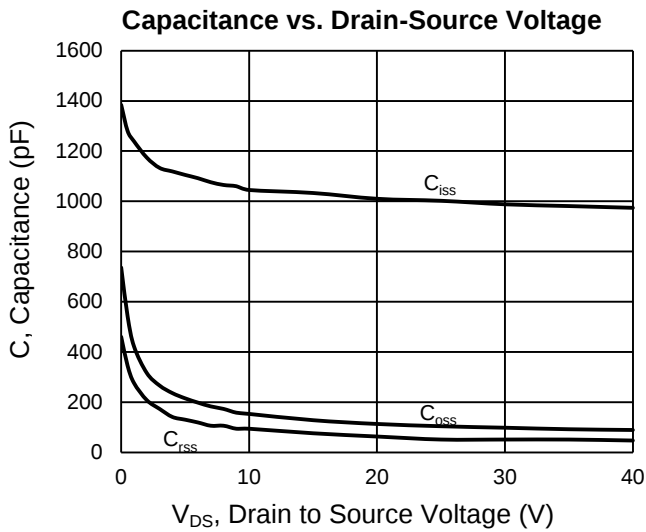


On-Resistance vs. Gate-Source Voltage



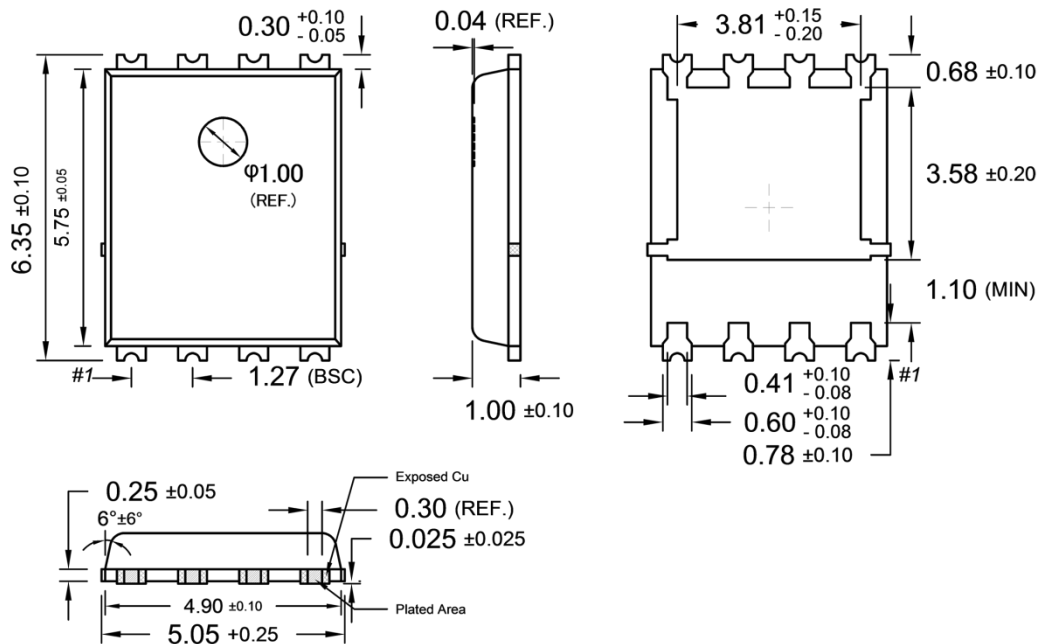
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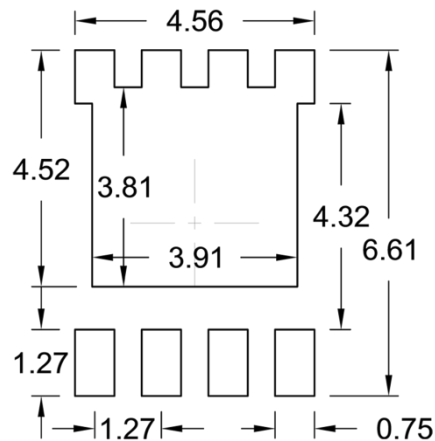


PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)

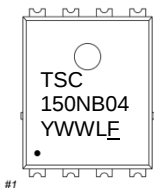
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SUGGESTED PAD LAYOUT (Unit: Millimeters)



MARKING DIAGRAM



- Y** = Year Code
- WW** = Week Code (01~52)
- L** = Lot Code (1~9, A~Z)
- F** = Factory Code
- = AEC-Q101 Qualified

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