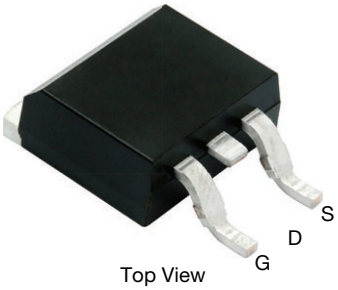
# N-Channel 200 V (D-S) 175 °C MOSFET




TO-263

Top View

## FEATURES

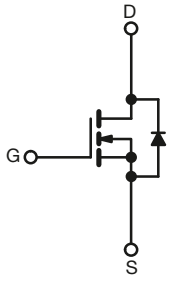
- ThunderFET® power MOSFET
- Maximum 175 °C junction temperature
- 100 % $R_g$ and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

RoHS COMPLIANT

HALOGEN FREE

## APPLICATIONS

- Power supplies:
  - Uninterruptible power supplies
  - AC/DC switch-mode power supplies
  - Lighting
- Synchronous rectification
- DC/DC converter
- Motor drive switch
- DC/AC inverter
- Solar micro inverter
- Class D audio amplifier




N-Channel MOSFET

| PRODUCT SUMMARY | |
|---|---|
| $V_{DS}$ (V) | 200 |
| $R_{DS(on)}$ max. (Ω) at $V_{GS}$ = 10 V | 0.0150 |
| $R_{DS(on)}$ max. (Ω) at $V_{GS}$ = 7.5 V | 0.0165 |
| $Q_g$ typ. (nC) | 58 |
| $I_D$ (A) | 90 |
| Configuration | Single |

| ORDERING INFORMATION | |
|---|---|
| Package | TO-263 |
| Lead (Pb)-free and halogen-free | SUM90142E-GE3 |

**ABSOLUTE MAXIMUM RATINGS** ($T_A$ = 25 °C, unless otherwise noted)

| PARAMETER | | SYMBOL | LIMIT | UNIT |
|---|---|---|---|---|
| Drain-source voltage | | $V_{DS}$ | 200 | V |
| Gate-source voltage | | $V_{GS}$ | ± 20 | |
| Continuous drain current | $T_C$ = 25 °C | $I_D$ | 90 | A |
| | $T_C$ = 125 °C | | 52 | |
| Pulsed drain current (t = 100 µs) | | $I_{DM}$ | 240 | |
| Continuous source-drain diode current | | $I_S$ | 90 | |
| Single pulse avalanche current [a] | L = 0.1 mH | $I_{AS}$ | 60 | |
| Single pulse avalanche energy [a] | | $E_{AS}$ | 180 | mJ |
| Maximum power dissipation | $T_C$ = 25 °C | $P_D$ | 375 [b] | W |
| | $T_C$ = 125 °C | | 125 [b] | |
| Operating junction and storage temperature range | | $T_J$, $T_{stg}$ | -55 to +175 | °C |
| Soldering recommendations (peak temperature) [c] | | | 260 | |

**THERMAL RESISTANCE RATINGS**

| PARAMETER | | SYMBOL | MAXIMUM | UNIT |
|---|---|---|---|---|
| Maximum junction-to-ambient (PCB mount) [c] | | $R_{thJA}$ | 40 | °C/W |
| Maximum junction-to-case (drain) | Steady state | $R_{thJC}$ | 0.4 | |

**Notes**

a. Duty cycle ≤ 1 %.
b. See SOA curve for voltage derating.
c. When mounted on 1" square PCB (FR4 material).
d. Package limited.

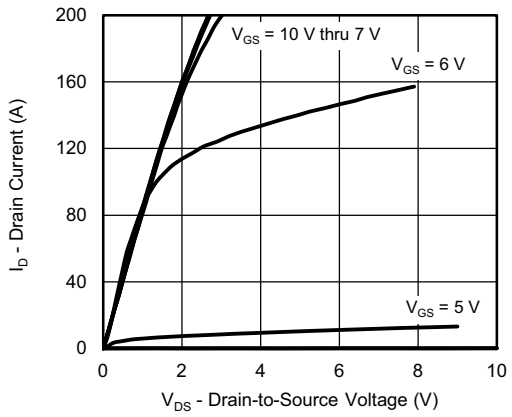
| **SPECIFICATIONS** ($T_J$ = 25 °C, unless otherwise noted) | | | | | | |
|---|---|---|---|---|---|---|
| **PARAMETER** | **SYMBOL** | **TEST CONDITIONS** | **MIN.** | **TYP.** | **MAX.** | **UNIT** |
| **Static** | | | | | | |
| Drain-source breakdown voltage | $V_{DS}$ | $V_{GS}$ = 0 V, $I_D$ = 250 µA | 200 | - | - | V |
| Gate-source threshold voltage | $V_{GS(th)}$ | $V_{DS}$ = $V_{GS}$ , $I_D$ = 250 µA | 2 | - | 4 | V |
| Gate-source leakage | $I_{GSS}$ | $V_{DS}$ = 0 V, $V_{GS}$ = ± 20 V | - | - | 250 | nA |
| Zero gate voltage drain current | $I_{DSS}$ | $V_{DS}$ = 200 V, $V_{GS}$ = 0 V | - | - | 1 | µA |
| | | $V_{DS}$ = 200 V, $V_{GS}$ = 0 V, $T_J$ = 125 °C | - | - | 150 | |
| | | $V_{DS}$ = 200 V, $V_{GS}$ = 0 V, $T_J$ = 175 °C | - | - | 5 | mA |
| On-state drain current [a] | $I_{D(on)}$ | $V_{DS}$ ≥ 10 V, $V_{GS}$ = 10 V | 60 | - | - | A |
| Drain-source on-state resistance [a] | $R_{DS(on)}$ | $V_{GS}$ = 10 V, $I_D$ = 30 A | - | 0.0123 | 0.0150 | Ω |
| | | $V_{GS}$ = 7.5 V, $I_D$ = 30 A | - | 0.0130 | 0.0165 | |
| Forward transconductance [a] | $g_{fs}$ | $V_{DS}$ = 15 V, $I_D$ = 30 A | - | 63 | - | S |
| **Dynamic [b]** | | | | | | |
| Input capacitance | $C_{iss}$ | $V_{DS}$ = 100 V, $V_{GS}$ = 0 V, f = 1 MHz | - | 3120 | - | pF |
| Output capacitance | $C_{oss}$ | | - | 280 | - | |
| Reverse transfer capacitance | $C_{rss}$ | | - | 24 | - | |
| Total gate charge | $Q_g$ | $V_{DS}$ = 100 V, $V_{GS}$ = 10 V, $I_D$ = 60 A | - | 58 | 87 | nC |
| Gate-source charge | $Q_{gs}$ | | - | 17.6 | - | |
| Gate-drain charge | $Q_{gd}$ | | - | 17.2 | - | |
| Output charge | $Q_{oss}$ | $V_{DS}$ = 100 V, $V_{GS}$ = 0 V | - | 108 | 162 | |
| Gate resistance | $R_g$ | f = 1 MHz | 1.5 | 3 | 5 | Ω |
| Turn-on delay time | $t_{d(on)}$ | $V_{DD}$ = 100 V, $R_L$ = 1.66 Ω, $I_D$ ≅ 60 A, $V_{GEN}$ = 10 V, $R_g$ = 1 Ω | - | 14 | 28 | ns |
| Rise time | $t_r$ | | - | 125 | 250 | |
| Turn-off delay time | $t_{d(off)}$ | | - | 27 | 54 | |
| Fall time | $t_f$ | | - | 80 | 150 | |
| **Drain-Source Body Diode Characteristics** | | | | | | |
| Pulse diode forward current (t = 100 µs) | $I_{SM}$ | | - | - | 240 | A |
| Body diode voltage | $V_{SD}$ | $I_F$ = 30 A, $V_{GS}$ = 0 V | - | 0.85 | 1.5 | V |
| Body diode reverse recovery time | $t_{rr}$ | $I_F$ = 30 A, dI/dt = 100 A/µs | - | 150 | 300 | ns |
| Body diode reverse recovery charge | $Q_{rr}$ | | - | 0.9 | 1.8 | nC |
| Reverse recovery fall time | $t_a$ | | - | 125 | - | ns |
| Reverse recovery rise time | $t_b$ | | - | 25 | - | |
| Body diode peak reverse recovery charge | $I_{RM(REC)}$ | | - | 11.5 | 20 | A |

**Notes**

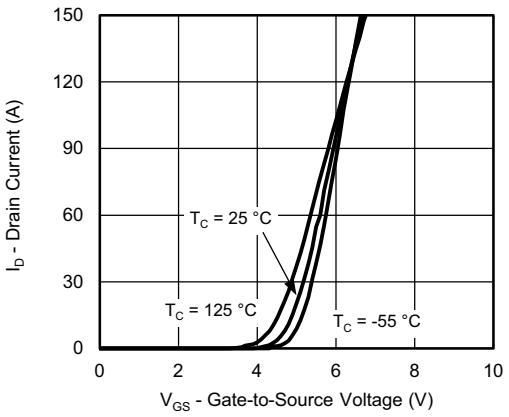
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.
c. Independent of operating temperature.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

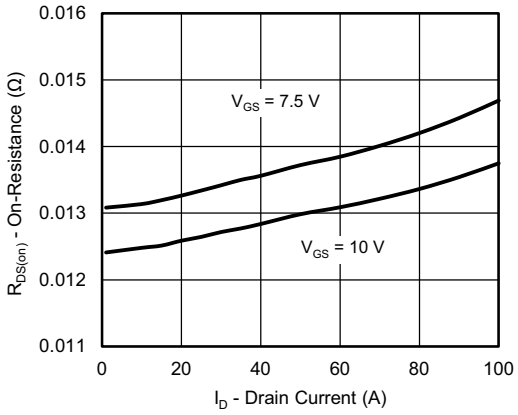
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



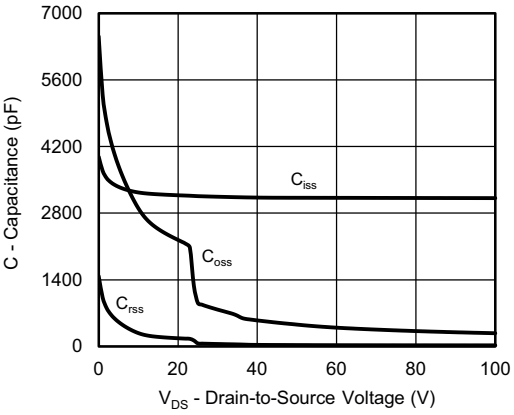

**Output Characteristics**



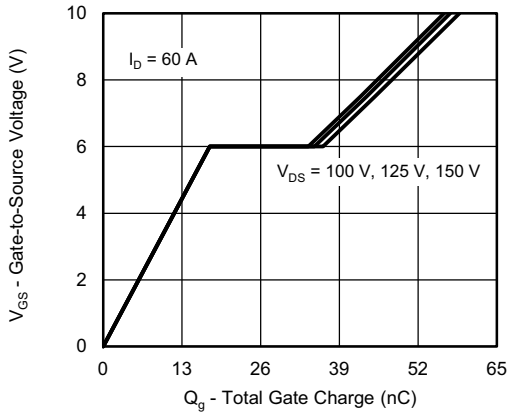

**Transfer Characteristics**



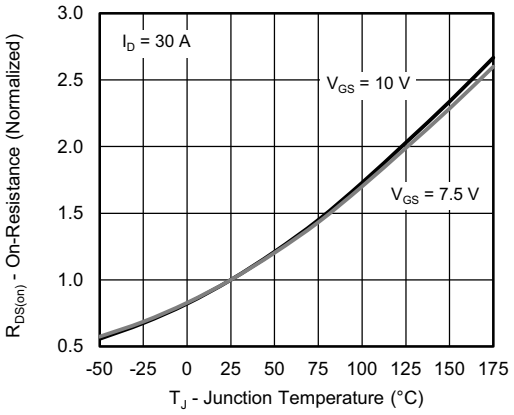

**On-Resistance vs. Drain Current and Gate Voltage**




**Capacitance**

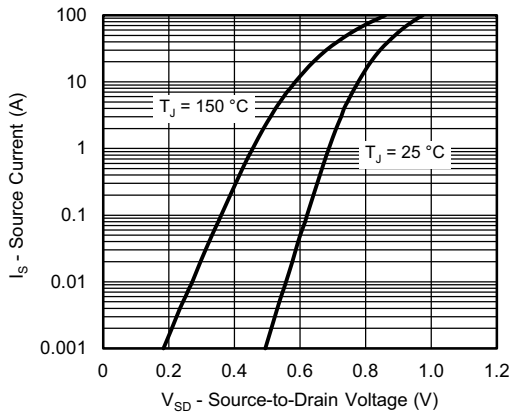



**Gate Charge**

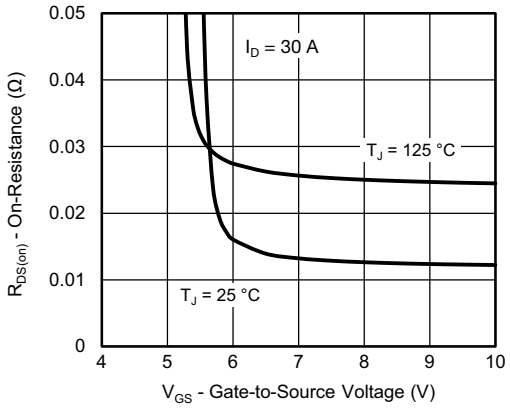



**On-Resistance vs. Junction Temperature**

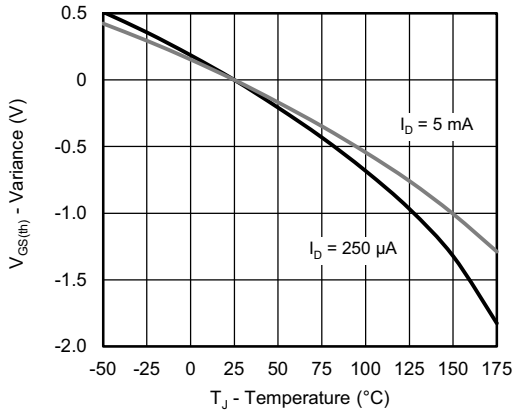
## TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



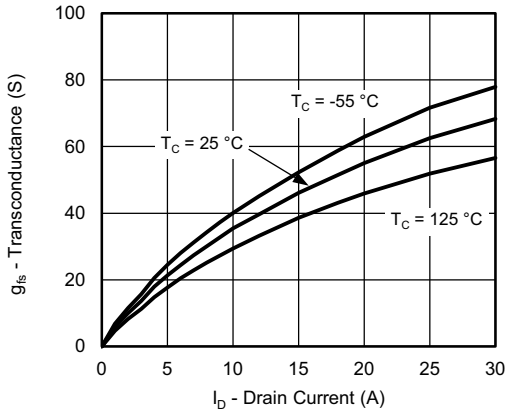

**Source-Drain Diode Forward Voltage**



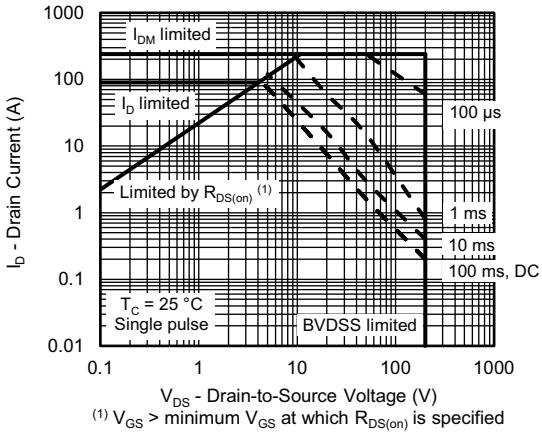

**On-Resistance vs. Gate-to-Source Voltage**




**Threshold Voltage**

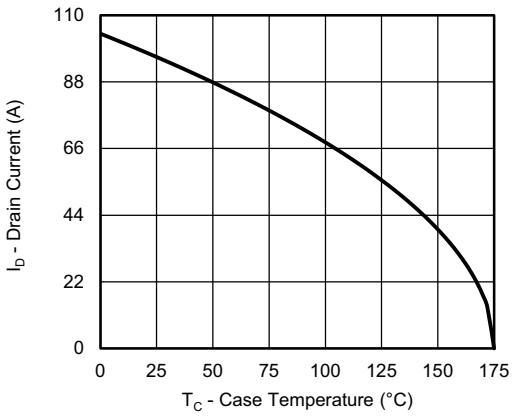



**Transconductance**

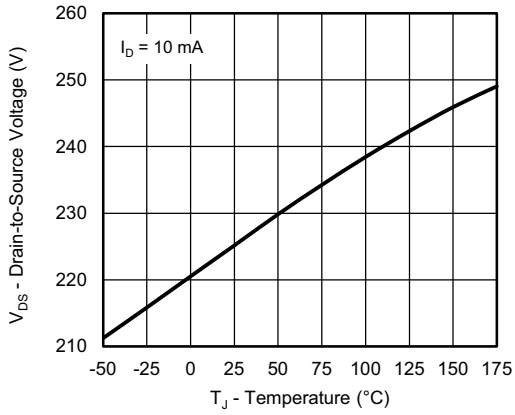



**Safe Operating Area, Junction-to-Ambient**

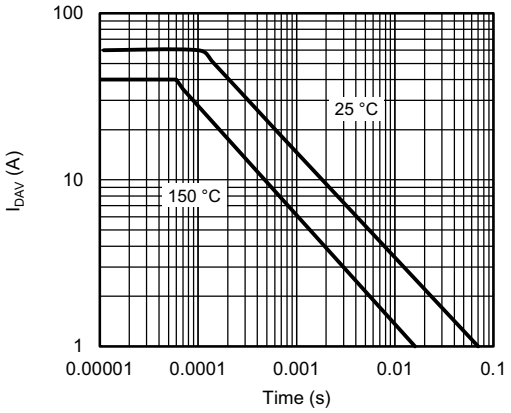
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)




**Current Derating** [a]




**Drain Source Breakdown vs. Junction Temperature**

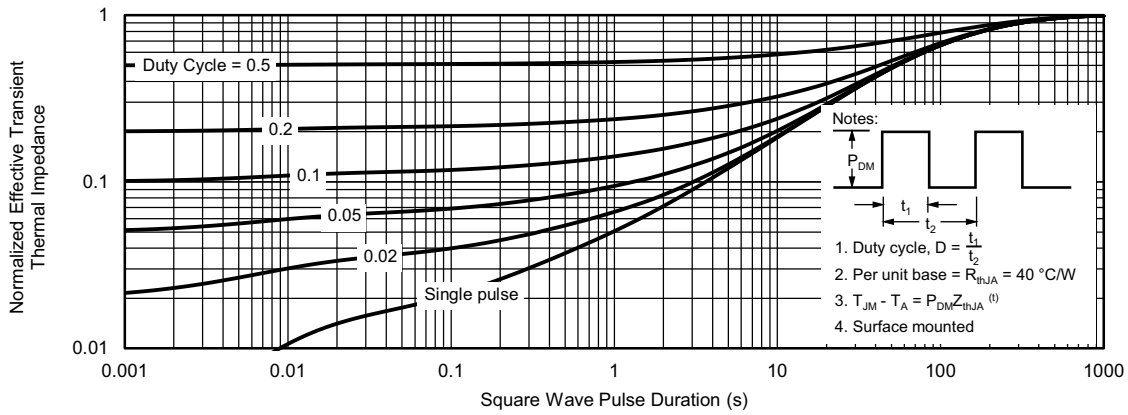



**$I_{DAV}$ vs. Time**

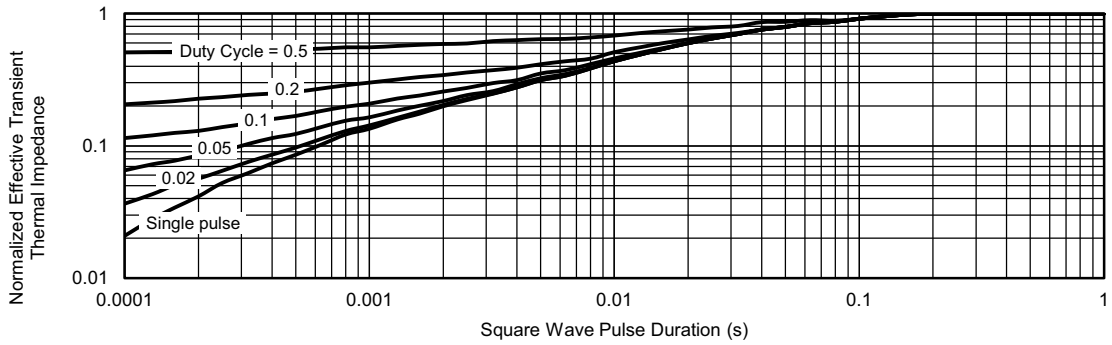
**Note**

a. The power dissipation $P_D$ is based on $T_J$ max. = 25 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)




**Normalized Thermal Transient Impedance, Junction-to-Ambient**

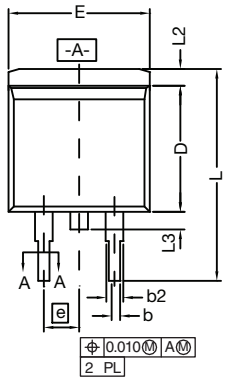


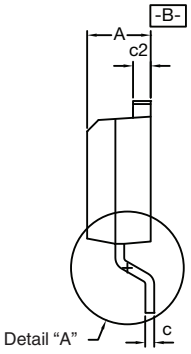

**Normalized Thermal Transient Impedance, Junction-to-Case**

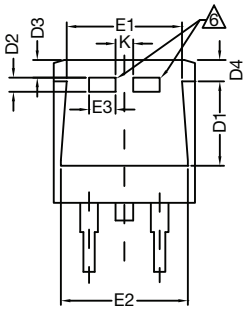
*Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?75050.*

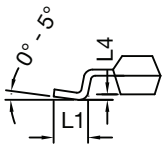
# TO-263 (D²PAK): 3-LEAD

## VERSION 1: FACILITY CODE = T

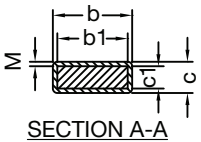



DETAIL A (ROTATED 90°)



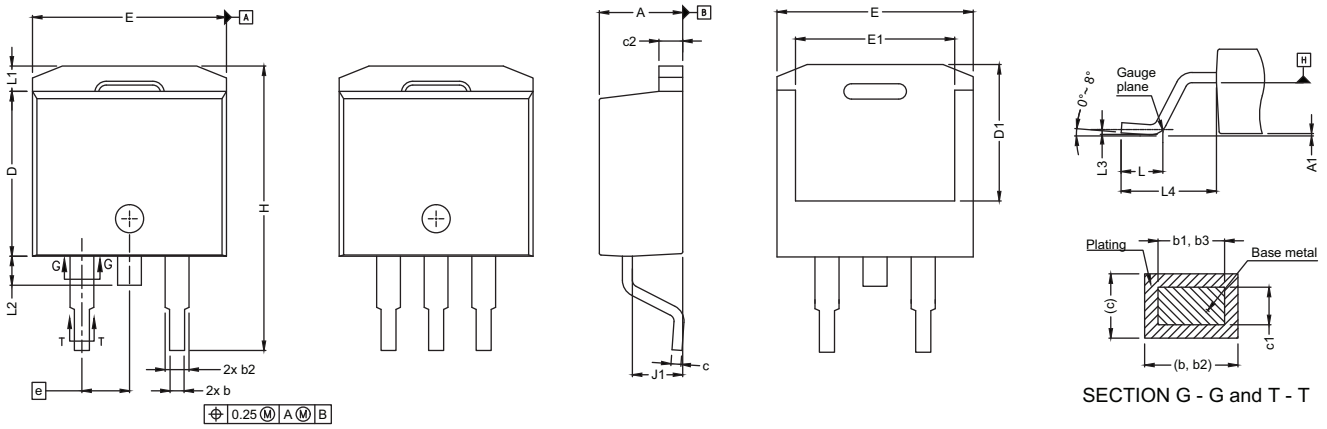

SECTION A-A

| DIM. | | INCHES | | MILLIMETERS | |
|---|---|---|---|---|---|
| | | MIN. | MAX. | MIN. | MAX. |
| A | | 0.160 | 0.190 | 4.064 | 4.826 |
| b | | 0.020 | 0.039 | 0.508 | 0.990 |
| b1 | | 0.020 | 0.035 | 0.508 | 0.889 |
| b2 | | 0.045 | 0.055 | 1.143 | 1.397 |
| c* | Thin lead | 0.013 | 0.018 | 0.330 | 0.457 |
| | Thick lead | 0.023 | 0.028 | 0.584 | 0.711 |
| c1 | Thin lead | 0.013 | 0.017 | 0.330 | 0.431 |
| | Thick lead | 0.023 | 0.027 | 0.584 | 0.685 |
| c2 | | 0.045 | 0.055 | 1.143 | 1.397 |
| D | | 0.340 | 0.380 | 8.636 | 9.652 |
| D1 | | 0.220 | 0.240 | 5.588 | 6.096 |
| D2 | | 0.038 | 0.042 | 0.965 | 1.067 |
| D3 | | 0.045 | 0.055 | 1.143 | 1.397 |
| D4 | | 0.044 | 0.052 | 1.118 | 1.321 |
| E | | 0.380 | 0.410 | 9.652 | 10.414 |
| E1 | | 0.245 | - | 6.223 | - |
| E2 | | 0.355 | 0.375 | 9.017 | 9.525 |
| E3 | | 0.072 | 0.078 | 1.829 | 1.981 |
| e | | 0.100 BSC | | 2.54 BSC | |
| K | | 0.045 | 0.055 | 1.143 | 1.397 |
| L | | 0.575 | 0.625 | 14.605 | 15.875 |
| L1 | | 0.090 | 0.110 | 2.286 | 2.794 |
| L2 | | 0.040 | 0.055 | 1.016 | 1.397 |
| L3 | | 0.050 | 0.070 | 1.270 | 1.778 |
| L4 | | 0.010 BSC | | 0.254 BSC | |
| M | | - | 0.002 | - | 0.050 |

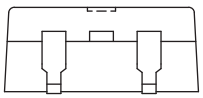
**Notes**

1. Plane B includes maximum features of heat sink tab and plastic.
2. No more than 25 % of L1 can fall above seating plane by max. 8 mils.
3. Pin-to-pin coplanarity max. 4 mils.
4. *: Thin lead is for SUB, SYB.
   Thick lead is for SUM, SYM, SQM.
5. Use inches as the primary measurement.
6. This feature is for thick lead.

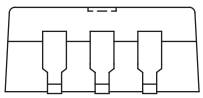
## VERSION 2: FACILITY CODE = N




SECTION G - G and T - T



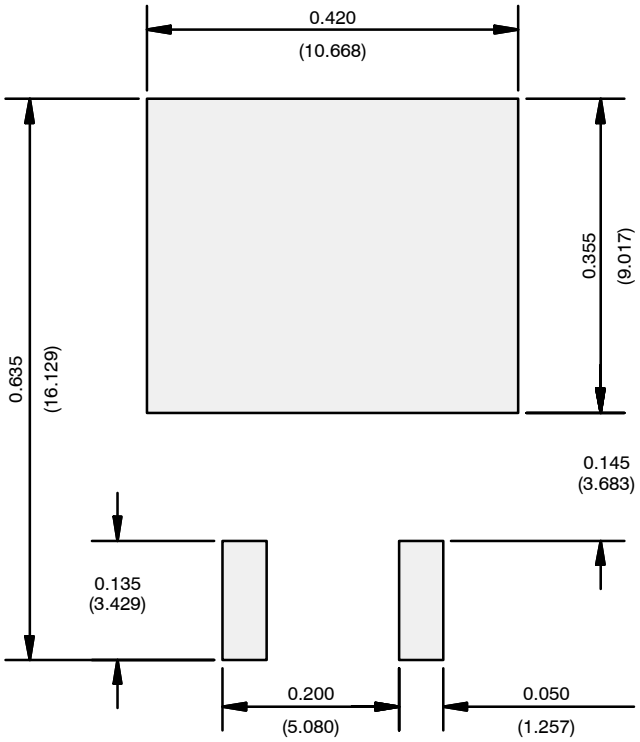
OPTION 1
2 leads



OPTION 2
3 leads

| DIM. | MIN. | MAX. |
|---|---|---|
| A | 4.36 | 4.56 |
| A1 | 0 | 0.25 |
| b | 0.70 | 0.90 |
| b1 | 0.51 | 0.89 |
| b2 | 1.20 | 1.46 |
| b3 | 1.17 | 1.37 |
| c | 0.38 | 0.694 |
| c1 | 0.38 | 0.534 |
| c2 | 1.19 | 1.34 |
| D | 8.60 | 9.00 |
| D1 | 6.9 | 7.5 |
| E | 10.15 | 10.55 |
| E1 | 8.1 | 8.7 |
| e | 2.54 BSC | |
| H | 15.0 | 15.6 |
| L | 1.9 | 2.5 |
| L1 | - | 1.65 |
| L2 | - | 1.78 |
| L3 | 0.25 typ. | |
| L4 | 4.78 | 5.28 |
| J1 | 2.56 | 2.96 |
| ECN: S24-1080-Rev. L, 28-Oct-2024<br>DWG: 5843 | | |

## RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead




Recommended Minimum Pads
Dimensions in Inches/(mm)

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