

## Automotive N-Channel 60 V (D-S) 175 °C MOSFET

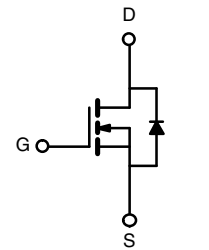
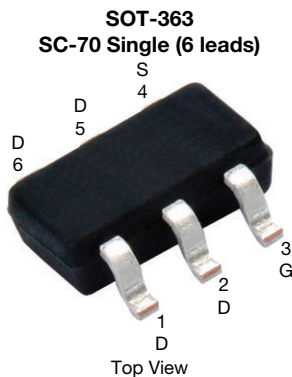


**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

PRODUCT SUMMARY	
V <sub>DS</sub> (V)	60
R <sub>DS(on)</sub> (Ω) at V <sub>GS</sub> = 10 V	0.120
R <sub>DS(on)</sub> (Ω) at V <sub>GS</sub> = 4.5 V	0.150
I <sub>D</sub> (A)	1.7
Configuration	Single
Package	SC-70

### FEATURES

- TrenchFET® power MOSFET
- AEC-Q101 qualified<sup>d</sup>
- 100 % R<sub>g</sub> and UIS tested
- Material categorization:  
for definitions of compliance please see  
[www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



N-Channel MOSFET

Marking Code: 90

ABSOLUTE MAXIMUM RATINGS (T <sub>C</sub> = 25 °C, unless otherwise noted)			
PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V <sub>DS</sub>	60	V
Gate-Source Voltage	V <sub>GS</sub>	± 20	
Continuous Drain Current <sup>a</sup>	I <sub>D</sub>	T <sub>C</sub> = 25 °C	1.7
		T <sub>C</sub> = 125 °C	1.7
Continuous Source Current (Diode Conduction) <sup>a</sup>	I <sub>S</sub>	1.7	A
Pulsed Drain Current <sup>b</sup>	I <sub>DM</sub>	6.7	
Single Pulse Avalanche Current	I <sub>AS</sub>	10	
Single Pulse Avalanche Energy	E <sub>AS</sub>	5	mJ
Maximum Power Dissipation <sup>b</sup>	P <sub>D</sub>	T <sub>C</sub> = 25 °C	3.3
		T <sub>C</sub> = 125 °C	1.1
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55 to +175	°C

THERMAL RESISTANCE RATINGS			
PARAMETER	SYMBOL	LIMIT	UNIT
Junction-to-Ambient	R <sub>thJA</sub>	125	°C/W
Junction-to-Foot (Drain)	R <sub>thJF</sub>	45	

### Notes

- Package limited.
- Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.
- When mounted on 1" square PCB (FR4 material).
- Parametric verification ongoing.



SPECIFICATIONS (T <sub>C</sub> = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
<b>Static</b>							
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA		60	-	-	V
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA		1.5	2	2.5	
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 20 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 60 V	-	-	1	μA
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 60 V, T <sub>J</sub> = 125 °C	-	-	50	
		V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 60 V, T <sub>J</sub> = 175 °C	-	-	150	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>GS</sub> = 10 V	V <sub>DS</sub> ≥ 5 V	10	-	-	A
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 3.8 A	-	0.085	0.120	Ω
		V <sub>GS</sub> = 10 V	I <sub>D</sub> = 3.8 A, T <sub>J</sub> = 125 °C	-	-	0.200	
		V <sub>GS</sub> = 10 V	I <sub>D</sub> = 3.8 A, T <sub>J</sub> = 175 °C	-	-	0.240	
		V <sub>GS</sub> = 4.5 V	I <sub>D</sub> = 3.1 A	-	0.095	0.150	
Forward Transconductance <sup>b</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 1.8 A		-	6	-	S
<b>Dynamic <sup>b</sup></b>							
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V	V <sub>DS</sub> = 15 V, f = 1 MHz	-	275	344	pF
Output Capacitance	C <sub>oss</sub>			-	34	42	
Reverse Transfer Capacitance	C <sub>rss</sub>			-	13	17	
Total Gate Charge <sup>c</sup>	Q <sub>g</sub>	V <sub>GS</sub> = 10 V	V <sub>DS</sub> = 30 V, I <sub>D</sub> = 3.8 A	-	4.4	5.5	nC
Gate-Source Charge	Q <sub>gs</sub>			-	0.7	-	
Gate-Drain Charge <sup>c</sup>	Q <sub>gd</sub>			-	1.3	-	
Gate Resistance	R <sub>g</sub>	f = 1 MHz		2.1	4.1	6.2	Ω
Turn-On Delay Time <sup>c</sup>	t <sub>d(on)</sub>	V <sub>DD</sub> = 30 V, R <sub>L</sub> = 3.9 Ω I <sub>D</sub> ≅ 3.8 A, V <sub>GEN</sub> = 10 V, R <sub>g</sub> = 1 Ω		-	5.8	7.3	ns
Rise Time <sup>c</sup>	t <sub>r</sub>			-	23	29	
Turn-Off Delay Time <sup>c</sup>	t <sub>d(off)</sub>			-	10	13	
Fall Time <sup>c</sup>	t <sub>f</sub>			-	30	39	
<b>Source-Drain Diode Ratings and Characteristics <sup>b</sup></b>							
Pulsed Current <sup>a</sup>	I <sub>SM</sub>			-	-	11	A
Forward Voltage	V <sub>SD</sub>	I <sub>F</sub> = 1.8 A, V <sub>GS</sub> = 0 V		-	0.8	1.2	V

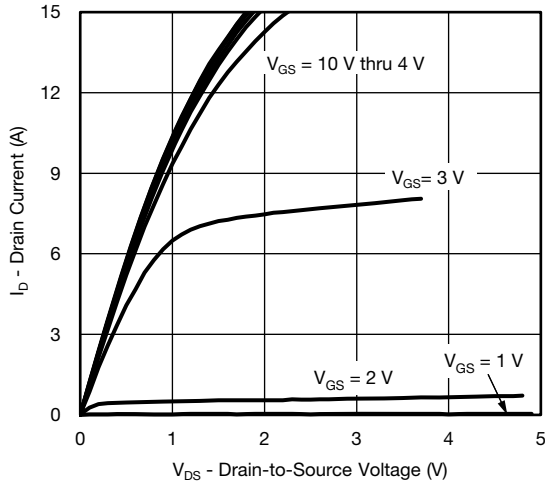
**Notes**

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.

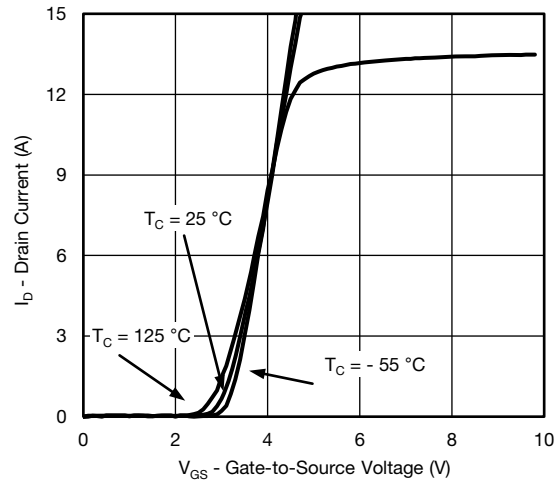
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



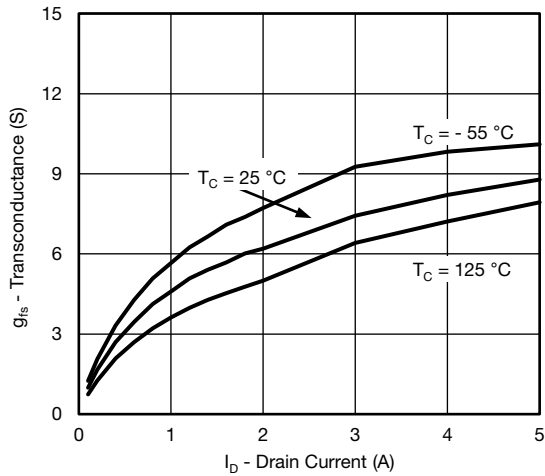
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



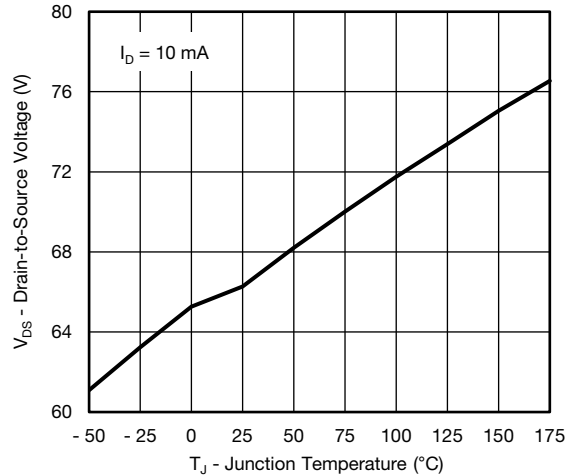
Output Characteristics



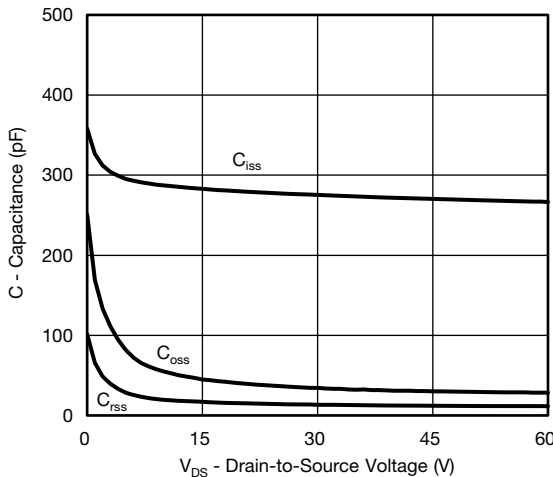
Transfer Characteristics



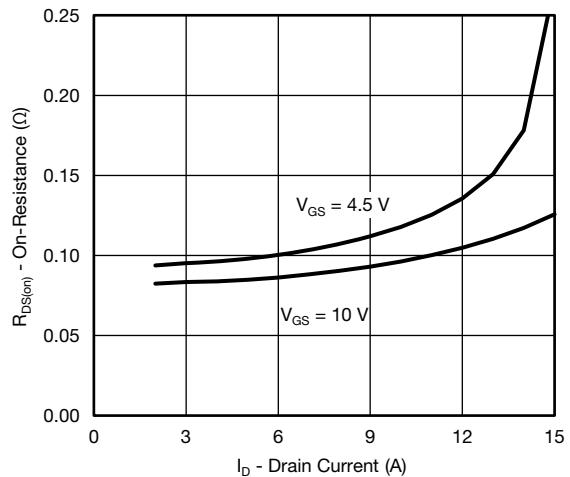
Transconductance



Drain Source Breakdown vs. Junction Temperature



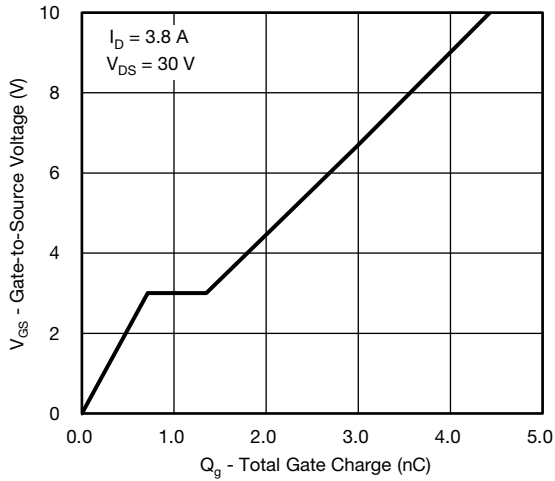
Capacitance



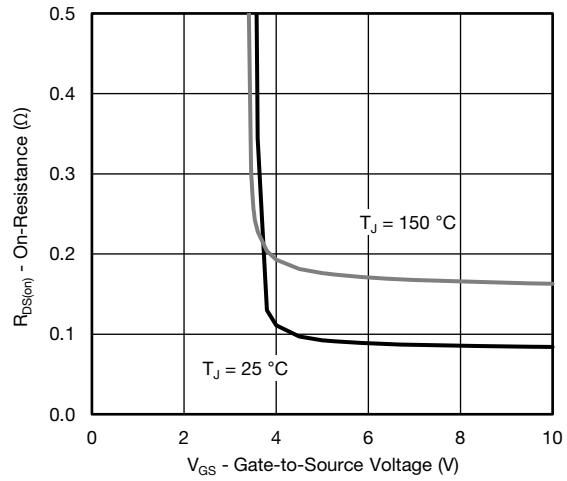
On-Resistance vs. Drain Current



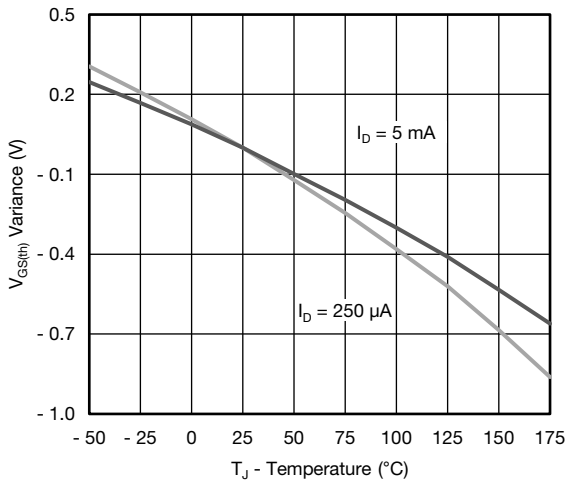
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



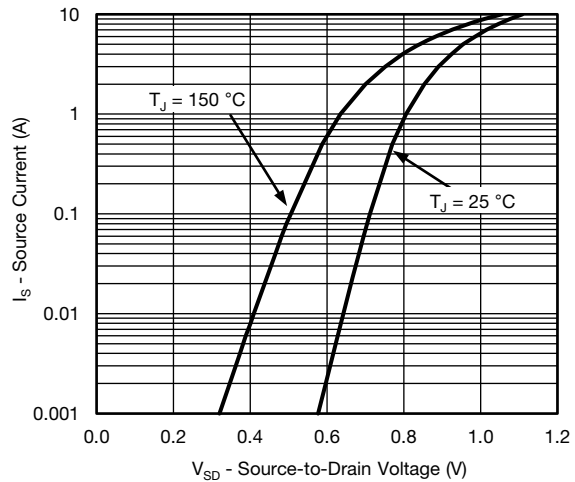
Gate Charge



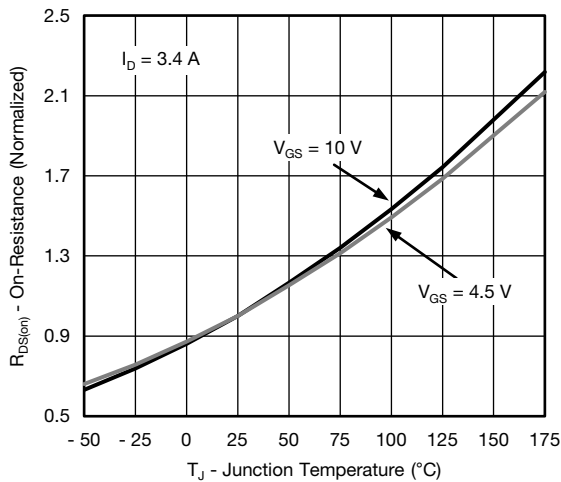
On-Resistance vs. Gate-to-Source Voltage



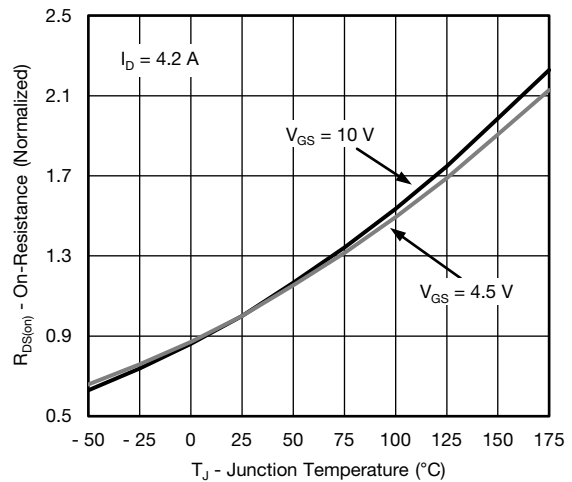
Threshold Voltage



Source Drain Diode Forward Voltage



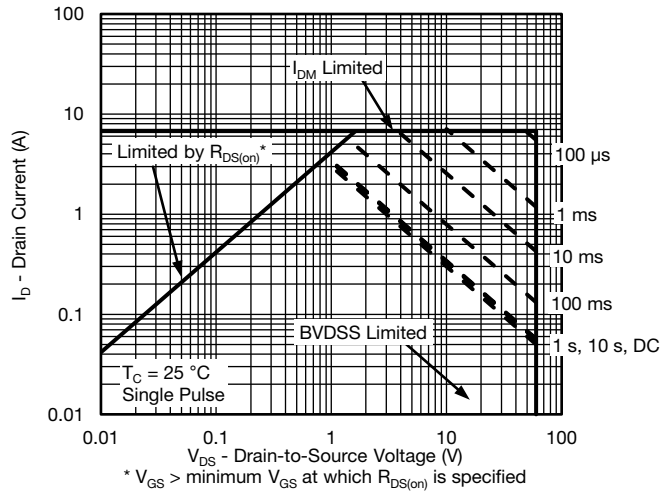
On-Resistance vs. Junction Temperature



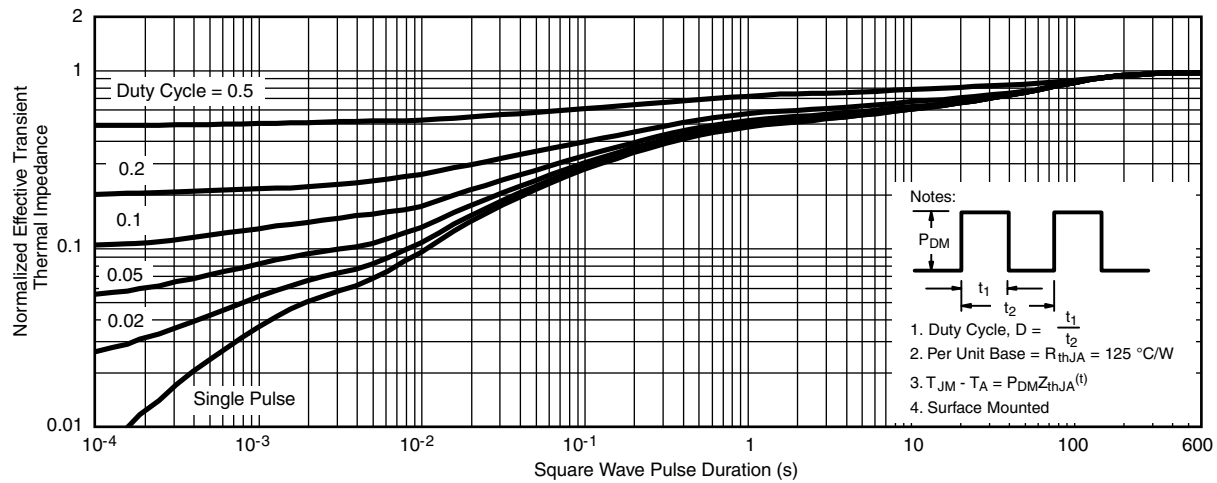
On-Resistance vs. Junction Temperature



**THERMAL RATINGS** ( $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted)



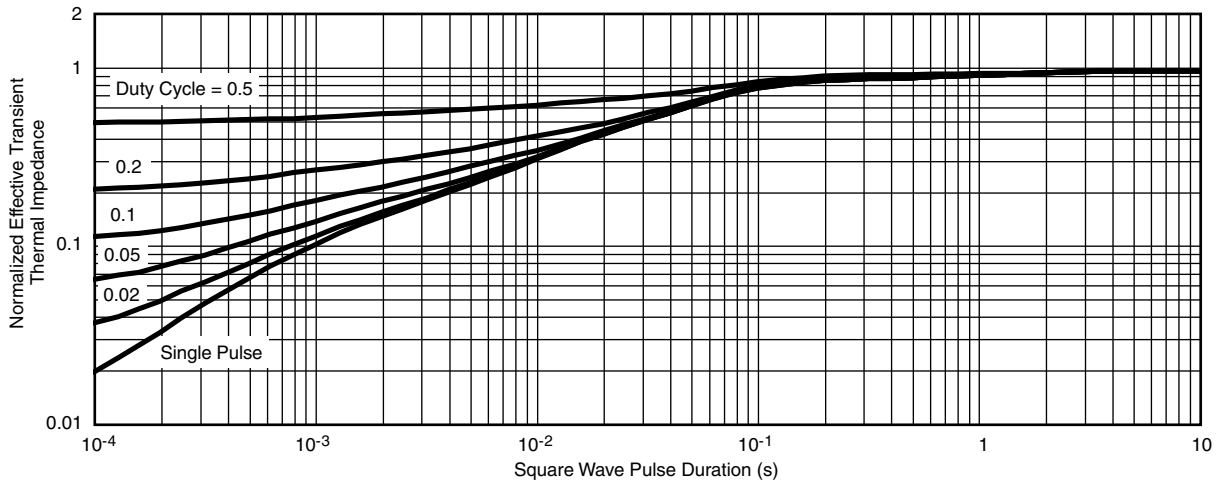
**Safe Operating Area**



**Normalized Thermal Transient Impedance, Junction-to-Ambient**



**THERMAL RATINGS** ( $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted)



**Normalized Thermal Transient Impedance, Junction-to-Foot**

**Note**

- The characteristics shown in the two graphs
    - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
    - Normalized Transient Thermal Impedance Junction-to-Foot (25 °C)
- are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see [www.vishay.com/ppg?65884](http://www.vishay.com/ppg?65884).



## SC-70

Ordering codes for the SQ rugged series power MOSFETs in the SC-70 package:

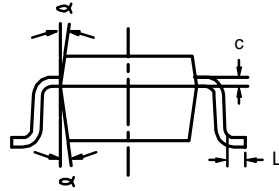
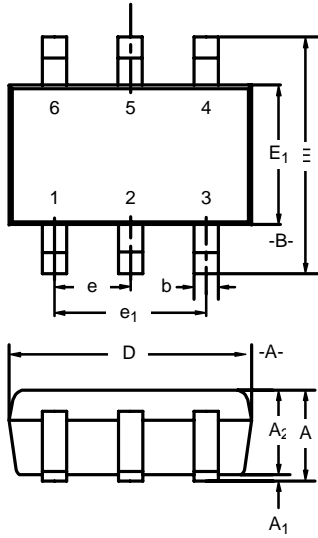
DATASHEET PART NUMBER	OLD ORDERING CODE <sup>a</sup>	NEW ORDERING CODE
SQ1421EEH	SQ1421EEH-T1-GE3	<b>SQ1421EEH-T1_GE3</b>
SQ1431EH	SQ1431EH-T1-GE3	<b>SQ1431EH-T1_GE3</b>
SQ1440EH	-	<b>SQ1440EH-T1_GE3</b>
SQ1470AEH	-	<b>SQ1470AEH-T1_GE3</b>
SQ1539EH	-	<b>SQ1539EH-T1_GE3</b>
SQ1563AEH	-	<b>SQ1563AEH-T1_GE3</b>
SQ1902AEL	-	<b>SQ1902AEL-T1_GE3</b>
SQ1912AEEH	-	<b>SQ1912AEEH-T1_GE3</b>

**Note**

a. Old ordering code is obsolete and no longer valid for new orders



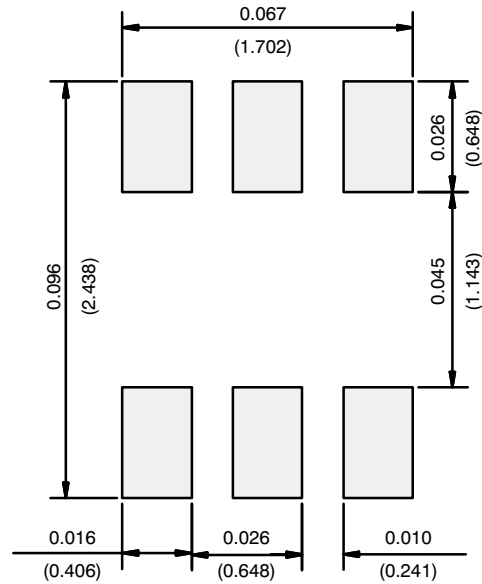
**SC-70: 6-LEADS**



Dim	MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max
A	0.90	-	1.10	0.035	-	0.043
A <sub>1</sub>	-	-	0.10	-	-	0.004
A <sub>2</sub>	0.80	-	1.00	0.031	-	0.039
b	0.15	-	0.30	0.006	-	0.012
c	0.10	-	0.25	0.004	-	0.010
D	1.80	2.00	2.20	0.071	0.079	0.087
E	1.80	2.10	2.40	0.071	0.083	0.094
E <sub>1</sub>	1.15	1.25	1.35	0.045	0.049	0.053
e	0.65BSC			0.026BSC		
e <sub>1</sub>	1.20	1.30	1.40	0.047	0.051	0.055
L	0.10	0.20	0.30	0.004	0.008	0.012
α	7°Nom			7°Nom		

ECN: S-03946—Rev. B, 09-Jul-01  
DWG: 5550

## RECOMMENDED MINIMUM PADS FOR SC-70: 6-Lead



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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