

Dual P-Channel 20 V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)	Q_g (Typ.)
- 20	0.756 at $V_{GS} = - 4.5$ V	- 0.35	1 nC
	1.038 at $V_{GS} = - 2.5$ V	- 0.35	
	1.44 at $V_{GS} = - 1.8$ V	- 0.1	
	2.4 at $V_{GS} = - 1.5$ V	- 0.05	

FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFET
- 100 % R_g Tested
- Typical ESD protection: 1000 V (HBM)
- Fast Switching Speed
- Compliant to RoHS Directive 2002/95/EC

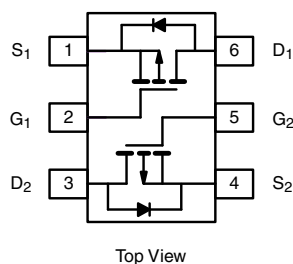


RoHS
COMPLIANT
HALOGEN
FREE

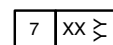
APPLICATIONS

- Load and Small Signal Switch for Portable Devices
- Drivers: Relays, Solenoids, Displays, Lamps
- Battery Operated Systems
- Smart Phones, Tablet PCs

SC-89 (6-LEADS)

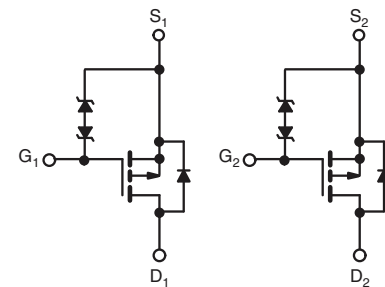


Marking Code



Lot Traceability
and Date Code

Part # Code



Dual P-Channel MOSFET

Ordering Information: Si1023CX-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	- 20	V
Gate-Source Voltage	V_{GS}	± 8	
Continuous Drain Current ($T_J = 150$ °C)	I_D	- 0.45 ^{b, c}	A
		- 0.36 ^{b, c}	
Pulsed Drain Current ($t = 300$ μ s)	I_{DM}	- 1.5	
Continuous Source-Drain Diode Current	I_S	- 0.18 ^{b, c}	
Maximum Power Dissipation	P_D	0.22 ^{b, c}	W
		0.14 ^{b, c}	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150	°C

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{a, b}	R_{thJA}	470	565	°C/W
		560	675	

Notes:

- Maximum under steady state conditions is 675 °C/W.
- Surface mounted on 1" x 1" FR4 board.
- $t = 5$ s.

SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = - 250 μA	- 20			V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = - 250 μA		- 12		mV/°C
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J			1.8		
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = - 250 μA	- 0.4		- 1	V
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 8 V			± 30	μA
		V _{DS} = 0 V, V _{GS} = ± 4.5 V			± 1	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = - 20 V, V _{GS} = 0 V			- 1	
		V _{DS} = - 20 V, V _{GS} = 0 V, T _J = 85 °C			- 10	
On-State Drain Current ^a	I _{D(on)}	V _{DS} = ≥ 5 V, V _{GS} = - 4.5 V	- 1.5			A
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = - 4.5 V, I _D = - 0.35 A		0.630	0.756	Ω
		V _{GS} = - 2.5 V, I _D = - 0.35 A		0.865	1.038	
		V _{GS} = - 1.8 V, I _D = - 0.1 A		1.20	1.44	
		V _{GS} = - 1.5 V, I _D = - 0.05 A		1.6	2.4	
Forward Transconductance	g _{fs}	V _{DS} = - 10 V, I _D = - 0.4 A		1		S
Dynamic ^b						
Input Capacitance	C _{iss}	V _{DS} = - 10 V, V _{GS} = 0 V, f = 1 MHz		45		pF
Output Capacitance	C _{oss}			15		
Reverse Transfer Capacitance	C _{rss}			10		
Total Gate Charge	Q _g	V _{DS} = - 10 V, V _{GS} = - 4.5 V, I _D = - 0.4 A		1.65	2.50	nC
		V _{DS} = - 10 V, V _{GS} = - 2.5 V, I _D = - 0.4 A		1	2	
			Gate-Source Charge	Q _{gs}		
Gate-Drain Charge	Q _{gd}			0.26		
Gate Resistance	R _g	f = 1 MHz	2.4	12	24	Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = - 10 V, R _L = 33.3 Ω I _D ≅ - 0.3 A, V _{GEN} = - 4.5 V, R _g = 1 Ω		9	18	ns
Rise Time	t _r			10	20	
Turn-Off DelayTime	t _{d(off)}			10	20	
Fall Time	t _f			8	16	
Turn-On Delay Time	t _{d(on)}	V _{DD} = - 10 V, R _L = 33.3 Ω I _D ≅ - 0.3 A, V _{GEN} = - 8 V, R _g = 1 Ω		1	2	
Rise Time	t _r			8	16	
Turn-Off DelayTime	t _{d(off)}			9	18	
Fall Time	t _f			5	10	
Drain-Source Body Diode Characteristics						
Pulse Diode Forward Current ^a	I _{SM}				- 1.5	A
Body Diode Voltage	V _{SD}	I _S = - 0.3 A		- 0.8	- 1.2	V
Body Diode Reverse Recovery Time	t _{rr}	I _F = - 0.3 A, dI/dt = 100 A/μs		16	24	ns
Body Diode Reverse Recovery Charge	Q _{rr}			8	16	nC
Reverse Recovery Fall Time	t _a			11		ns
Reverse Recovery Rise Time	t _b			5		

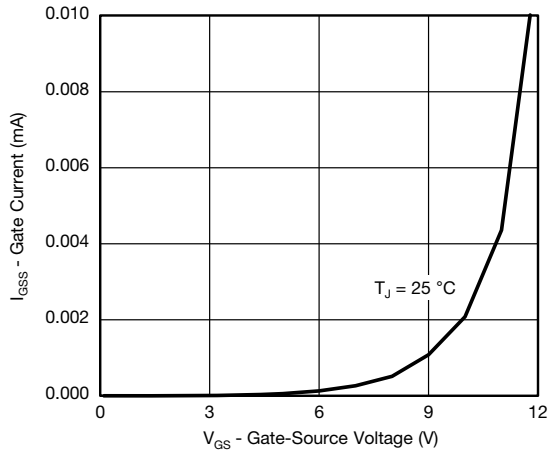
Notes:

a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

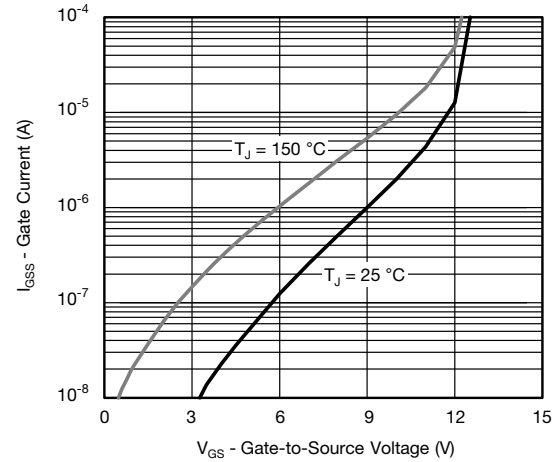
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

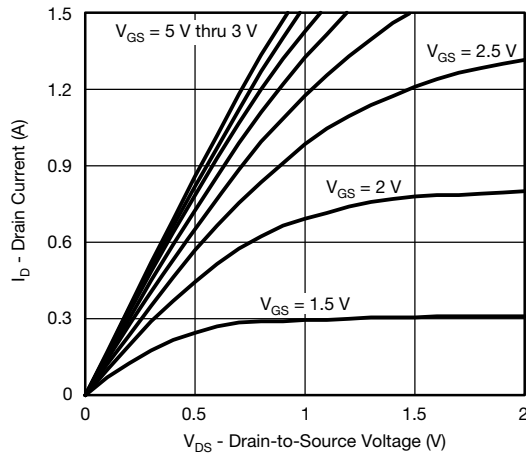
P-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



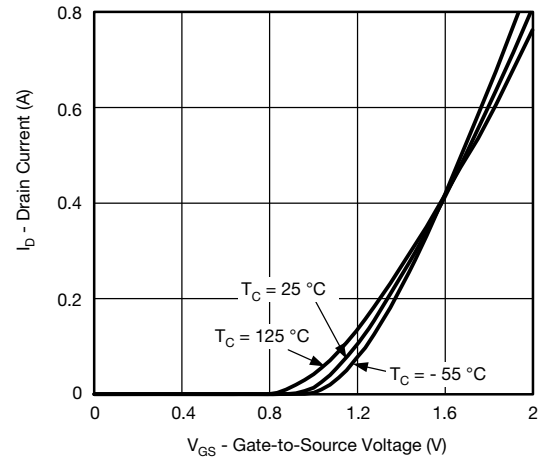
Gate Current vs. Gate-Source Voltage



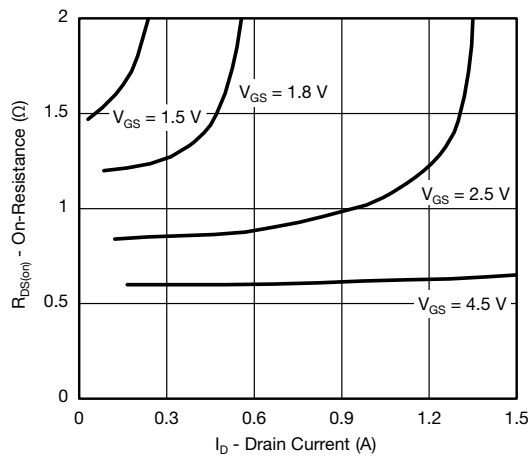
Gate Current vs. Gate-Source Voltage



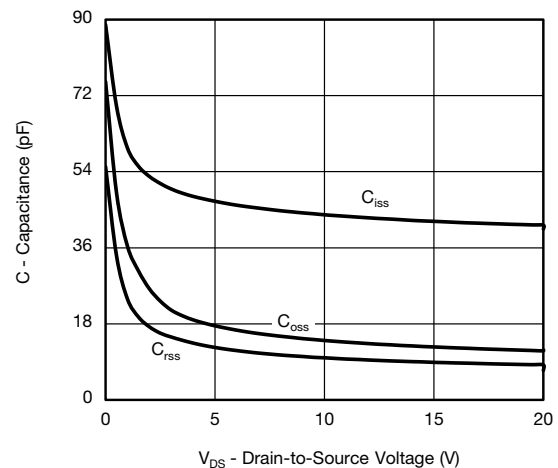
Output Characteristics



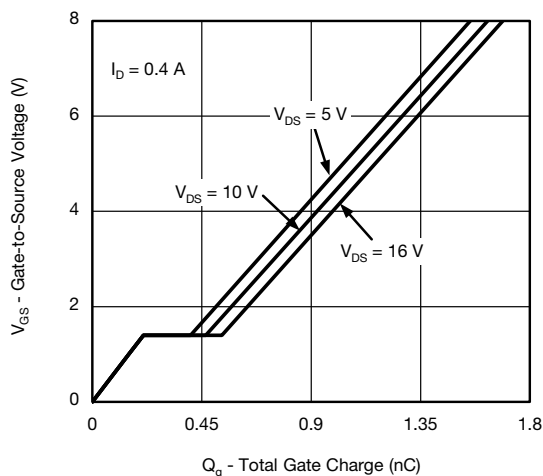
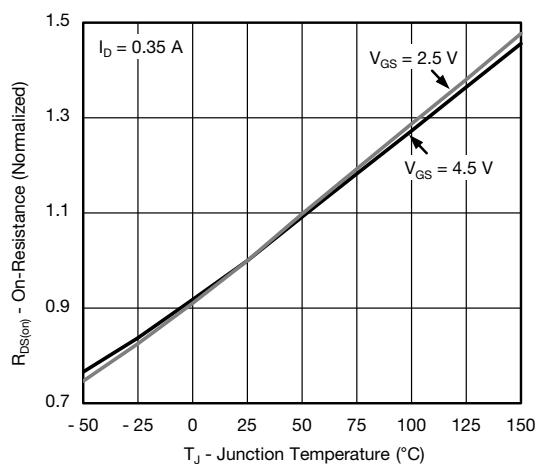
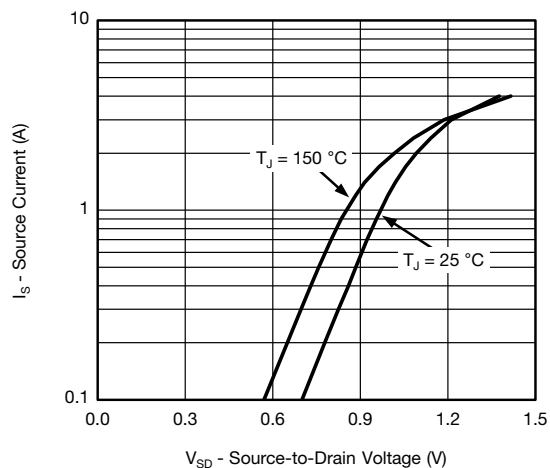
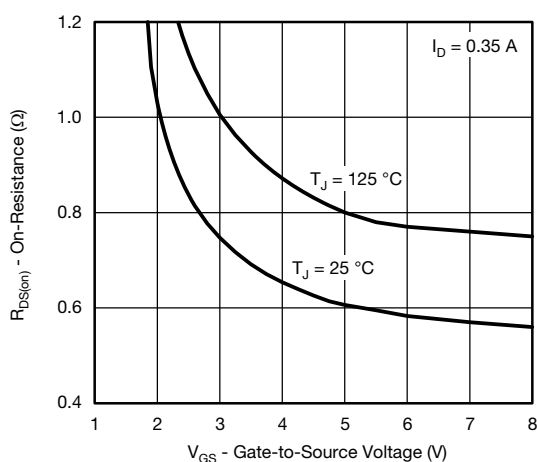
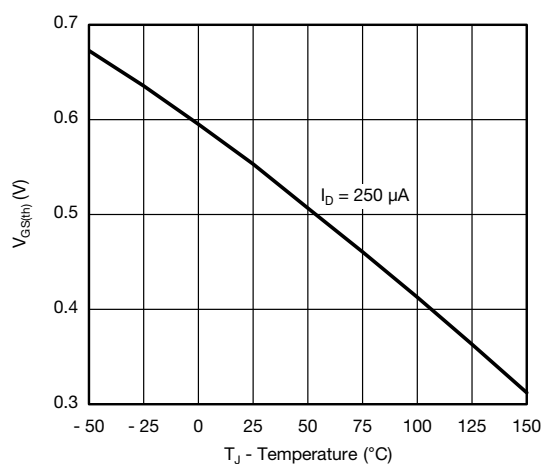
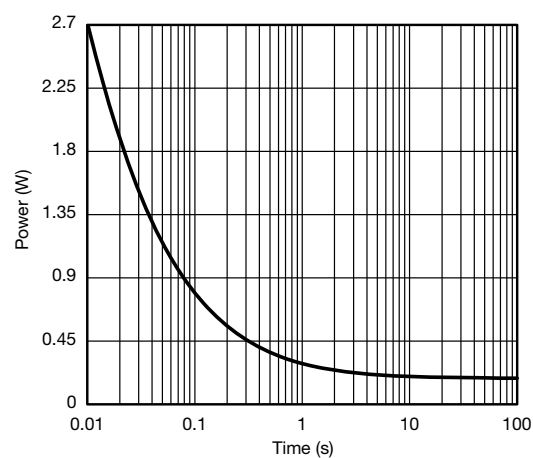
Transfer Characteristics



On-Resistance vs. Drain Current

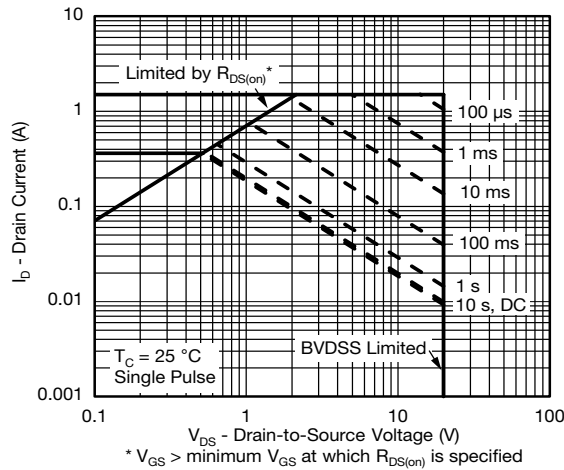


Capacitance

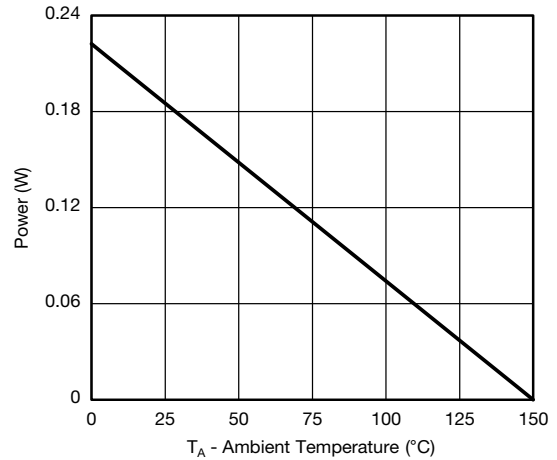
P-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)**Gate Charge****On-Resistance vs. Junction Temperature****Source-Drain Diode Forward Voltage****On-Resistance vs. Gate-to-Source Voltage****Threshold Voltage****Single Pulse Power, Junction-to-Ambient**



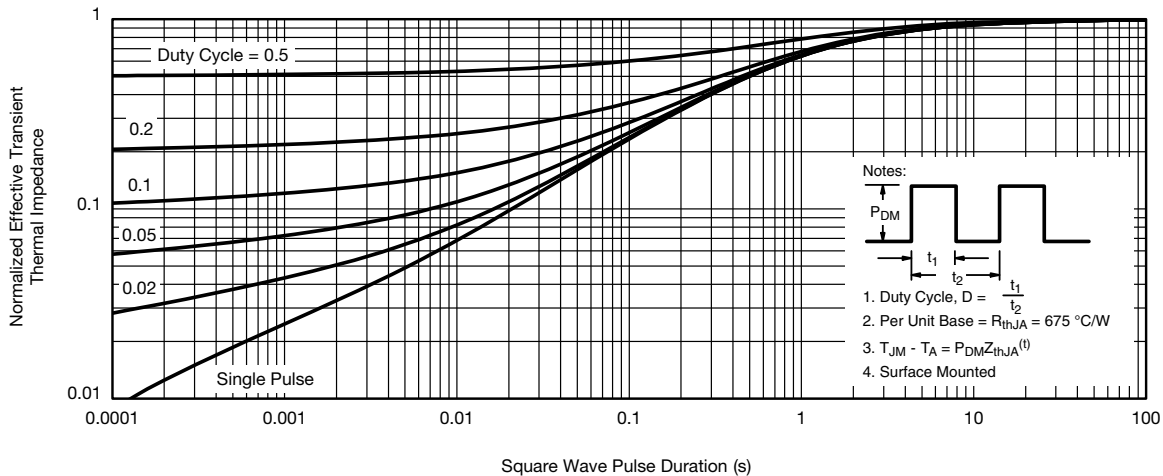
P-CHANNEL TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Safe Operating Area, Junction-to-Ambient



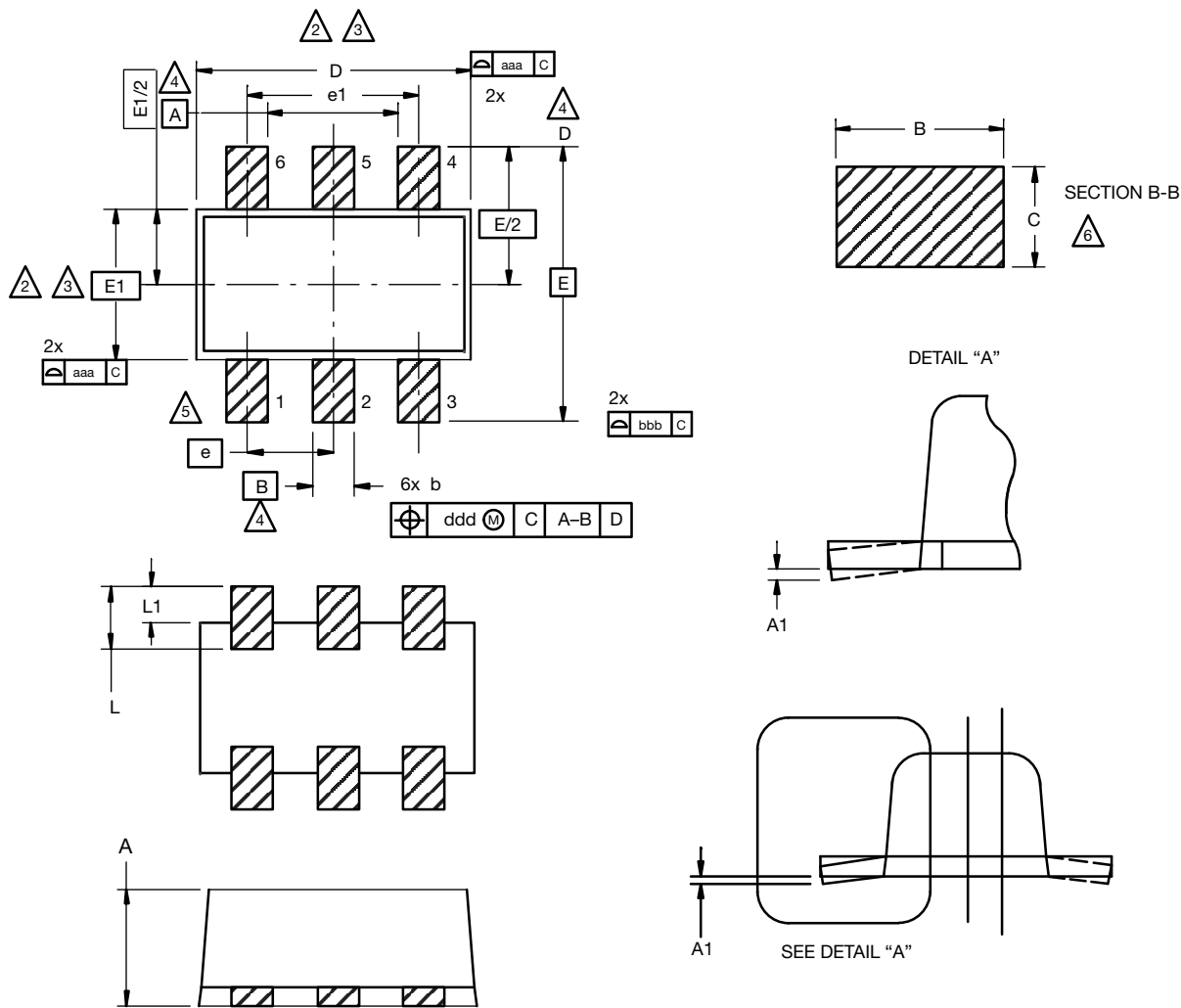
Power Derating, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Ambient

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?63303.

SC-89 6-Leads (SOT-563F)



Notes

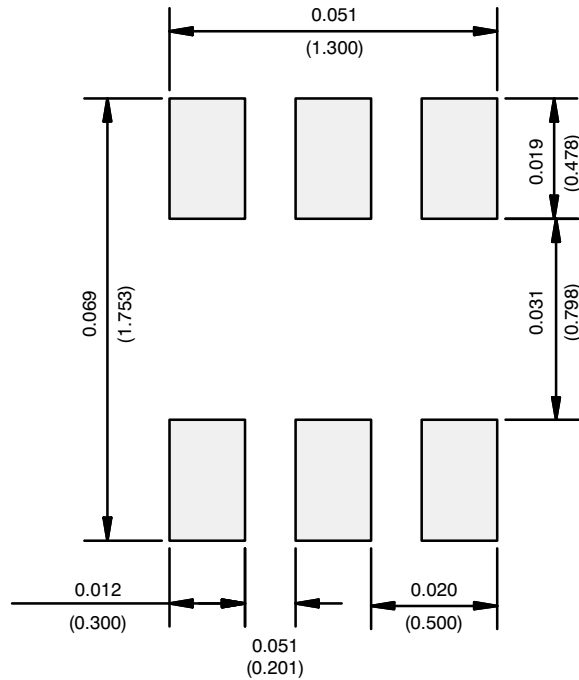
1. Dimensions in millimeters.

- ② Dimension D does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm per dimension E1 does not include interlead flash or protrusion, interlead flash or protrusion shall not exceed 0.15 mm per side.
- ③ Dimensions D and E1 are determined at the outmost extremes of the plastic body exclusive of mold flash, the bar burrs, gate burrs and interlead flash, but including any mismatch between the top and the bottom of the plastic body.
- ④ Datums A, B and D to be determined 0.10 mm from the lead tip.
- ⑤ Terminal numbers are shown for reference only.
- ⑥ These dimensions apply to the flat section of the lead between 0.08 mm and 0.15 mm from the lead tip.

DIM.	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.56	0.58	0.60
A1	0	0.02	0.10
b	0.15	0.22	0.30
c	0.10	0.14	0.18
D	1.50	1.60	1.70
E	1.50	1.60	1.70
E1	1.15	1.20	1.25
e	0.45	0.50	0.55
e1	0.95	1.00	1.05
L	0.25	0.35	0.50
L1	0.10	0.20	0.30

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DWG: 5880

RECOMMENDED MINIMUM PADS FOR SC-89: 6-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

[Return to Index](#)



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