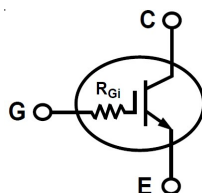


High Voltage XPT™ IGBT

IXYL60N450

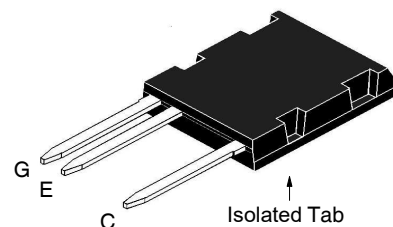
$$\begin{aligned} V_{CES} &= 4500V \\ I_{C110} &= 38A \\ V_{CE(sat)} &\leq 3.30V \end{aligned}$$

(Electrically Isolated Tab)



Symbol	Test Conditions	Maximum Ratings	
V_{CES}	$T_J = 25^\circ\text{C to } 150^\circ\text{C}$	4500	V
V_{CGR}	$T_J = 25^\circ\text{C to } 150^\circ\text{C}, R_{GE} = 1\text{M}\Omega$	4500	V
V_{GES}	Continuous	± 20	V
V_{GEM}	Transient	± 30	V
I_{C25}	$T_C = 25^\circ\text{C}$	90	A
I_{C110}	$T_C = 110^\circ\text{C}$	38	A
I_{CM}	$T_C = 25^\circ\text{C}, 1\text{ms}$	680	A
SSOA (RBSOA)	$V_{GE} = 15\text{V}, T_{VJ} = 125^\circ\text{C}, R_G = 4.7\Omega$	$I_{CM} = 120$	A
	Clamped Inductive Load	1500	V
P_C	$T_C = 25^\circ\text{C}$	417	W
T_J		-55 ... +150	$^\circ\text{C}$
T_{JM}		150	$^\circ\text{C}$
T_{stg}		-55 ... +150	$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering	300	$^\circ\text{C}$
T_{SOLD}	Plastic Body for 10s	260	$^\circ\text{C}$
F_C	Mounting Force	40..120 / 9..27	N/lb
V_{ISOL}	50/60 Hz, RM, $t = 1\text{min}$	4000	V~
Weight		8	g

ISOPLUS i5-Pak™



G = Gate
C = Collector
E = Emitter

Features

- Silicon Chip on Direct-Copper Bond (DCB) Substrate
- Isolated Mounting Surface
- 4000V~ Electrical Isolation
- High Blocking Voltage
- High Peak Current Capability
- Low Saturation Voltage

Advantages

- Low Gate Drive Requirement
- High Power Density

Applications

- Switch-Mode and Resonant-Mode Power Supplies
- Uninterruptible Power Supplies (UPS)
- Laser Generators
- Capacitor Discharge Circuits
- AC Switches

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$, Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
BV_{CES}	$I_C = 250\mu\text{A}, V_{GE} = 0\text{V}$	4500		V
$V_{GE(th)}$	$I_C = 250\mu\text{A}, V_{CE} = V_{GE}$	3.0		5.0 V
I_{CES}	$V_{CE} = 4000\text{V}, V_{GE} = 0\text{V}$ Note 1, $T_J = 90^\circ\text{C}$		75	25 μA μA
I_{GES}	$V_{CE} = 0\text{V}, V_{GE} = \pm 20\text{V}$			± 300 nA
$V_{CE(sat)}$	$I_C = 60\text{A}, V_{GE} = 15\text{V}$, Note 1 $T_J = 125^\circ\text{C}$		2.64 3.46	V V

Symbol Test Conditions ($T_J = 25^\circ\text{C}$ Unless Otherwise Specified)		Characteristic Values		
		Min.	Typ.	Max.
g_{fs}	$I_C = 60\text{A}, V_{CE} = 10\text{V}, \text{Note 1}$	32	54	S
C_{ies}	$V_{CE} = 25\text{V}, V_{GE} = 0\text{V}, f = 1\text{MHz}$		7530	pF
C_{oes}			270	pF
C_{res}			115	pF
R_{Gi}	Integrated Gate Input Resistance		5.0	Ω
$Q_{g(on)}$	$I_C = 60\text{A}, V_{GE} = 15\text{V}, V_{CE} = 1000\text{V}$		366	nC
Q_{ge}			48	nC
Q_{gc}			138	nC
$t_{d(on)}$	Resistive Switching Times, $T_J = 25^\circ\text{C}$ $I_C = 60\text{A}, V_{GE} = 15\text{V}$ $V_{CE} = 960\text{V}, R_G = 4.7\Omega$		55	ns
t_r			450	ns
$t_{d(off)}$			450	ns
t_f			1360	ns
$t_{d(on)}$	Resistive Switching Times, $T_J = 125^\circ\text{C}$ $I_C = 60\text{A}, V_{GE} = 15\text{V}$ $V_{CE} = 960\text{V}, R_G = 4.7\Omega$		60	ns
t_r			664	ns
$t_{d(off)}$			510	ns
t_f			1070	ns
R_{thJC}				0.30 $^\circ\text{C/W}$
R_{thCS}			0.15	$^\circ\text{C/W}$

Notes:

1. Pulse test, $t < 300\mu\text{s}$, duty cycle, $d < 2\%$.
2. Device must be heatsunk for high-temperature leakage current measurements to avoid thermal runaway.

IXYS Reserves the Right to Change Limits, Test Conditions, and Dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents:

4,835,592	4,931,844	5,049,961	5,237,481	6,162,665	6,404,065 B1	6,683,344	6,727,585	7,005,734 B2	7,157,338B2
4,860,072	5,017,508	5,063,307	5,381,025	6,259,123 B1	6,534,343	6,710,405 B2	6,759,692	7,063,975 B2	
4,881,106	5,034,796	5,187,117	5,486,715	6,306,728 B1	6,583,505	6,710,463	6,771,478 B2	7,071,537	

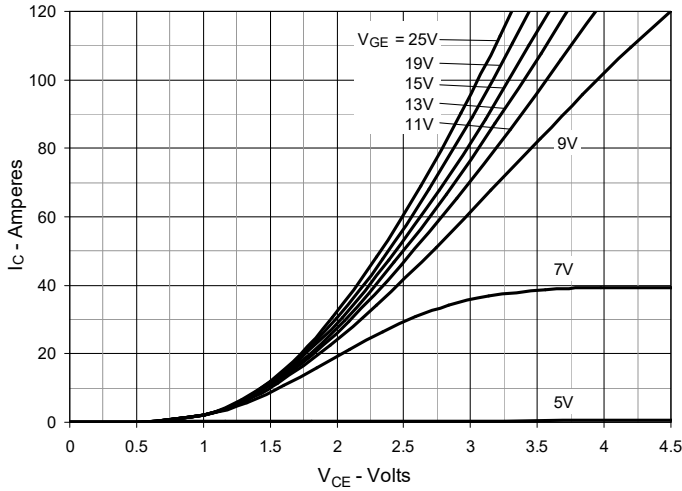
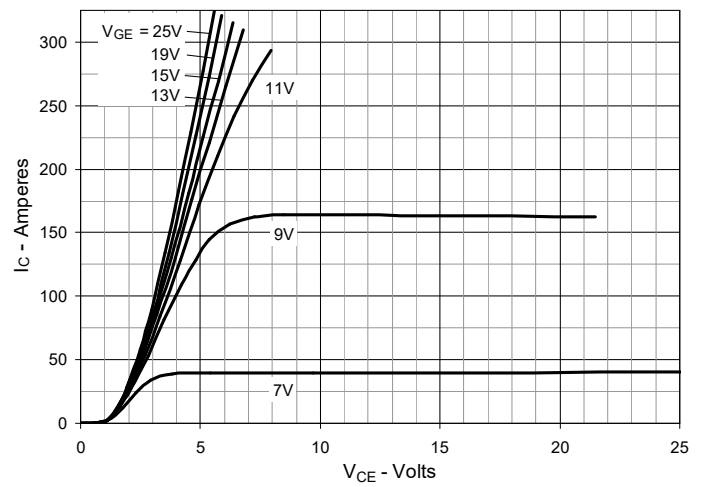
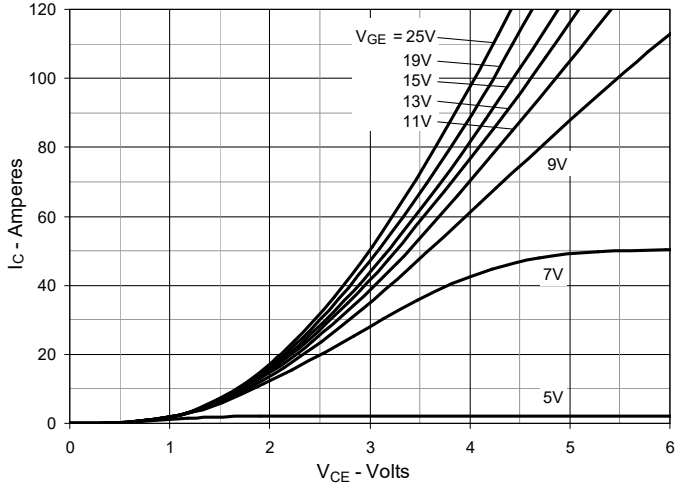
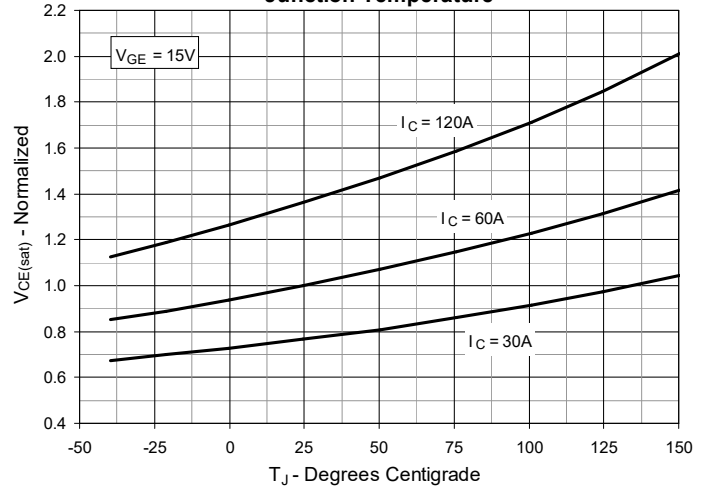
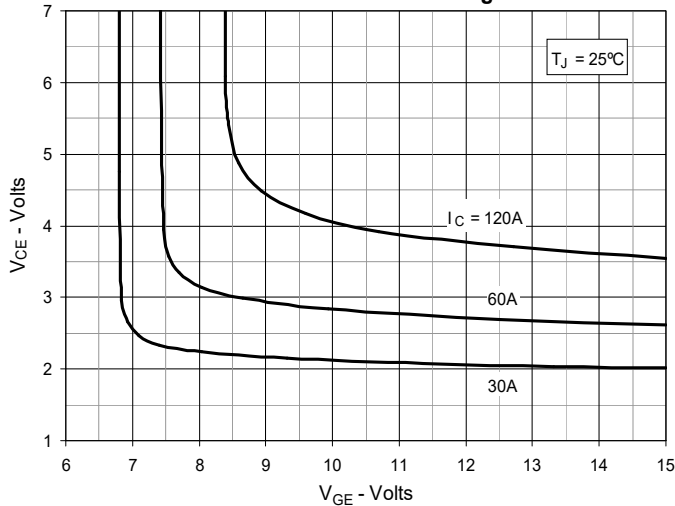
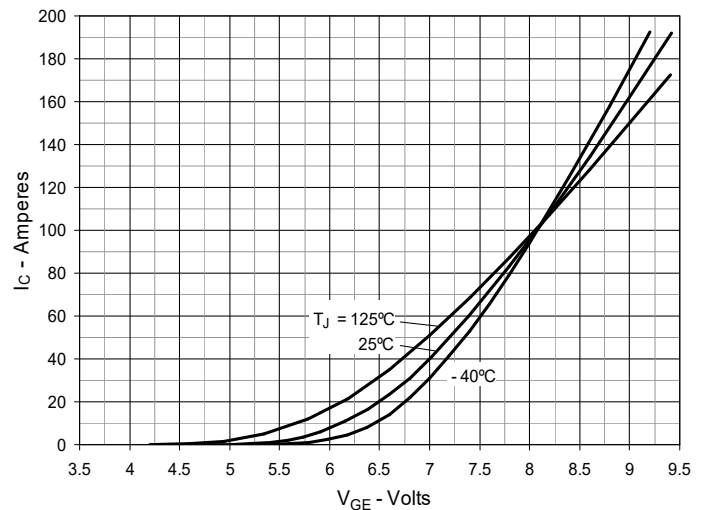
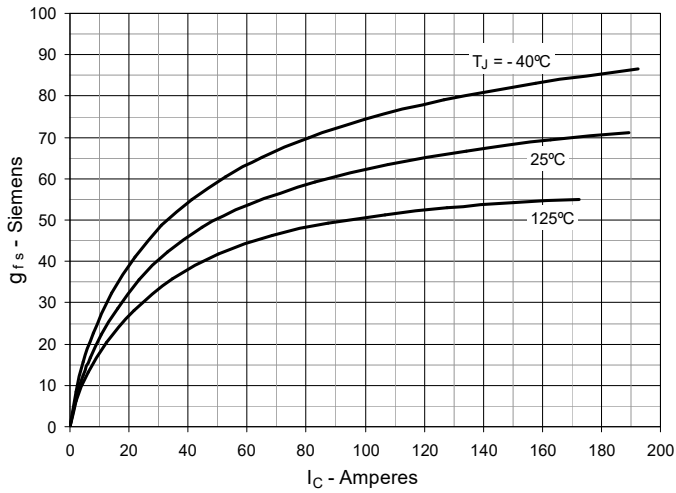
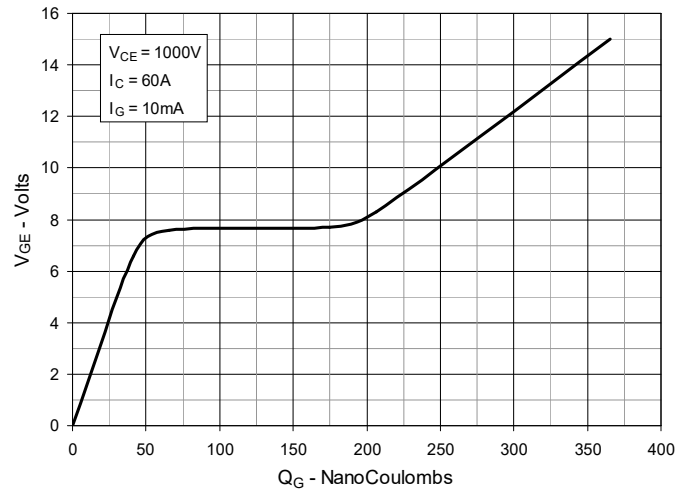
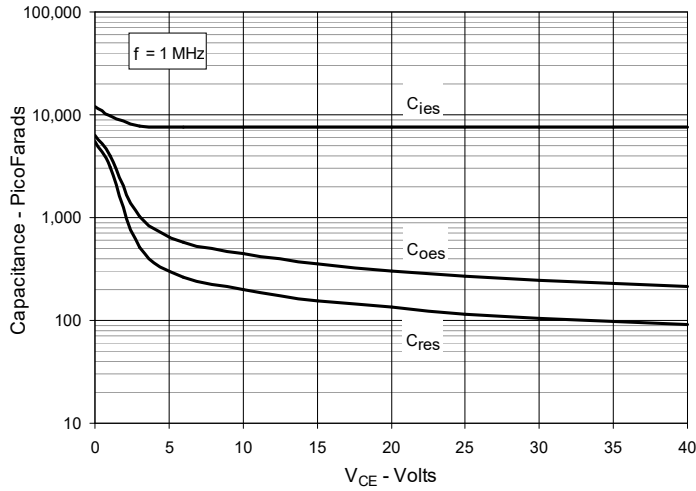
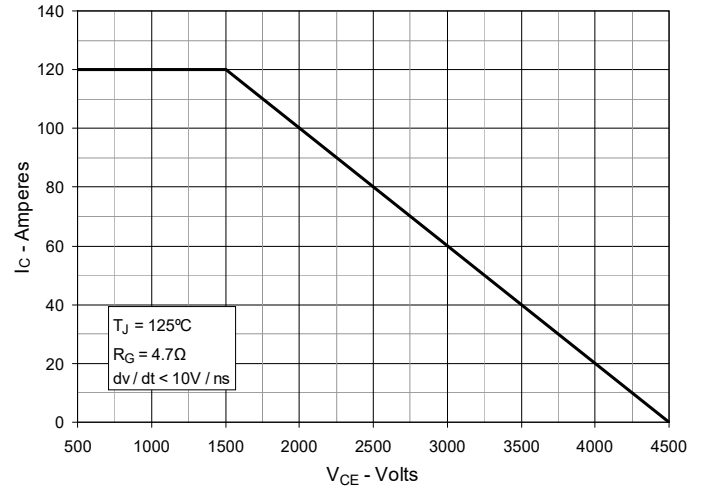
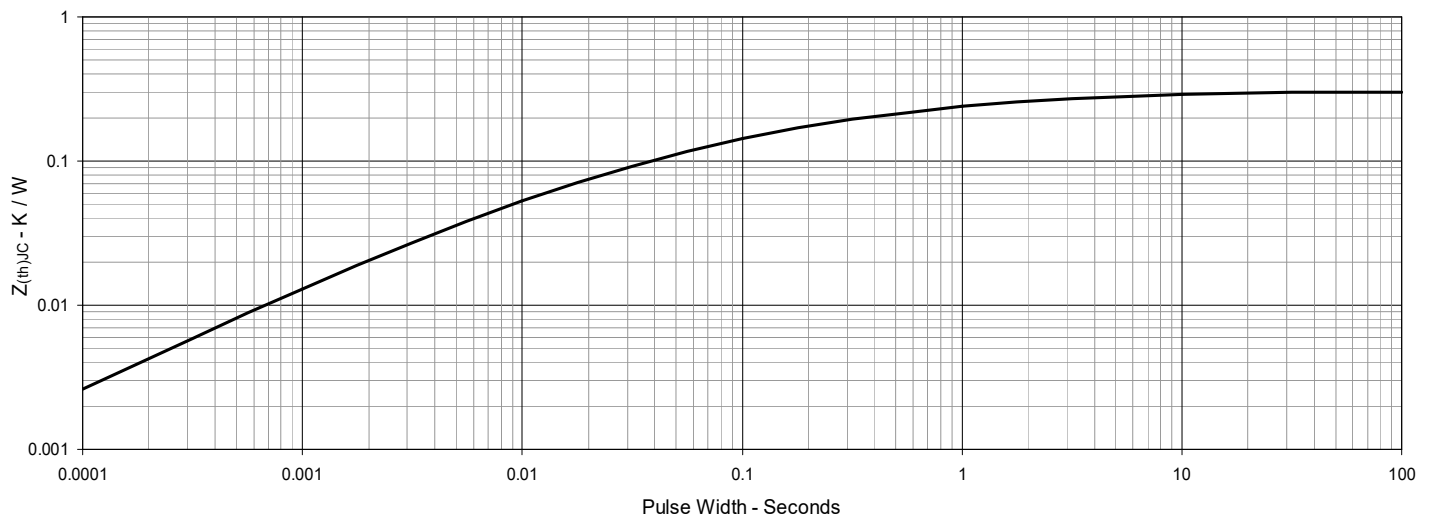
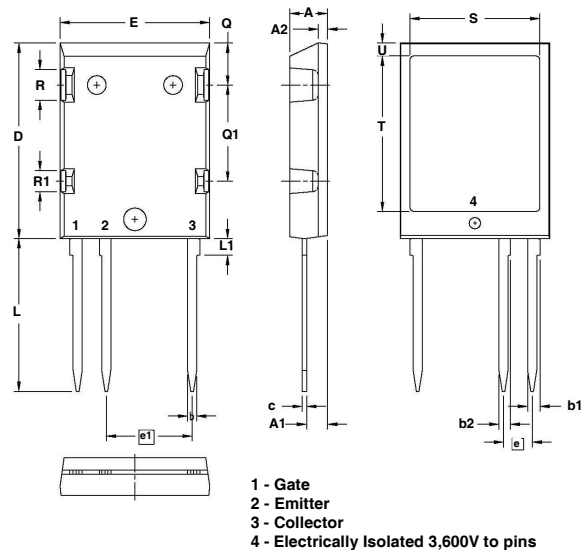
Fig. 1. Output Characteristics @ $T_J = 25^\circ\text{C}$

Fig. 2. Extended Output Characteristics @ $T_J = 25^\circ\text{C}$

Fig. 3. Output Characteristics @ $T_J = 125^\circ\text{C}$

Fig. 4. Dependence of $V_{CE(sat)}$ on Junction Temperature

Fig. 5. Collector-to-Emitter Voltage vs. Gate-to-Emitter Voltage

Fig. 6. Input Admittance


Fig. 7. Transconductance

Fig. 8. Gate Charge

Fig. 9. Capacitance

Fig. 10. Reverse-Bias Safe Operating Area

Fig. 11. Maximum Transient Thermal Impedance


ISOPLUS i5-Pak™ (IXYL) Outline


SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.190	.205	4.83	5.21
A1	.102	.118	2.59	3.00
A2	.046	.055	1.17	1.40
b	.045	.055	1.14	1.40
b1	.063	.072	1.60	1.83
b2	.058	.068	1.47	1.73
c	.020	.029	0.51	0.74
D	1.020	1.040	25.91	26.42
E	.770	.799	19.56	20.29
e	.150 BSC		3.81 BSC	
e1	.450 BSC		11.43 BSC	
L	.780	.820	19.81	20.83
L1	.080	.102	2.03	2.59
Q	.210	.235	5.33	5.97
Q1	.490	.513	12.45	13.03
R	.150	.180	3.81	4.57
R1	.100	.130	2.54	3.30
S	.668	.690	16.97	17.53
T	.801	.821	20.34	20.85
U	.065	.080	1.65	2.03

