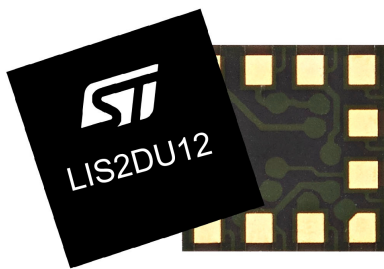


MEMS digital output motion sensor: advanced ultra-low-power 3-axis accelerometer



Features

- Supply voltage range from 1.62 to 3.6 V with independent IO supply
- Ultra-low power consumption
 - Normal mode with anti-alias filter: 5.9 μ A
 - Ultra-low-power mode: 0.45 μ A
 - One-shot mode: 0.2 μ A
 - Power-down: 0.02 μ A
- Low noise down to 160 μ g/ $\sqrt{\text{Hz}}$
- $\pm 2\text{g}/\pm 4\text{g}/\pm 8\text{g}/\pm 16\text{g}$ full scales
- ODR from 1.6 Hz to 800 Hz
- Embedded temperature sensor
- Embedded FIFO: up to 512 samples of accelerometer and temperature data in high resolution or up to 768 samples of acceleration data at low resolution
- High-speed I²C/SPI/MIPI I3CSM digital output interface
- Embedded digital functions (free-fall, wake-up, single/double-tap recognition, activity/inactivity, 6D/4D orientation)
- Self-test
- Small package: 2.0 x 2.0 x 0.74 (max) mm LGA 12-lead
- 10000 g high shock survivability
- ECOPACK, RoHS and “Green” compliant

Applications

- Motion detection for wearables
- Gesture recognition and gaming
- Motion-activated functions and user interfaces
- Display orientation
- Tap/double-tap recognition
- Free-fall detection
- Smart power saving for handheld devices
- Hearing aids and portable healthcare devices
- Wireless sensor nodes
- Motion-enabled metering devices

Description

The LIS2DU12 is an ultra-low-power three-axis linear accelerometer embedding advanced digital functions.

The LIS2DU12 has user-selectable full scales of $\pm 2\text{g}/\pm 4\text{g}/\pm 8\text{g}/\pm 16\text{g}$ and is capable of measuring accelerations with output data rates from 1.6 Hz to 800 Hz.

The LIS2DU12 has an integrated 128-level FIFO buffer allowing to store a wide range of data, reducing system power consumption.

The embedded self-test capability allows the user to check that the sensor works in the final application.

Product status link	
LIS2DU12	
Product summary	
Order code	LIS2DU12TR
Temp. range [°C]	-40 to +85
Package	LGA-12
Packing	Tape and reel
Product resources	
TN0018 (Design and soldering)	

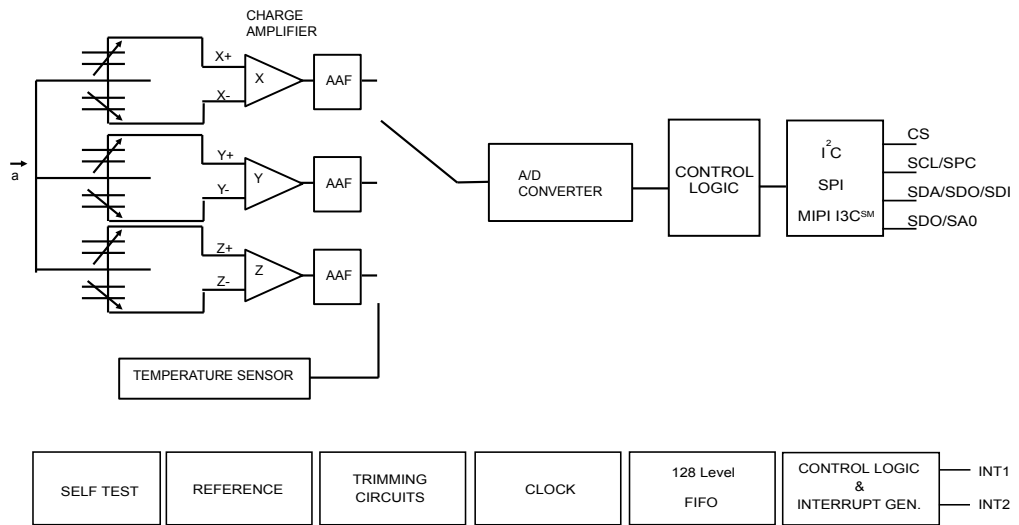
The LIS2DU12 has a dedicated internal engine to process motion and acceleration detection including free-fall, wake-up, single/double-tap recognition, activity/inactivity, and 6D/4D orientation.

The LIS2DU12 is available in a small thin plastic land grid array package (LGA) and it is guaranteed to operate over an extended temperature range from -40°C to $+85^{\circ}\text{C}$.

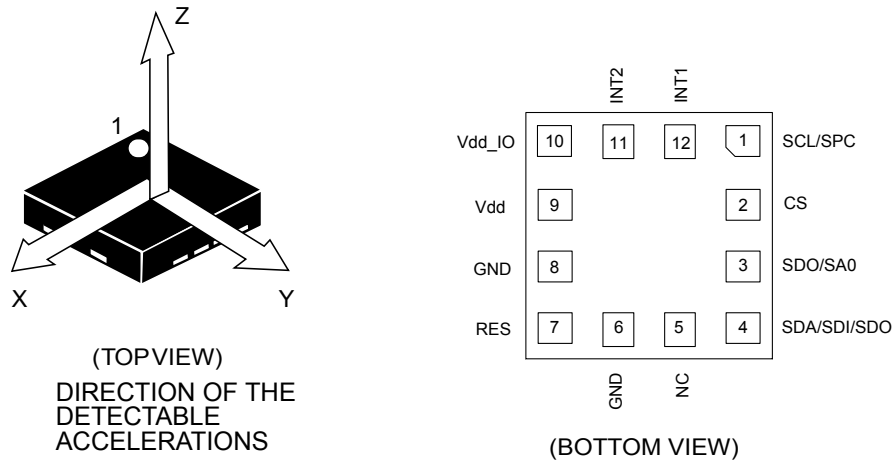
1 Block diagram and pin description

1.1 Block diagram

Figure 1. Block diagram



1.2 Pin description

Figure 2. Pin connections

Table 1. Pin description

Pin#	Name	Function
1	SCL SPC	I ² C/MIPI I3C SM serial clock (SCL) SPI serial port clock (SPC)
2 ⁽¹⁾	CS	SPI/I ² C/MIPI I3C SM mode selection (1: SPI idle mode / I ² C/MIPI I3C SM enabled; 0: SPI enabled / I ² C/MIPI I3C SM disabled)
3 ⁽¹⁾	SDO SA0	SPI serial data output (SDO) I ² C less significant bit of the device address (SA0)
4	SDA SDI SDO	I ² C/MIPI I3C SM serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)
5	NC	Internally not connected. Can be tied to Vdd, Vdd_IO, or GND.
6	GND	0 V supply
7	RES	Connect to GND
8	GND	0 V supply
9	Vdd	Power supply
10	Vdd_IO	Power supply for I/O pins
11 ⁽²⁾	INT2	Interrupt pin 2. Clock input when selected in single data conversion on demand.
12 ⁽²⁾	INT1	Interrupt pin 1

1. CS and SDO/SA0 pins are internally pulled up. The pull-up of the CS pin can be disconnected by setting bit 2 of register IF_PU_CTRL (0Ch) to '1'. The pull-up of the SDO pin can be disconnected by setting bit 7 of register IF_PU_CTRL (0Ch) to '1'.
2. The INT1 and INT2 pins are internally pulled down. The internal pull-down of the INT1 pin can be disconnected by setting the PD_DIS_INT1 bit in IF_CTRL (0Eh) to '1'. The internal pull-down of the INT2 pin can be disconnected by setting the PD_DIS_INT2 bit in MD2_CFG (20h) to '1'.

2 Mechanical and electrical specifications

2.1 Mechanical characteristics

@ Vdd = 1.8 V, T = 25 °C unless otherwise noted.

The product is factory calibrated at 1.8 V. The operational power supply range is from 1.62 V to 3.6 V.

Table 2. Mechanical characteristics

Symbol	Parameter	Test conditions	Min.	Typ. ⁽¹⁾	Max.	Unit
FS	Measurement range			±2		g
				±4		
				±8		
				±16		
So	Sensitivity	@ FS ±2 g		0.976		mg/digit
		@ FS ±4 g		1.952		
		@ FS ±8 g		3.904		
		@ FS ±16 g		7.808		
An	Noise density - normal mode	@ FS ±8 g ODR = 800 Hz, BW = ODR/2		280		µg/√Hz
TyOff	Zero-g level offset accuracy ⁽²⁾			±30		mg
TCO	Zero-g offset change vs. temperature			±1		mg/°C
TCS	Sensitivity change vs. temperature			±0.035		%/°C
ST	Self-test positive difference	X-axis		320		mg
		Y-axis		320		
		Z-axis		420		

1. Typical specifications are not guaranteed.

2. Values after factory calibration test and trimming.

2.2 Electrical characteristics

@ Vdd = 1.8 V, T = 25 °C unless otherwise noted.

The product is factory calibrated at 1.8 V. The operational power supply range is from 1.62 V to 3.6 V.

Table 3. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ. ⁽¹⁾	Max.	Unit
Vdd	Supply voltage		1.62	1.8	3.6	V
Vdd_IO	I/O pins supply voltage ⁽²⁾		1.62		Vdd + 0.1	V
IddNM	Current consumption in normal mode	FS = ±8 g ODR = 800 Hz, BW = ODR/2 with anti-alias filter		5.9		µA
IddULP	Current consumption in ultra-low-power mode	FS = ±8 g ODR = 1.6 Hz, BW = ODR/2		0.45		µA
Idd_PD	Current consumption in power-down			20		nA
V _{IH}	Digital high-level input voltage		0.7*Vdd_IO			V
V _{IL}	Digital low-level input voltage				0.3*Vdd_IO	V
V _{OH}	Digital high-level output voltage	I _{OH} = 4 mA ⁽³⁾	Vdd_IO - 0.2 V			
V _{OL}	Digital low-level output voltage	I _{OL} = 4 mA ⁽³⁾			0.2 V	

1. Typical specifications are not guaranteed.
2. It is possible to remove Vdd, maintaining Vdd_IO without blocking the communication busses. In this condition the measurement chain is powered off.
3. 4 mA is the maximum driving capability, ie. the maximum DC current that can be sourced/sunk by the digital pin in order to guarantee the correct digital output voltage levels V_{OH} and V_{OL}.

2.3 Temperature sensor characteristics

@ Vdd = 1.8 V, T = 25 °C unless otherwise noted.

Table 4. Temperature sensor characteristics

Symbol	Parameter	Min.	Typ. ⁽¹⁾	Max.	Unit
Top	Operating temperature range	-40		+85	°C
Toff	Temperature offset ⁽²⁾	-15		+15	°C
TSDr	Temperature sensor output change vs. temperature		0.045 ⁽³⁾		°C/LSB
TODR	Temperature refresh rate		ODR		Hz

1. Typical specifications are not guaranteed.
2. The output of the temperature sensor is 0 LSB (typ.) at 25 °C.
3. 12-bit resolution.

2.4 Communication interface characteristics

2.4.1 SPI - serial peripheral interface

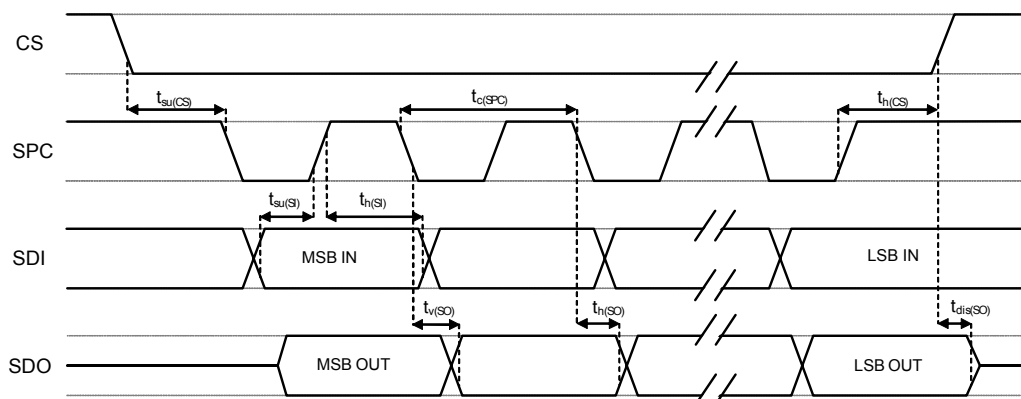
Subject to general operating conditions for V_{dd} and Top.

Table 5. SPI slave timing values

Symbol	Parameter	Value ⁽¹⁾		Unit
		Min	Max	
$t_{c(SPC)}$	SPI clock cycle	100		ns
$f_{c(SPC)}$	SPI clock frequency		10	MHz
$t_{su(CS)}$	CS setup time	6		ns
$t_{h(CS)}$	CS hold time	40		
$t_{su(SI)}$	SDI input setup time	12		
$t_{h(SI)}$	SDI input hold time	15		
$t_{v(SO)}$	SDO valid output time		50	
$t_{h(SO)}$	SDO output hold time	9		
$t_{dis(SO)}$	SDO output disable time		50	

1. 10 MHz clock frequency for SPI with both 4 and 3 wires, based on characterization results, not tested in production.

Figure 3. SPI slave timing diagram



Note: Measurement points are done at $0.3 \cdot V_{dd_IO}$ and $0.7 \cdot V_{dd_IO}$ for both input and output ports.

2.4.2 I²C - inter-IC control interface

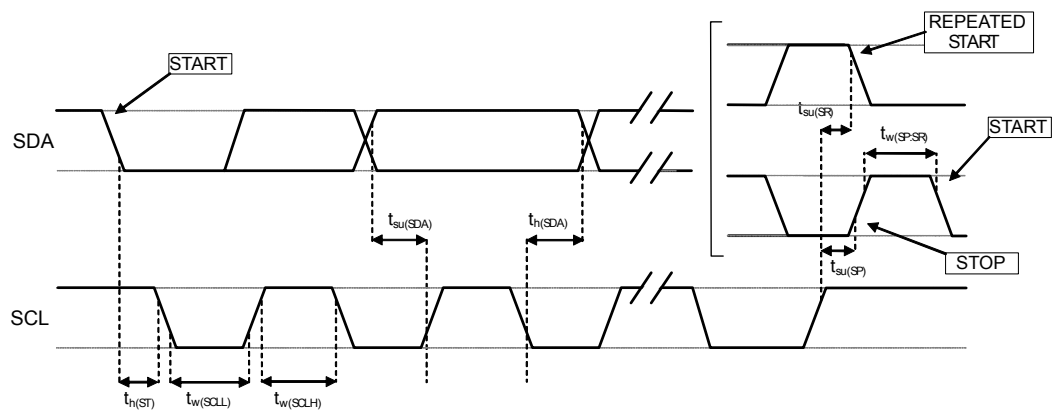
Subject to general operating conditions for V_{dd} and Top.

Table 6. I²C slave timing values

Symbol	Parameter	I ² C standard mode ⁽¹⁾		I ² C fast mode ⁽¹⁾		Unit
		Min	Max	Min	Max	
f _(SCL)	SCL clock frequency	0	100	0	400	kHz
t _{w(SCLL)}	SCL clock low time	4.7		1.3		μs
t _{w(SCLH)}	SCL clock high time	4.0		0.6		
t _{su(SDA)}	SDA setup time	250		100		ns
t _{h(SDA)}	SDA data hold time	0.01	3.45	0.01	0.9	μs
t _{h(ST)}	START condition hold time	4		0.6		μs
t _{su(SR)}	Repeated START condition setup time	4.7		0.6		
t _{su(SP)}	STOP condition setup time	4		0.6		
t _{w(SP:SR)}	Bus free time between STOP and START condition	4.7		1.3		

1. Data based on standard I²C protocol requirement, not tested in production.

Figure 4. I²C slave timing diagram



Note: Measurement points are done at 0.3·V_{dd_IO} and 0.7·V_{dd_IO} for both ports.

2.5 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 7. Absolute maximum ratings

Symbol	Ratings	Maximum value	Unit
V _{dd}	Supply voltage	-0.3 to 4.3	V
V _{dd_IO}	I/O pins supply voltage	-0.3 to 4.3	V
V _{in}	Input voltage on any control pin (CS, SCL/SPC, SDA/SDI/SDO, SDO/SA0)	-0.3 to V _{dd_IO} +0.3	V
A _{POW}	Acceleration (any axis, powered, V _{dd} = 1.8 V)	3000 g for 0.5 ms	g
		10000 g for 0.2 ms	g
A _{UNP}	Acceleration (any axis, unpowered)	3000 g for 0.5 ms	g
		10000 g for 0.2 ms	g
T _{OP}	Operating temperature range	-40 to +85	°C
T _{STG}	Storage temperature range	-40 to +125	°C
ESD	Electrostatic discharge protection	2 (HBM)	kV

Note: Supply voltage on any pin should never exceed 4.3 V.



This device is sensitive to mechanical shock, improper handling can cause permanent damage to the part.



This device is sensitive to electrostatic discharge (ESD), improper handling can cause permanent damage to the part.

3 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

3.1 Soldering information

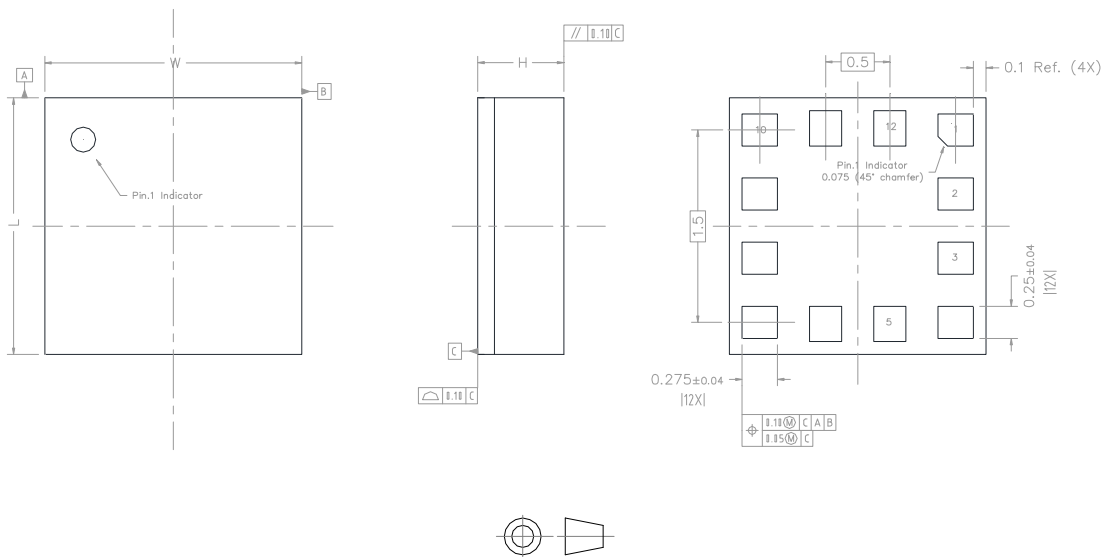
The LGA package is compliant with the **ECOPACK**, RoHS and “Green” standard.

It is qualified for soldering heat resistance according to JEDEC J-STD-020.

For the land pattern and soldering recommendations, please consult technical note **TN0018** available on www.st.com.

3.2 LGA-12 package information

Figure 5. LGA-12 2.0 x 2.0 x 0.74 mm package outline and mechanical data



Dimensions are in millimeter unless otherwise specified
General Tolerance is +/-0.15mm unless otherwise specified

OUTER DIMENSIONS

ITEM	DIMENSION [mm]	TOLERANCE [mm]
Length [L]	2	±0.1
Width [W]	2	±0.1
Height [H]	0.74 MAX	/

DM00170568

Revision history

Table 8. Document revision history

Date	Version	Changes
28-Jun-2021	1	Initial release

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