



BUK9K13-40H

Dual N-channel 40 V, 13 mOhm logic level MOSFET in LPAK56D

11 February 2021

Product data sheet

1. General description

Dual, Logic level N-channel MOSFET in an LPAK56D package, using Trench 9 TrenchMOS technology. This product has been designed and qualified to AEC-Q101 for use in high performance automotive applications

2. Features and benefits

- Fully automotive qualified to AEC-Q101 at 175 °C
- Trench 9 superjunction technology:
 - Low power losses, high power density
- LPAK copper clip package technology:
 - High robustness and reliability
 - Gull wing leads for high manufacturability and AOI
- Repetitive avalanche rated

3. Applications

- 12 V, 24 V and 48 V automotive systems
- Motors, lamps and solenoid control
- Transmission control
- DC-to-DC conversion

4. Quick reference data

Table 1. Quick reference data

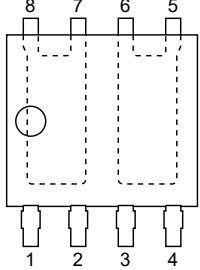
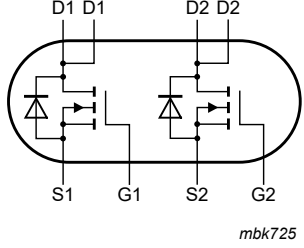
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$		-	-	40	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	[1]	-	-	42	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1		-	-	46	W
Static characteristics FET1 and FET2							
R_{DSon}	drain-source on-state resistance	$V_{GS} = 4.5\text{ V}$; $I_D = 10\text{ A}$; $T_j = 25\text{ °C}$; Fig. 11		9.8	14.1	16.9	mΩ
Dynamic characteristics FET1 and FET2							
Q_{GD}	gate-drain charge	$I_D = 10\text{ A}$; $V_{DS} = 32\text{ V}$; $V_{GS} = 5\text{ V}$; $T_j = 25\text{ °C}$; Fig. 13 ; Fig. 14		-	1.8	4.2	nC
Source-drain diode FET1 and FET2							
Q_r	recovered charge	$I_S = 10\text{ A}$; $dI_S/dt = -100\text{ A/}\mu\text{s}$; $V_{GS} = 0\text{ V}$; $V_{DS} = 20\text{ V}$; $T_j = 25\text{ °C}$	[2]	-	16.2	-	nC

[1] 42A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

[2] Includes capacitive recovery

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source1	 LFPAK56D; Dual LFPAK (SOT1205)	 mbk725
2	G1	gate1		
3	S2	source2		
4	G2	gate2		
5	D2	drain2		
6	D2	drain2		
7	D1	drain1		
8	D1	drain1		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK9K13-40H	LFPAK56D; Dual LFPAK	plastic, single ended surface mounted package (LFPAK56D); 8 leads	SOT1205

7. Marking

Table 4. Marking codes

Type number	Marking code
BUK9K13-40H	91340HK

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$		-	40	V
V_{GS}	gate-source voltage	DC; $T_j = 25\text{ °C}$		-20	20	V
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1		-	46	W
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	[1]	-	42	A
		$V_{GS} = 10\text{ V}$; $T_{mb} = 100\text{ °C}$; Fig. 2		-	30	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$; Fig. 3		-	169	A
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C
Source-drain diode FET1 and FET2						
I_S	source current	$T_{mb} = 25\text{ °C}$		-	42	A
I_{SM}	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$		-	169	A

Symbol	Parameter	Conditions		Min	Max	Unit
Avalanche Ruggedness FET1 and FET2						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 39.9\text{ A}$; $V_{sup} \leq 40\text{ V}$; $R_{GS} = 50\ \Omega$; $V_{GS} = 10\text{ V}$; $T_{j(\text{init})} = 25\text{ }^\circ\text{C}$; Fig. 4	[2] [3]	-	10.6	mJ
I_{AS}	non-repetitive avalanche current	$V_{sup} = 40\text{ V}$; $V_{GS} = 10\text{ V}$; $T_{j(\text{init})} = 25\text{ }^\circ\text{C}$; $R_{GS} = 50\ \Omega$; Fig. 4	[4]	-	39.9	A

- [1] 42A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.
 [2] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
 [3] Refer to application note AN10273 for further information.
 [4] Protected by 100% test

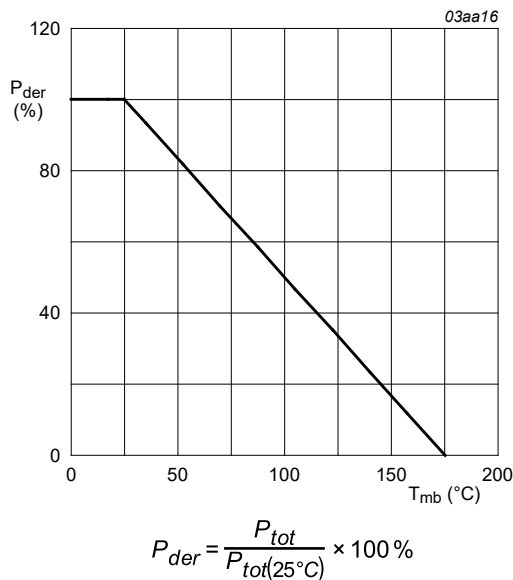
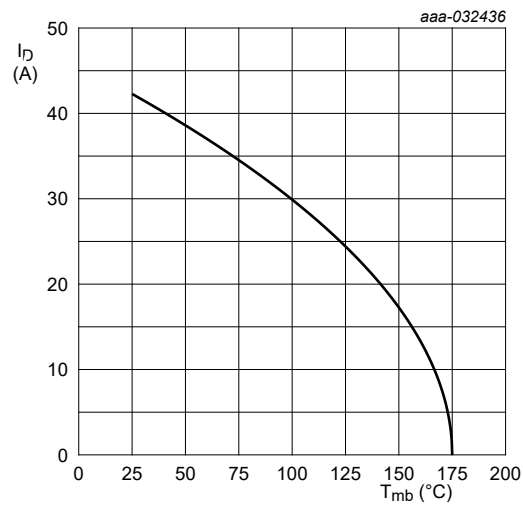


Fig. 1. Normalized total power dissipation as a function of mounting base temperature



42A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

Fig. 2. Continuous drain current as a function of mounting base temperature, FET1 and FET2

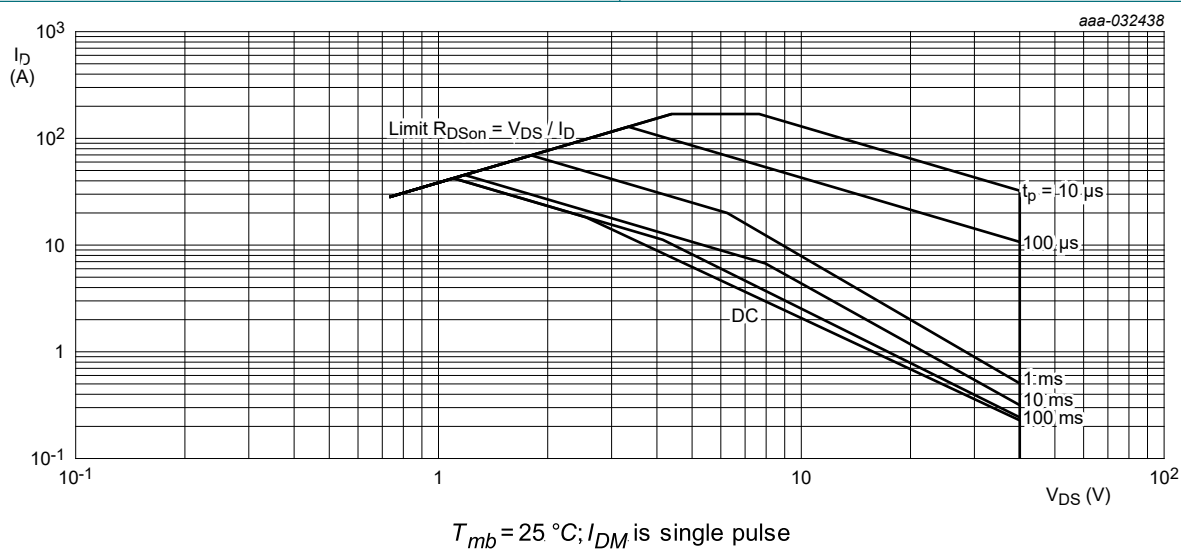
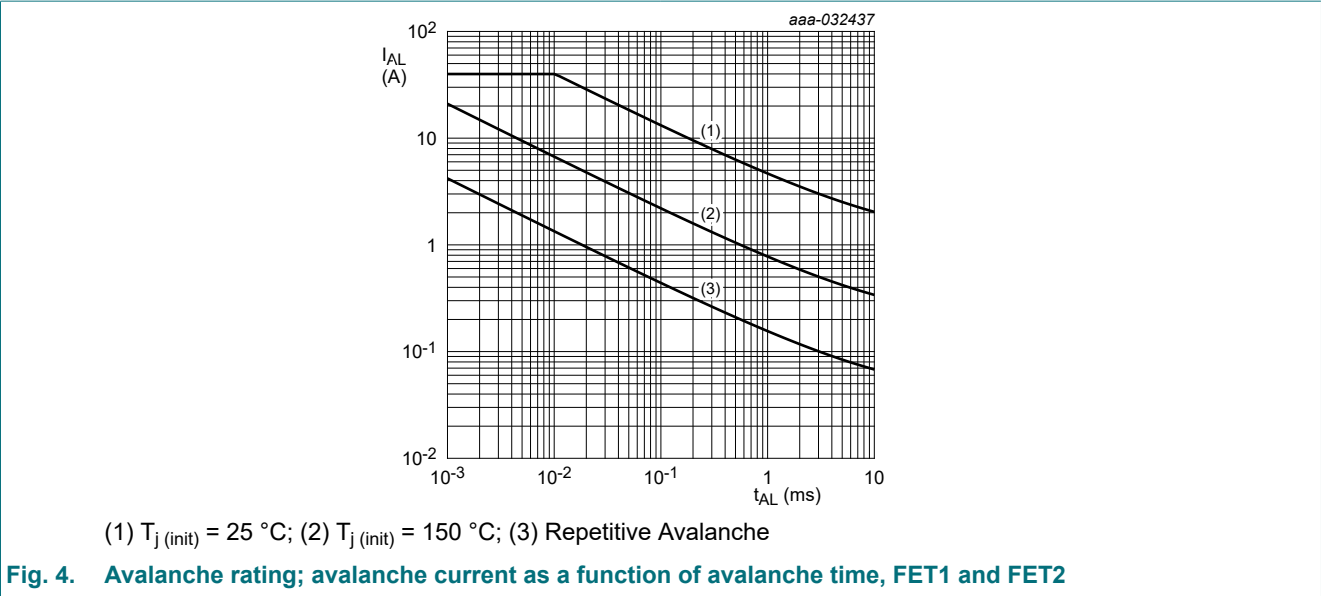


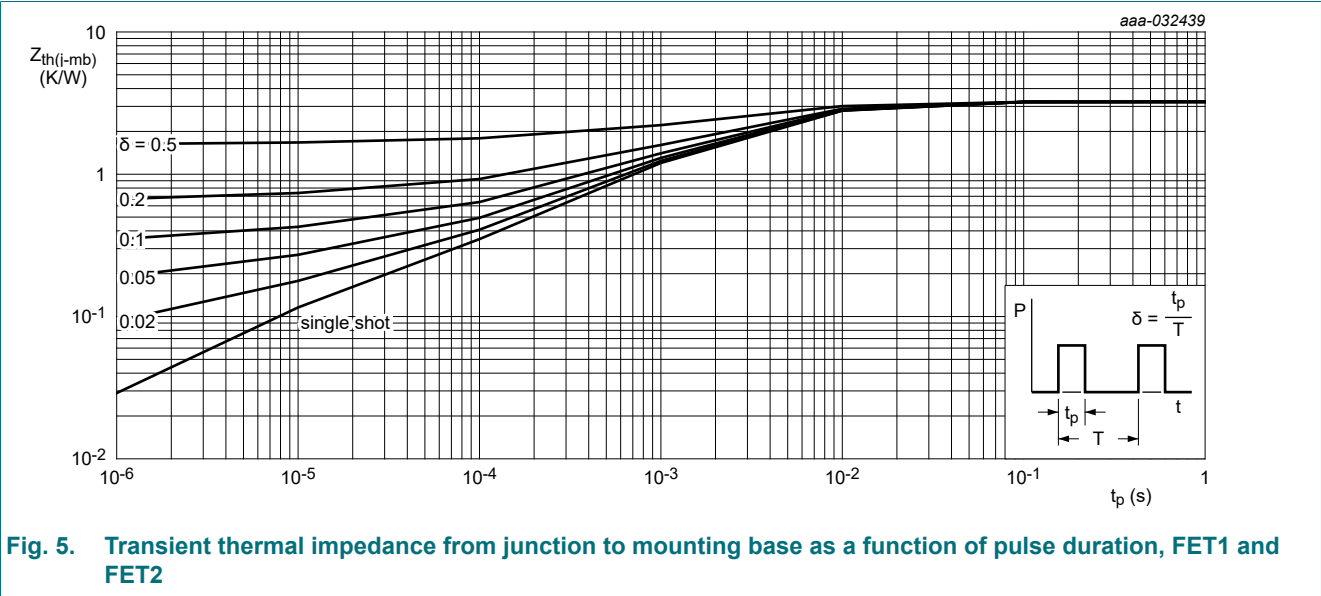
Fig. 3. Safe operating area; continuous and peak drain current as a function of drain-source voltage, FET1 and FET2



9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5		-	3	3.23	K/W



10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics FET1 and FET2						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\ \mu A$; $V_{GS} = 0\ V$; $T_J = 25\ ^\circ C$	40	43	-	V
		$I_D = 250\ \mu A$; $V_{GS} = 0\ V$; $T_J = -40\ ^\circ C$	-	40.5	-	V
		$I_D = 250\ \mu A$; $V_{GS} = 0\ V$; $T_J = -55\ ^\circ C$	36	40	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\ mA$; $V_{DS}=V_{GS}$; $T_J = 25\ ^\circ C$; Fig. 9 ; Fig. 10	1.5	1.85	2.2	V
		$I_D = 1\ mA$; $V_{DS}=V_{GS}$; $T_J = 175\ ^\circ C$; Fig. 10	0.7	-	-	V
		$I_D = 1\ mA$; $V_{DS}=V_{GS}$; $T_J = -55\ ^\circ C$; Fig. 10	-	-	2.6	V
I_{DSS}	drain leakage current	$V_{DS} = 40\ V$; $V_{GS} = 0\ V$; $T_J = 25\ ^\circ C$	-	0.01	5	μA
		$V_{DS} = 16\ V$; $V_{GS} = 0\ V$; $T_J = 125\ ^\circ C$	-	0.14	10	μA
		$V_{DS} = 40\ V$; $V_{GS} = 0\ V$; $T_J = 175\ ^\circ C$	-	26	500	μA
I_{GSS}	gate leakage current	$V_{GS} = -10\ V$; $V_{DS} = 0\ V$; $T_J = 25\ ^\circ C$	-	2	100	nA
		$V_{GS} = 16\ V$; $V_{DS} = 0\ V$; $T_J = 25\ ^\circ C$	-	2	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\ V$; $I_D = 10\ A$; $T_J = 25\ ^\circ C$; Fig. 11	7.9	11.4	13.6	m Ω
		$V_{GS} = 10\ V$; $I_D = 10\ A$; $T_J = 105\ ^\circ C$; Fig. 12	10.9	16	20.4	m Ω
		$V_{GS} = 10\ V$; $I_D = 10\ A$; $T_J = 125\ ^\circ C$; Fig. 12	12	17.4	21.9	m Ω
		$V_{GS} = 10\ V$; $I_D = 10\ A$; $T_J = 175\ ^\circ C$; Fig. 12	14.5	20.9	26.4	m Ω
		$V_{GS} = 4.5\ V$; $I_D = 10\ A$; $T_J = 25\ ^\circ C$; Fig. 11	9.8	14.1	16.9	m Ω
		$V_{GS} = 4.5\ V$; $I_D = 10\ A$; $T_J = 105\ ^\circ C$; Fig. 12	13.5	20	25.4	m Ω
		$V_{GS} = 4.5\ V$; $I_D = 10\ A$; $T_J = 125\ ^\circ C$; Fig. 12	14.8	21.6	27.2	m Ω
		$V_{GS} = 4.5\ V$; $I_D = 10\ A$; $T_J = 175\ ^\circ C$; Fig. 12	18	26.6	32.8	m Ω
R_G	gate resistance	$f = 1\ MHz$; $T_J = 25\ ^\circ C$	0.7	1.8	4.2	Ω
Dynamic characteristics FET1 and FET2						
$Q_{G(tot)}$	total gate charge	$I_D = 10\ A$; $V_{DS} = 32\ V$; $V_{GS} = 10\ V$; $T_J = 25\ ^\circ C$; Fig. 13 ; Fig. 14	-	13	19.4	nC
		$I_D = 10\ A$; $V_{DS} = 32\ V$; $V_{GS} = 5\ V$; $T_J = 25\ ^\circ C$; Fig. 13 ; Fig. 14	-	6.8	10.2	nC
Q_{GS}	gate-source charge		-	2.3	3.8	nC
Q_{GD}	gate-drain charge		-	1.8	4.2	nC
C_{iss}	input capacitance	$V_{DS} = 25\ V$; $V_{GS} = 0\ V$; $f = 1\ MHz$; $T_J = 25\ ^\circ C$; Fig. 15	-	848	1160	pF
C_{oss}	output capacitance		-	280	420	pF
C_{rss}	reverse transfer capacitance		-	39	84	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 32\ V$; $R_L = 3.2\ \Omega$; $V_{GS} = 5\ V$; $R_{G(ext)} = 5\ \Omega$; $T_J = 25\ ^\circ C$	-	6.5	-	ns
t_r	rise time		-	9.7	-	ns
$t_{d(off)}$	turn-off delay time		-	10.1	-	ns

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_f	fall time		-	7.8	-	ns
Source-drain diode FET1 and FET2						
V_{SD}	source-drain voltage	$I_S = 10\text{ A}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 16	-	0.81	1	V
t_{rr}	reverse recovery time	$I_S = 10\text{ A}$; $di_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$;	-	21.5	-	ns
Q_r	recovered charge	$V_{DS} = 20\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$	[1]	16.2	-	nC

[1] Includes capacitive recovery

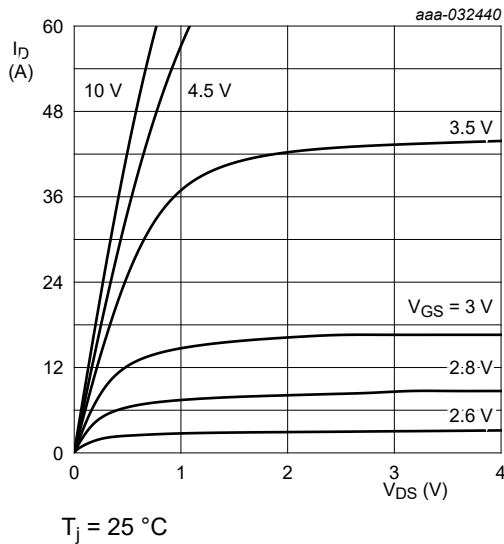


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values, FET1 and FET2

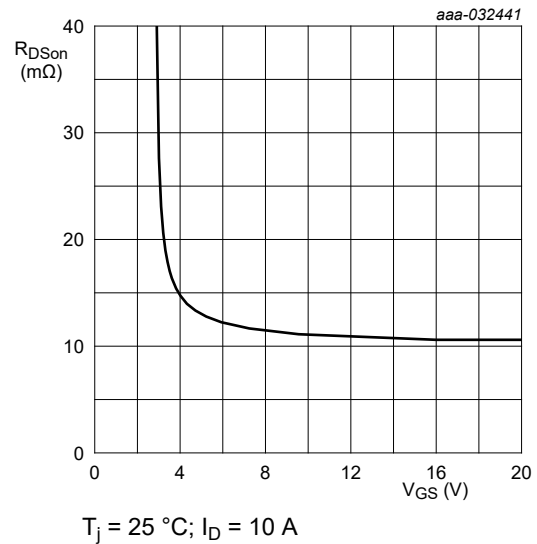


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values. FET1 and FET2

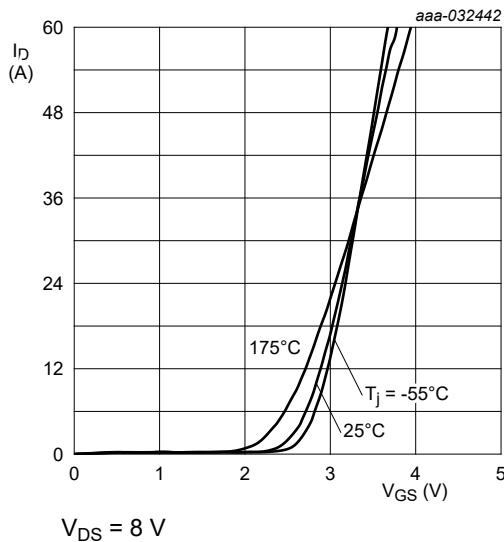


Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values, FET1 and FET2

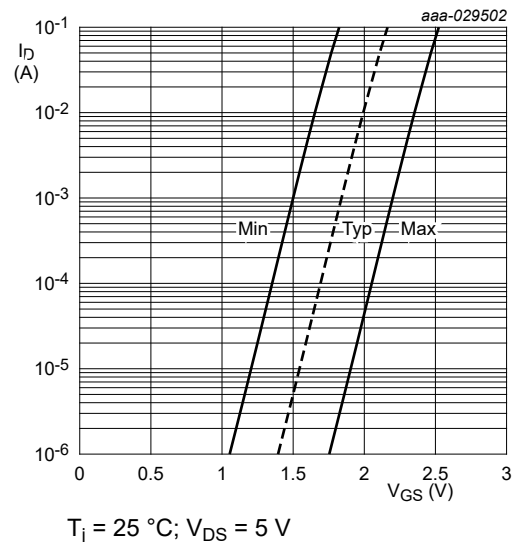


Fig. 9. Sub-threshold drain current as a function of gate-source voltage, FET1 and FET2

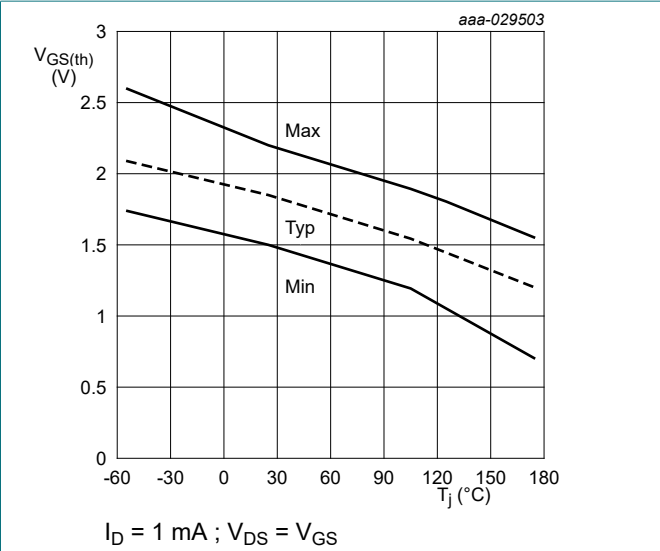


Fig. 10. Gate-source threshold voltage as a function of junction temperature, FET1 and FET2

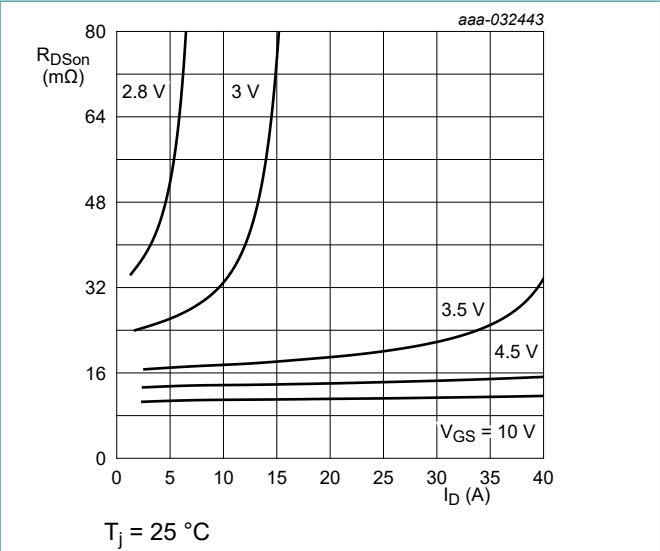


Fig. 11. Drain-source on-state resistance as a function of drain current; typical values, FET1 and FET2

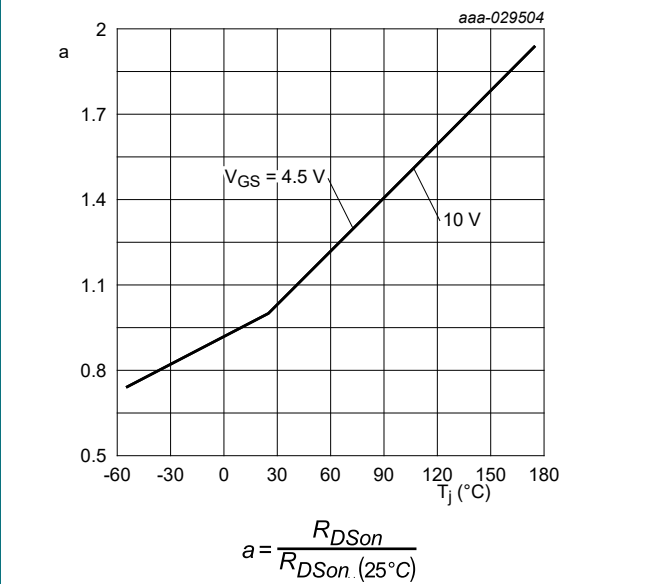


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature, FET1 and FET2

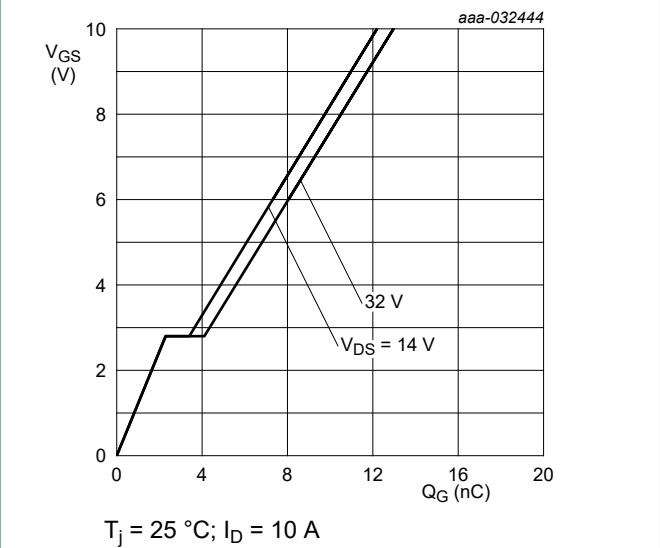


Fig. 13. Gate-source voltage as a function of gate charge; typical values, FET1 and FET2

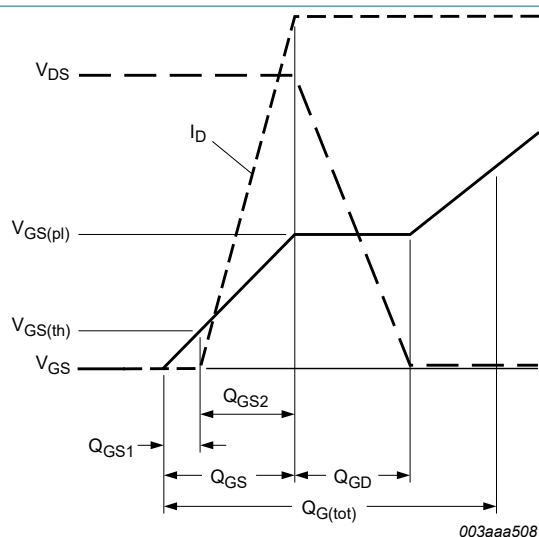


Fig. 14. Gate charge waveform definitions

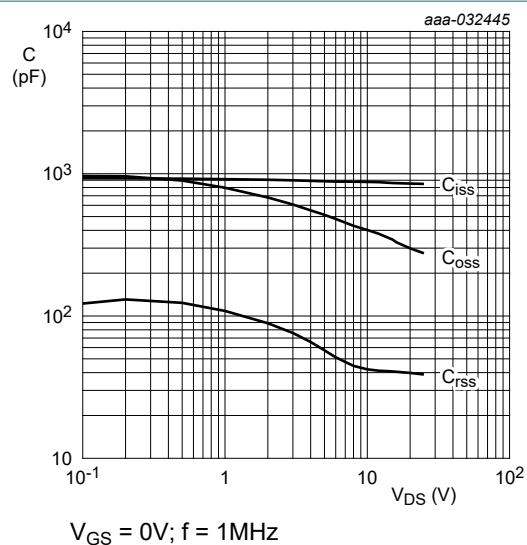


Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values, FET1 and FET2

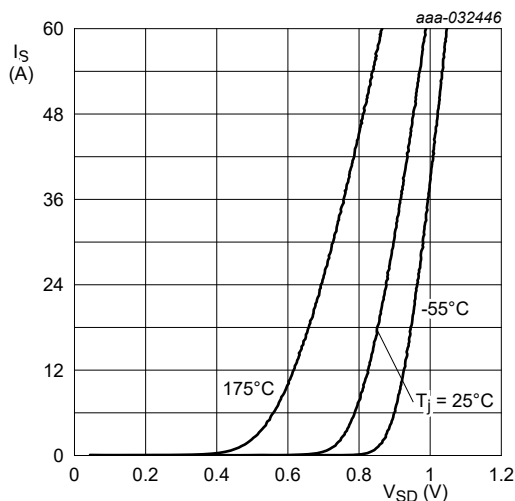

$$V_{GS} = 0 \text{ V}$$

Fig. 16. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values FET1 and FET2

11. Package outline

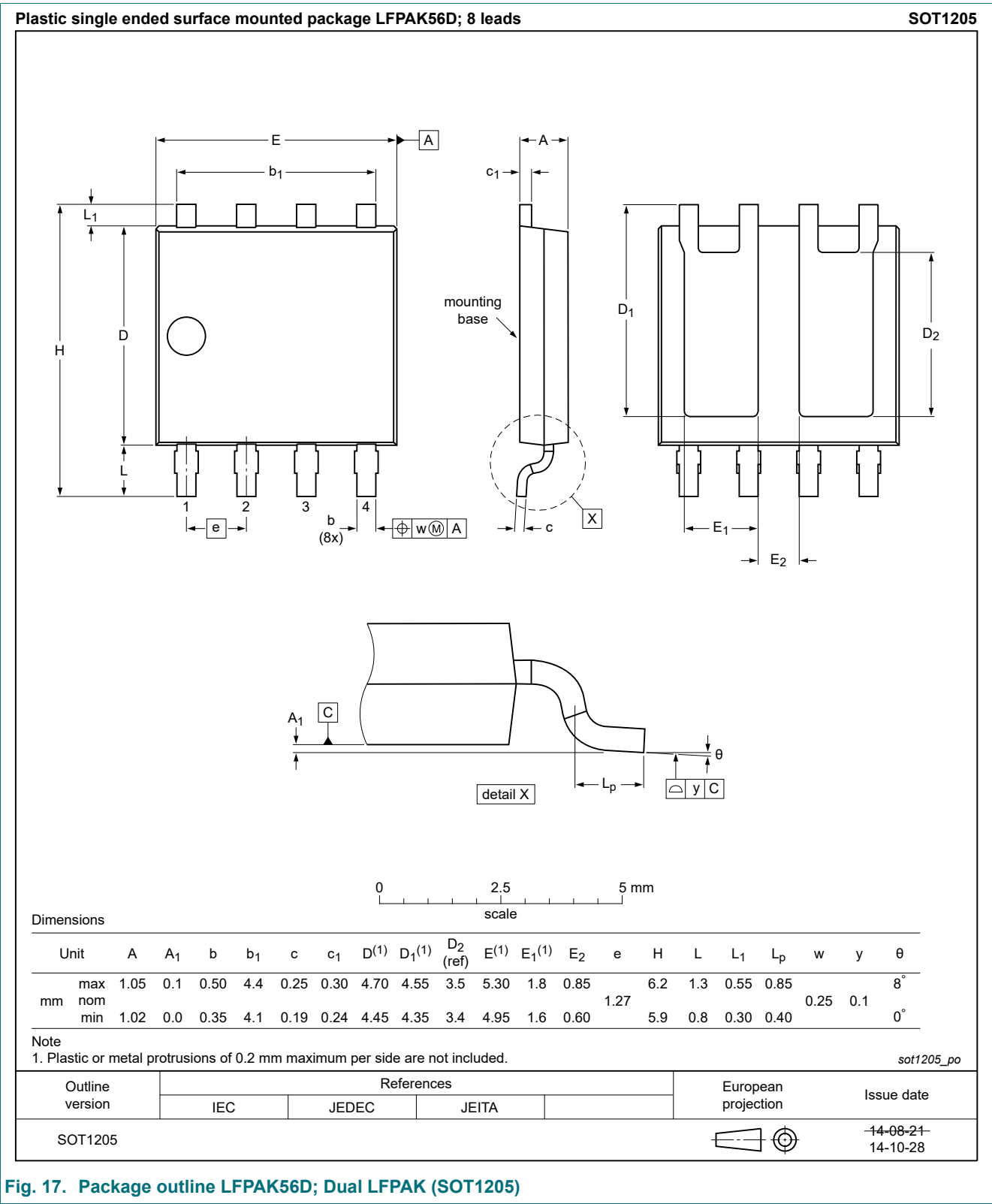


Fig. 17. Package outline LPAK56D; Dual LPAK (SOT1205)

12. Soldering

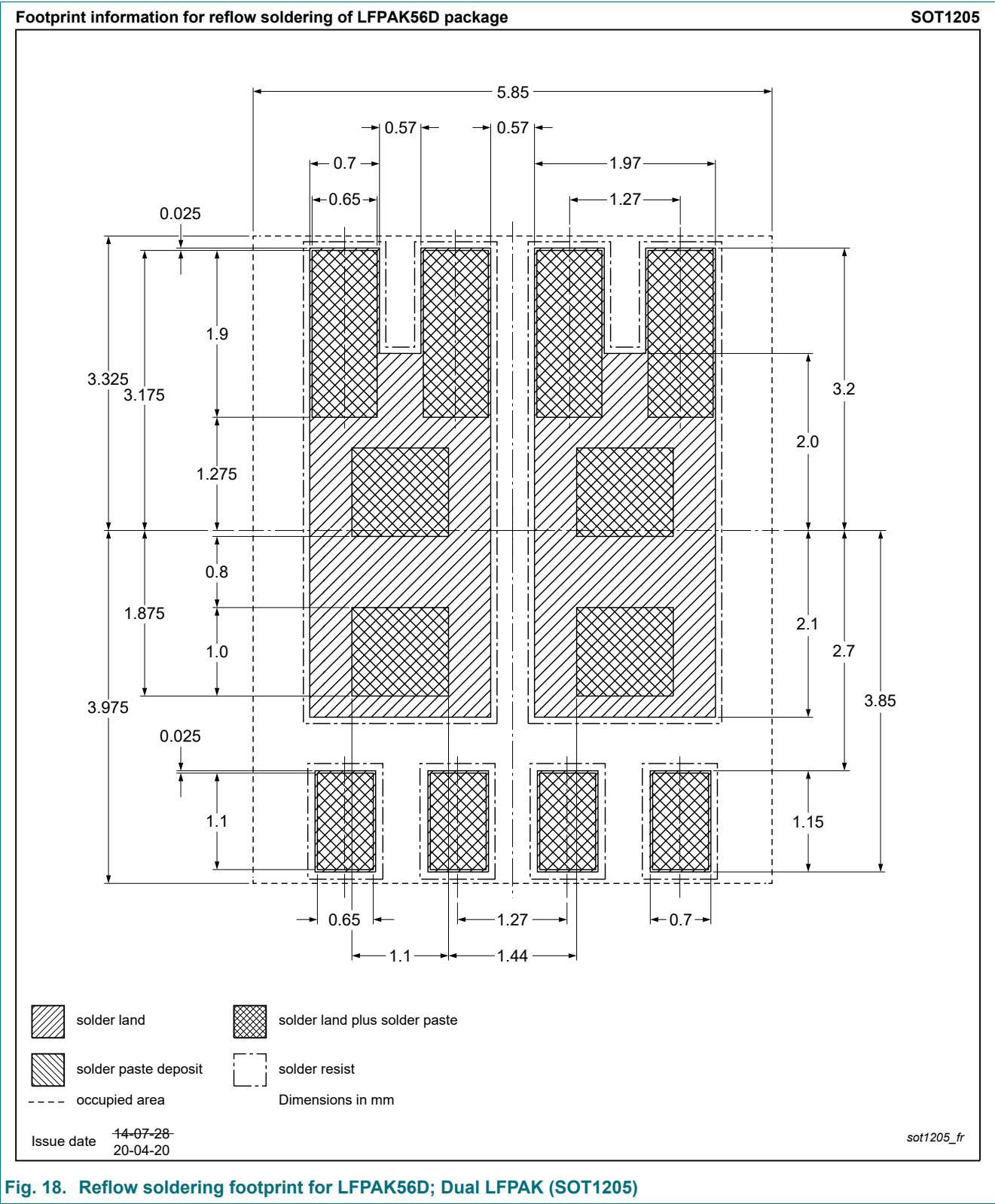


Fig. 18. Reflow soldering footprint for LPAK56D; Dual LPAK (SOT1205)

13. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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