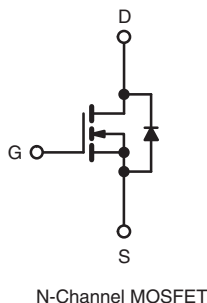
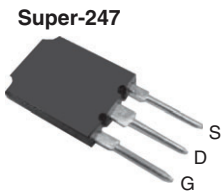


Power MOSFET



FEATURES

- Superfast body diode eliminates the need for external diodes in ZVS applications
- Lower gate charge results in simple drive requirements
- Enhanced dV/dt capabilities offer improved ruggedness
- Higher gate voltage threshold offers improved noise immunity
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Zero voltage switching SMPS
- Telecom and server power supplies
- Uninterruptible power supplies
- Motor control applications

PRODUCT SUMMARY

V_{DS} (V)	600	
$R_{DS(on)}$ (Ω)	$V_{GS} = 10\text{ V}$	0.12
Q_g (Max.) (nC)	320	
Q_{gs} (nC)	85	
Q_{gd} (nC)	160	
Configuration	Single	

ORDERING INFORMATION

Package	Super-247
Lead (Pb)-free and halogen-free	SiHFPS38N60L-GE3

ABSOLUTE MAXIMUM RATINGS ($T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V_{DS}	600	V
Gate-source voltage	V_{GS}	± 30	
Continuous drain current	$V_{GS} \text{ at } 10\text{ V}$	$T_C = 25\text{ }^\circ\text{C}$	A
		$T_C = 100\text{ }^\circ\text{C}$	
Pulsed drain current ^a	I_{DM}	150	
Linear derating factor		4.3	W/ $^\circ\text{C}$
Single pulse avalanche energy ^b	E_{AS}	680	mJ
Repetitive avalanche current ^a	I_{AR}	38	A
Repetitive avalanche energy ^a	E_{AR}	54	mJ
Maximum power dissipation	P_D	540	W
Peak diode recovery dV/dt ^c	dV/dt	19	V/ns
Operating junction and storage temperature range	T_J, T_{stg}	- 55 to + 150	$^\circ\text{C}$
Soldering recommendations (peak temperature)	for 10 s	300 ^d	
Mounting torque	6-32 or M3 screw	10	lbf · in
		1.1	N · m

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 12)
- Starting $T_J = 25\text{ }^\circ\text{C}$, $L = 0.91\text{ mH}$, $R_g = 25\text{ }\Omega$, $I_{AS} = 38\text{ A}$, dV/dt = 13 V/ns (see fig. 14a)
- $I_{SD} \leq 38\text{ A}$, dI/dt $\leq 630\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DS}$, $T_J \leq 150\text{ }^\circ\text{C}$
- 1.6 mm from case

**THERMAL RESISTANCE RATINGS**

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	R_{thJA}	-	40	°C/W
Case-to-sink, flat, greased surface	R_{thCS}	0.24	-	
Maximum junction-to-case (drain)	R_{thJC}	-	0.22	

SPECIFICATIONS ($T_J = 25\text{ °C}$, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA		600	-	-	V
V _{DS} temperature coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = 1 mA		-	410	-	mV/°C
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		3.0	-	5.0	V
Gate-source leakage	I _{GSS}	V _{GS} = ± 30 V		-	-	± 100	nA
Zero gate voltage drain current	I _{DSS}	V _{DS} = 600 V, V _{GS} = 0 V		-	-	50	μA
		V _{DS} = 480 V, V _{GS} = 0 V, T _J = 125 °C		-	-	2.0	mA
Drain-source on-state resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 23 A ^b	-	0.12	0.15	Ω
Forward transconductance	g _{fs}	V _{DS} = 50 V, I _D = 23 A ^b		20	-	-	S
Dynamic							
Input capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1.0 MHz, see fig. 5		-	7990	-	pF
Output capacitance	C _{Oss}			-	740	-	
Reverse transfer capacitance	C _{rss}			-	72	-	
Effective output capacitance	C _{Oss} eff.	V _{GS} = 0 V V _{DS} = 0 V to 480 V ^c		-	350	-	
Effective output capacitance (energy related)	C _{Oss} eff. (ER)			-	260	-	
Total gate charge	Q _g	V _{GS} = 10 V	I _D = 38 A, V _{DS} = 480 V see fig. 7 and 15 ^b	-	-	320	nC
Gate-source charge	Q _{gs}			-	-	85	
Gate-drain charge	Q _{gd}			-	-	160	
Gate resistance	R _G	f = 1 MHz, open drain		-	1.2	-	Ω
Turn-on delay time	t _{d(on)}	V _{DD} = 300 V, I _D = 38 A, R _G = 4.3 Ω, V _{GS} = 10 V, see fig. 11a and 11b ^b		-	44	-	ns
Rise time	t _r			-	130	-	
Turn-off delay time	t _{d(off)}			-	92	-	
Fall time	t _f			-	69	-	
Drain-source body diode characteristics							
Continuous source-drain diode current	I _S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	38	A
Pulsed diode forward current ^a	I _{SM}			-	-	150	
Body diode voltage	V _{SD}	T _J = 25 °C, I _S = 38 A, V _{GS} = 0 V ^b		-	-	1.5	V
Body diode reverse recovery time	t _{rr}	T _J = 25 °C, I _F = 38 A		-	170	250	ns
		T _J = 125 °C, dI/dt = 100 A/μs ^b		-	420	630	
Body diode reverse recovery charge	Q _{rr}	T _J = 25 °C, I _F = 38 A, V _{GS} = 0 V ^b		-	830	1240	nC
		T _J = 125 °C, dI/dt = 100 A/μs ^b		-	2600	3900	
Reverse recovery time	I _{RRM}	T _J = 25 °C		-	9.1	14	A
Forward turn-On time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)					

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 12)
- b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$
- c. $C_{oss\text{ eff.}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS}
 $C_{oss\text{ eff. (ER)}}$ is a fixed capacitance that stores the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS}



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

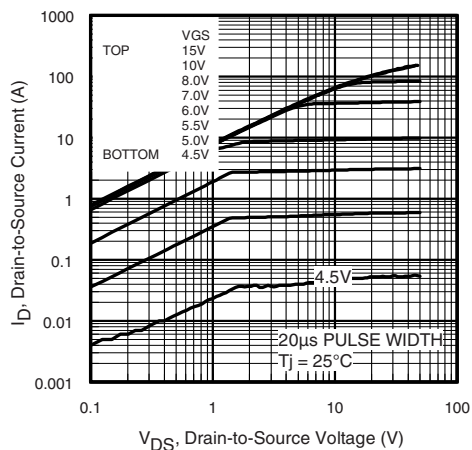


Fig. 1 - Typical Output Characteristics

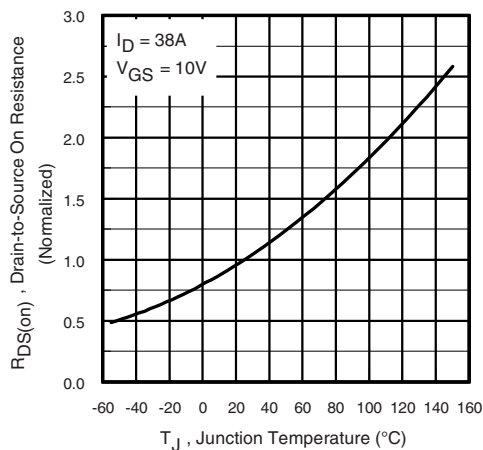


Fig. 4 - Normalized On-Resistance vs. Temperature

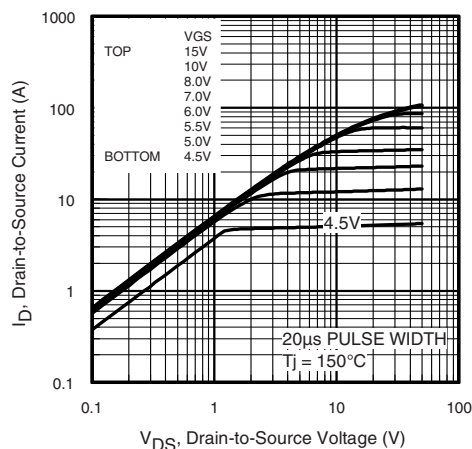


Fig. 2 - Typical Output Characteristics

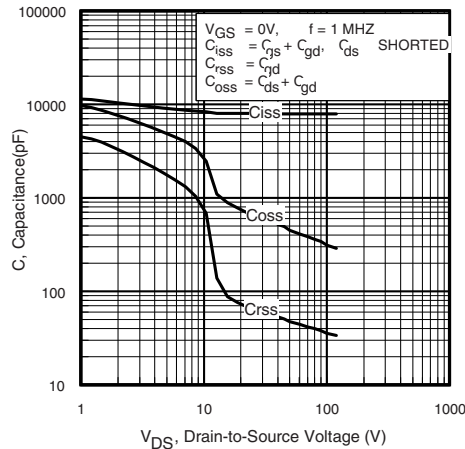


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

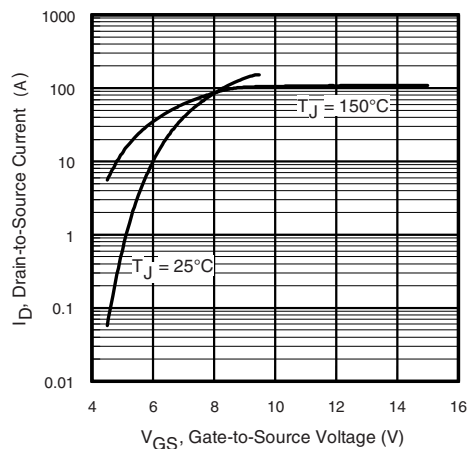


Fig. 3 - Typical Transfer Characteristics

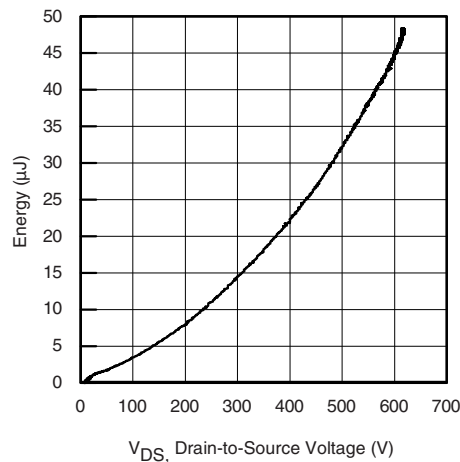
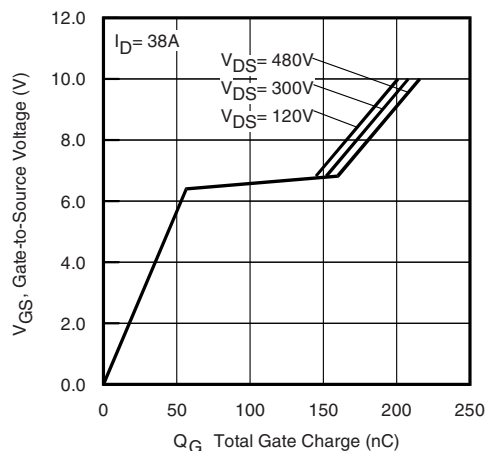
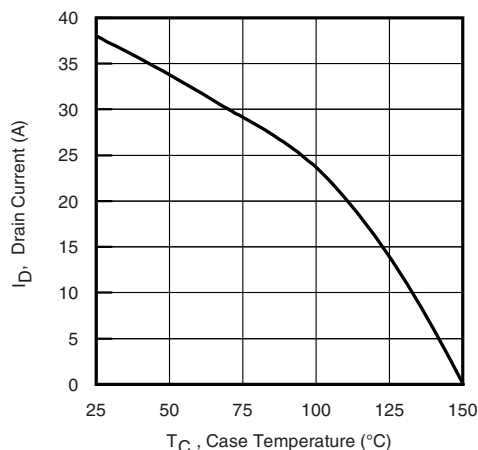
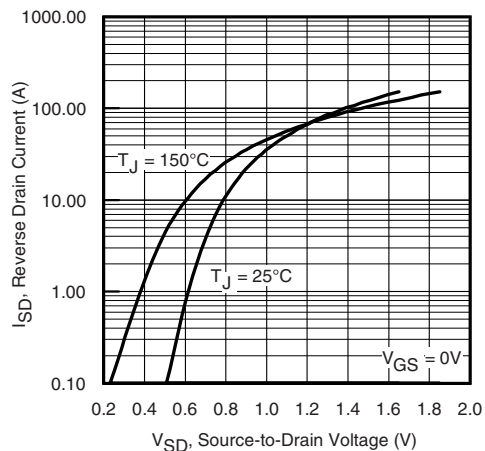
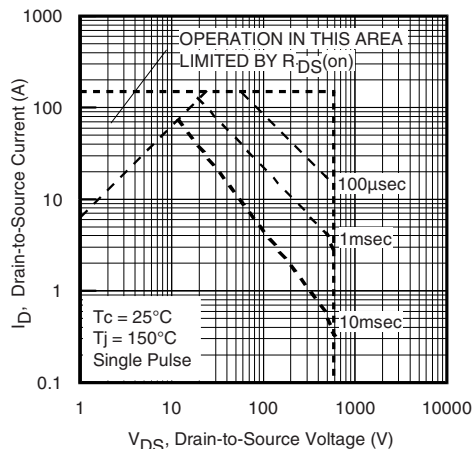
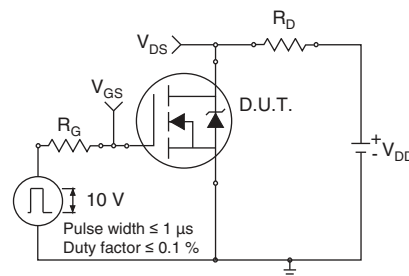
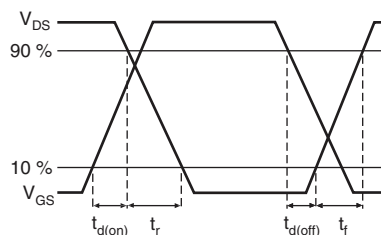
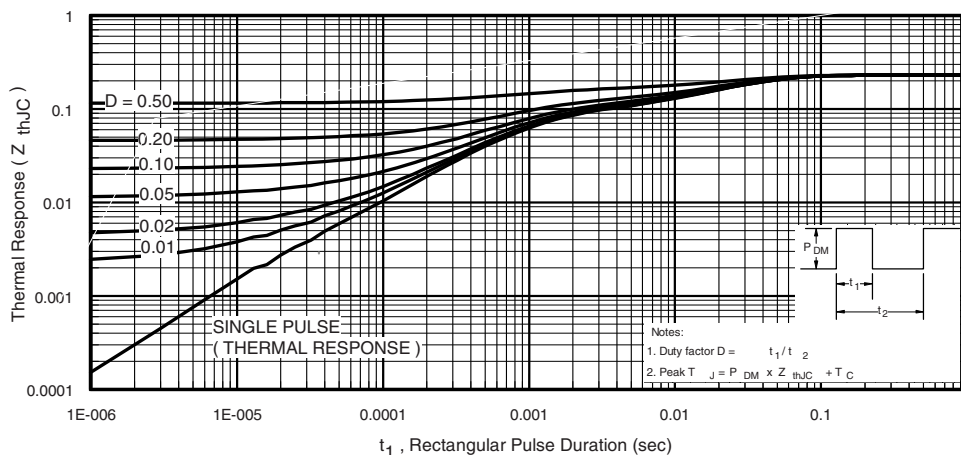
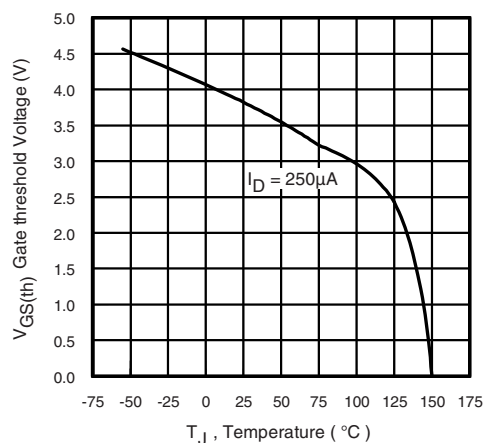
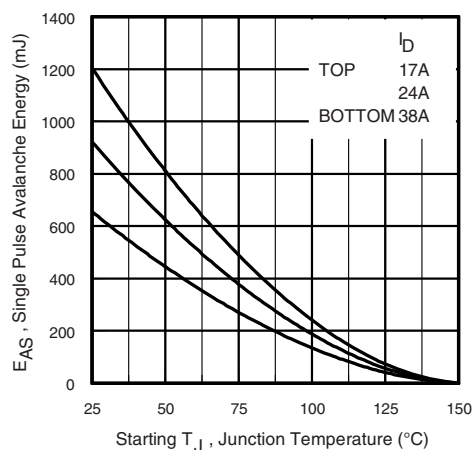
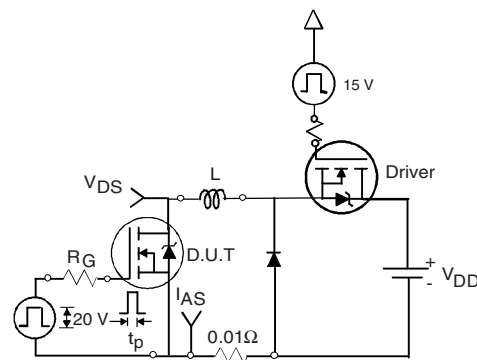
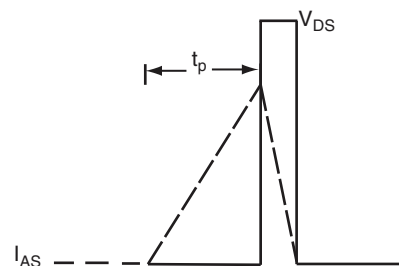
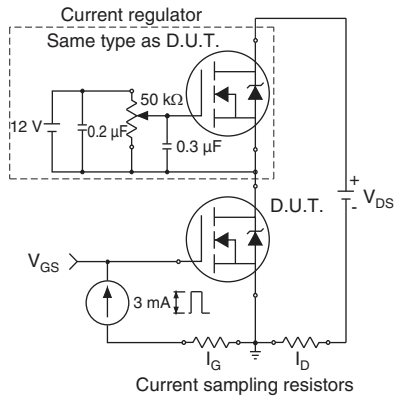
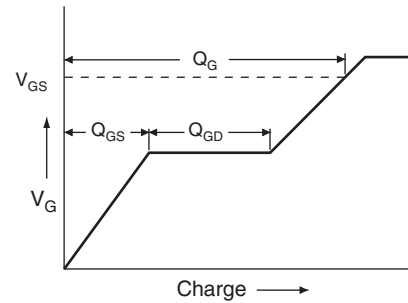
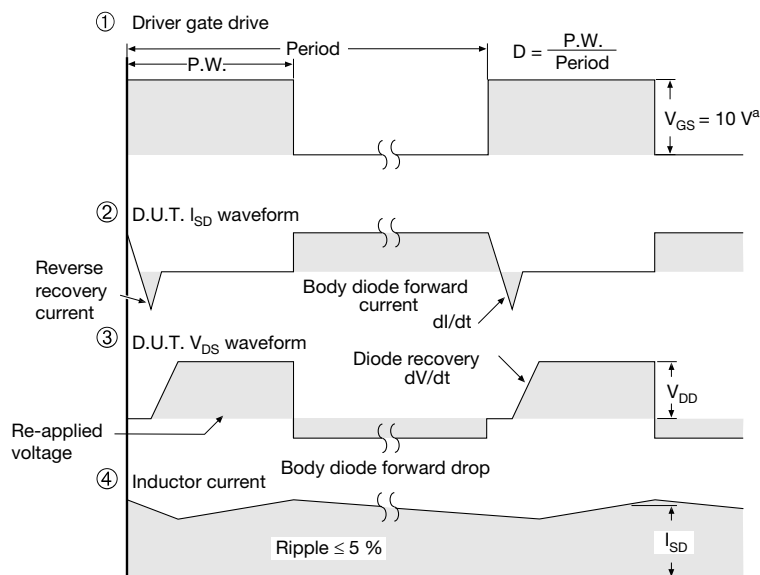
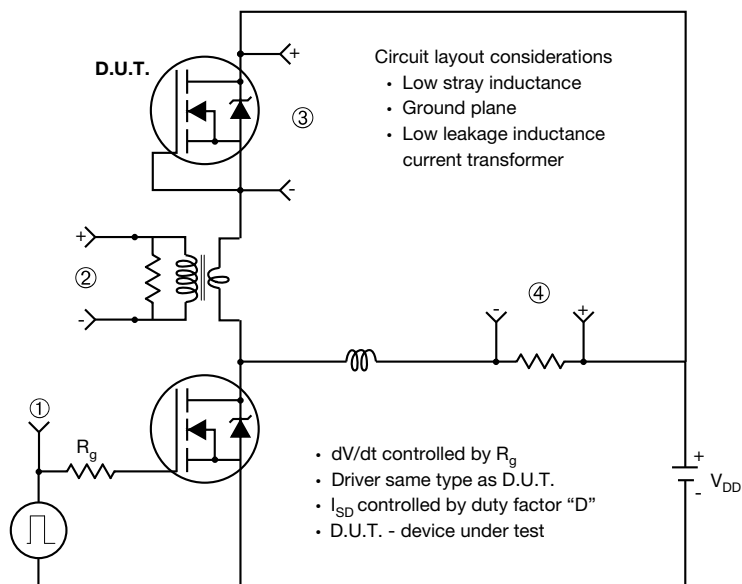


Fig. 1 - Typical Output Capacitance Stored Energy vs. VDS


Fig. 2 - Typical Gate Charge vs. Gate-to-Source Voltage

Fig. 10 - Maximum Drain Current vs. Case Temperature

Fig. 8 - Typical Source-Drain Diode Forward Voltage

Fig. 9 - Maximum Safe Operating Area

Fig. 11a - Switching Time Test Circuit

Fig. 11b - Switching Time Waveforms


Fig. 10 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

Fig. 13 - Threshold Voltage vs. Temperature

Fig. 14a - Maximum Avalanche Energy vs. Drain Current

Fig. 14b - Unclamped Inductive Test Circuit

Fig. 14c - Unclamped Inductive Waveforms


Fig. 15a - Basic Gate Charge Waveform

Fig. 15b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit

Note

a. $V_{GS} = 5 V$ for logic level devices

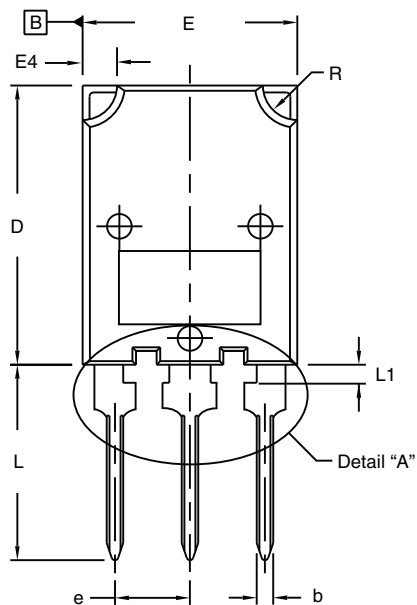
Fig. 16 - For N-Channel

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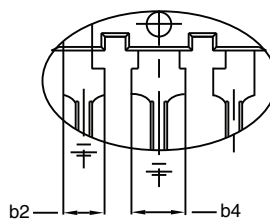
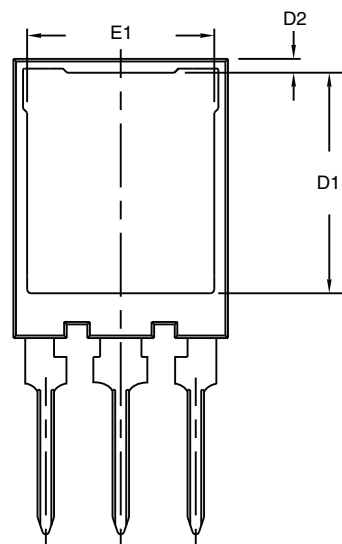
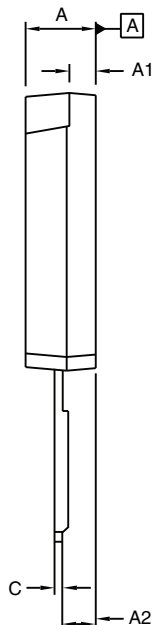
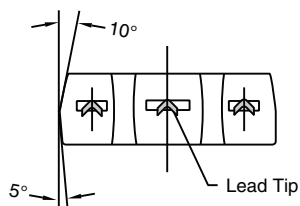


TO-274AA (High Voltage)

VERSION 1: FACILITY CODE = Y



⌀ 0.10 (0.25) Ⓜ B A Ⓜ



Detail "A"
Scale: 2:1

DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.70	5.30	0.185	0.209
A1	1.50	2.50	0.059	0.098
A2	2.25	2.65	0.089	0.104
b	1.30	1.60	0.051	0.063
b2	1.80	2.20	0.071	0.087
b4	3.00	3.25	0.118	0.128
c ⁽¹⁾	0.38	0.89	0.015	0.035
D	19.80	20.80	0.780	0.819

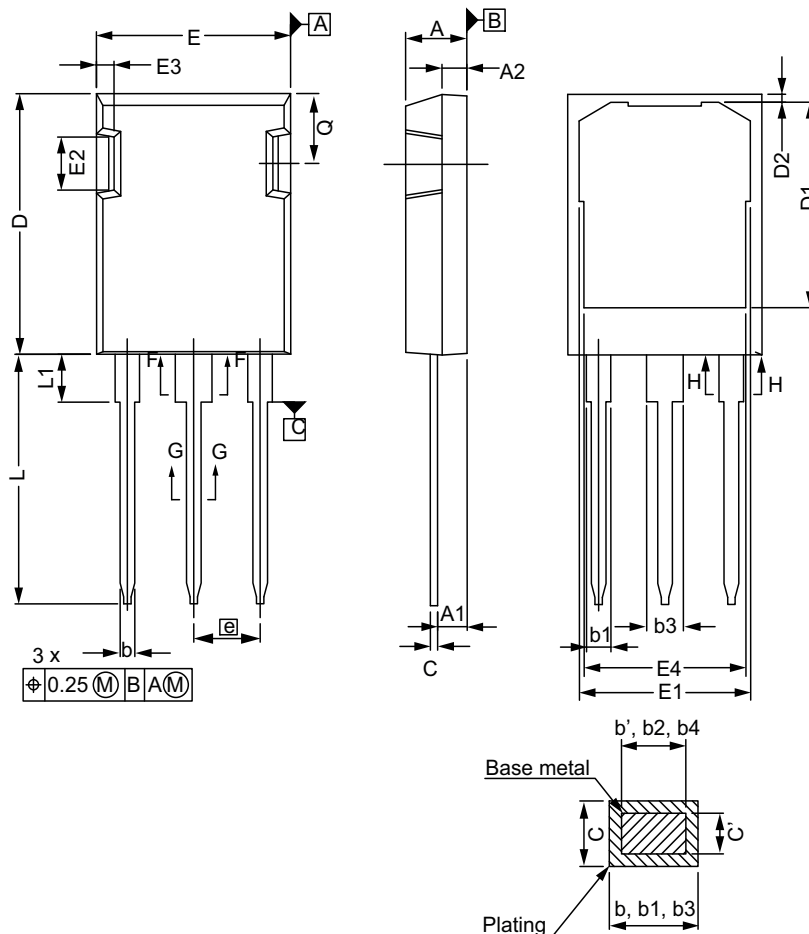
DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
D1	15.50	16.10	0.610	0.634
D2	0.70	1.30	0.028	0.051
E	15.10	16.10	0.594	0.634
E1	13.30	13.90	0.524	0.547
e	5.45 BSC		0.215 BSC	
L	13.70	14.70	0.539	0.579
L1	1.00	1.60	0.039	0.063
R	2.00	3.00	0.079	0.118

Notes

- Dimensioning and tolerancing per ASME Y14.5M-1994
- Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outer extremes of the plastic body
- Outline conforms to JEDEC® outline to TO-274AA
- ⁽¹⁾ Dimension measured at tip of lead



VERSION 2: FACILITY CODE = N



SECTION "F-F", "G-G" AND "H-H"
SCALE: NONE

	MILLIMETERS	
DIM.	MIN.	MAX.
A	4.83	5.21
A1	2.29	2.54
A2	1.91	2.16
b'	1.07	1.28
b	1.07	1.33
b1	1.91	2.41
b2	1.91	2.16
b3	2.87	3.38
b4	2.87	3.13
c'	0.55	0.65
c	0.55	0.68
D	20.80	21.10

	MILLIMETERS	
DIM.	MIN.	MAX.
D1	16.25	17.65
D2	0.50	0.80
E	15.75	16.13
E1	13.10	14.15
E2	3.68	5.10
E3	1.00	1.90
E4	12.38	13.43
e	5.44 BSC	
N	3	
L	19.81	20.32
L1	3.70	4.00
Q	5.49	6.00

ECN: E20-0538-Rev. C, 19-Oct-2020
DWG: 5975

Notes

- Dimensioning and tolerancing per ASME Y14.5M-1994
- Outline conforms to JEDEC® outline to TO-274AD
- Dimensions are measured in mm, angles are in degree
- Metal surfaces are tin plated, except area of cut



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