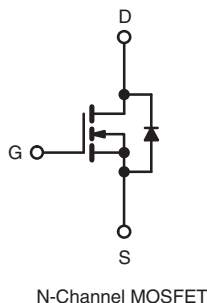
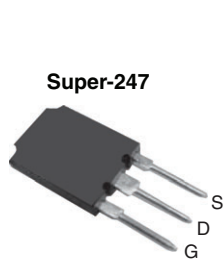


Power MOSFET



FEATURES

- Low gate charge Q_g results in simple drive requirement
- Improved gate, avalanche and dynamic dV/dt ruggedness
- Fully characterized capacitance and avalanche voltage and current
- Effective C_{oss} specified
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

PRODUCT SUMMARY

V_{DS} (V)	500	
$R_{DS(on)}$ (Max.) (Ω)	$V_{GS} = 10\text{ V}$	0.13
Q_g (Max.) (nC)	180	
Q_{gs} (nC)	46	
Q_{gd} (nC)	71	
Configuration	Single	

APPLICATIONS

- Switch mode power supply (SMPS)
- Uninterruptible power supply
- High speed power switching

TYPICAL SMPS TOPOLOGIES

- Full bridge converters
- Power factor correction boost

ORDERING INFORMATION

Package	Super-247
Lead (Pb)-free and halogen-free	SiHFPS37N50A-GE3

ABSOLUTE MAXIMUM RATINGS ($T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V_{DS}	500	V
Gate-source voltage	V_{GS}	± 30	
Continuous drain current	$V_{GS} \text{ at } 10\text{ V}$	$T_C = 25\text{ }^\circ\text{C}$	A
		$T_C = 100\text{ }^\circ\text{C}$	
Pulsed drain current ^a	I_{DM}	144	
Linear derating factor		3.6	W/ $^\circ\text{C}$
Single pulse avalanche energy ^b	E_{AS}	1260	mJ
Repetitive avalanche current ^a	I_{AR}	36	A
Repetitive avalanche energy ^a	E_{AR}	44	mJ
Maximum power dissipation	P_D	446	W
Peak diode recovery dV/dt ^c	dV/dt	3.5	V/ns
Operating junction and storage temperature range	T_J, T_{stg}	- 55 to + 150	$^\circ\text{C}$
Soldering recommendations (peak temperature)	for 10 s	300 ^d	

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- Starting $T_J = 25\text{ }^\circ\text{C}$, $L = 1.94\text{ mH}$, $R_g = 25\text{ }\Omega$, $I_{AS} = 36\text{ A}$ (see fig. 12)
- $I_{SD} \leq 36\text{ A}$, $dI/dt \leq 145\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DS}$, $T_J \leq 150\text{ }^\circ\text{C}$
- 1.6 mm from case

**THERMAL RESISTANCE RATINGS**

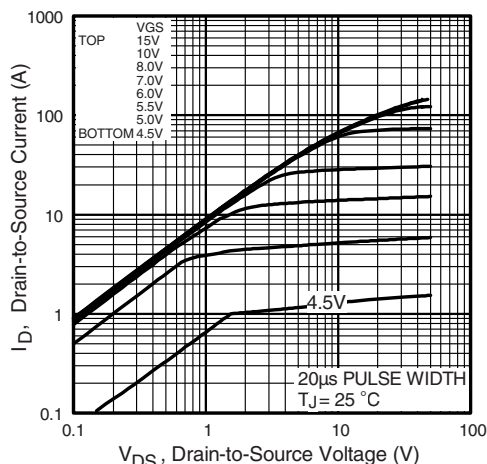
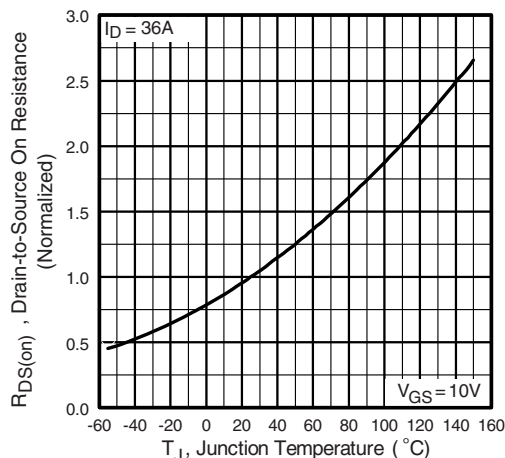
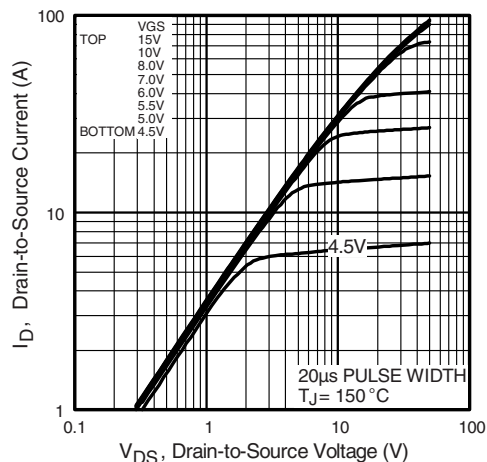
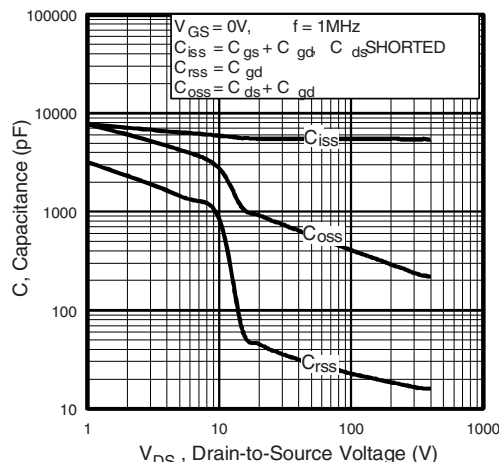
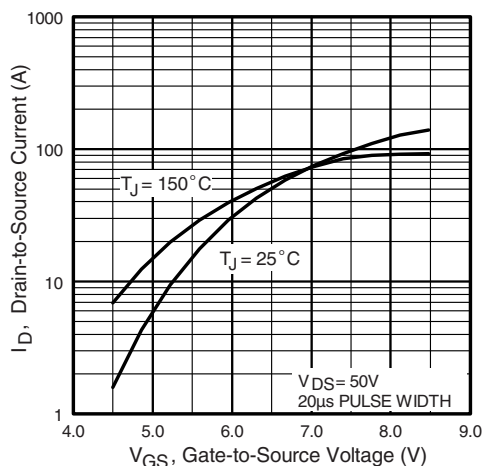
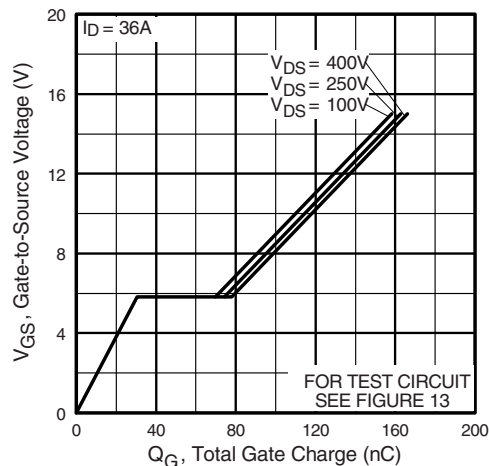
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	R_{thJA}	-	40	°C/W
Case-to-sink, flat, greased surface	R_{thCS}	0.24	-	
Maximum junction-to-case (drain)	R_{thJC}	-	0.28	

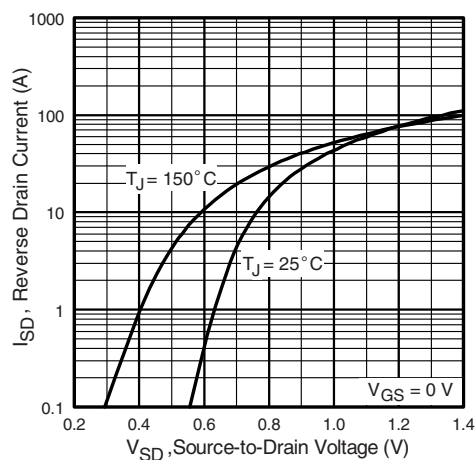
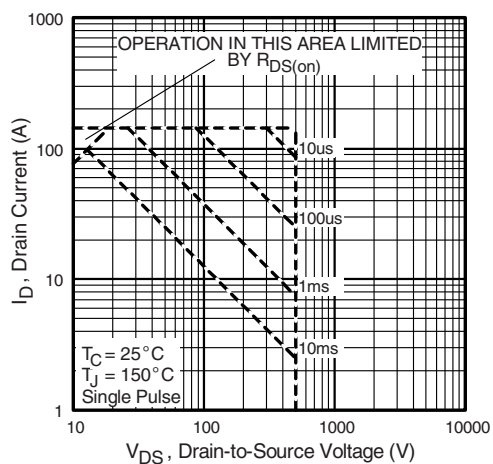
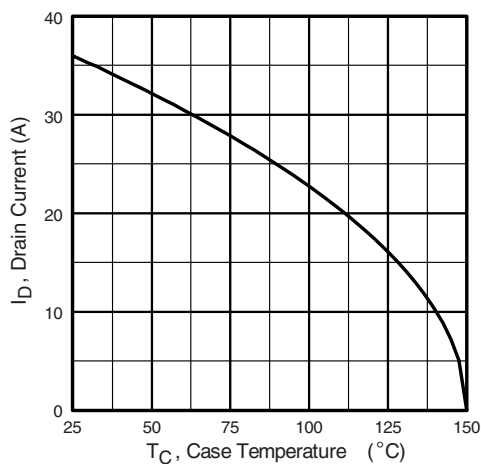
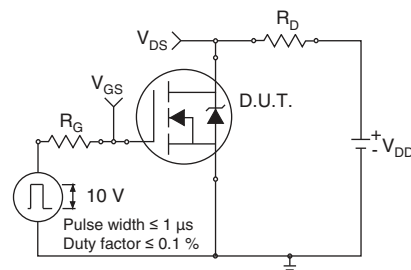
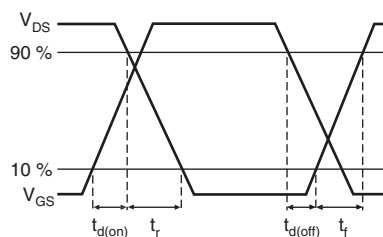
SPECIFICATIONS ($T_J = 25^\circ\text{C}$, unless otherwise noted)

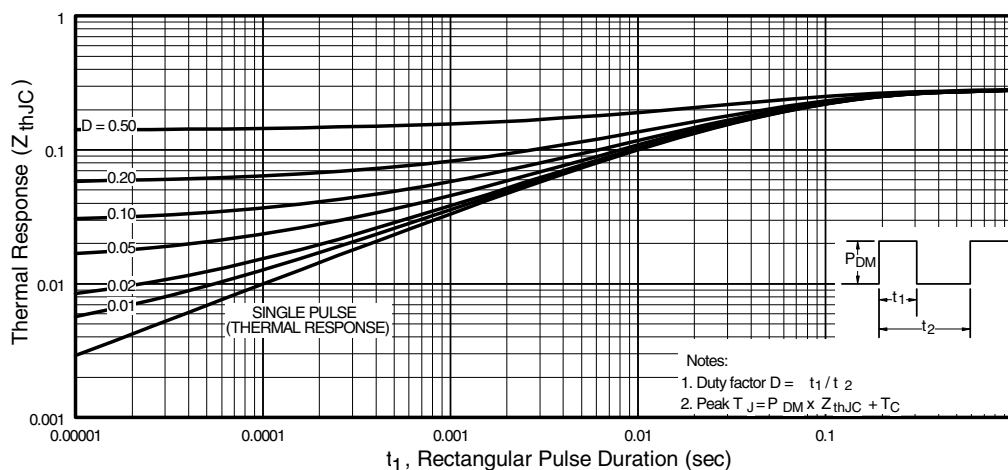
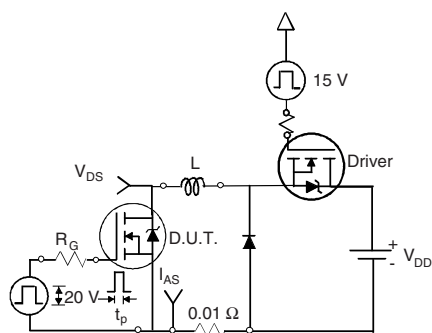
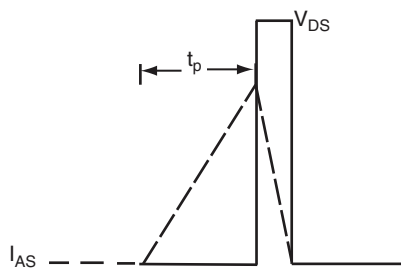
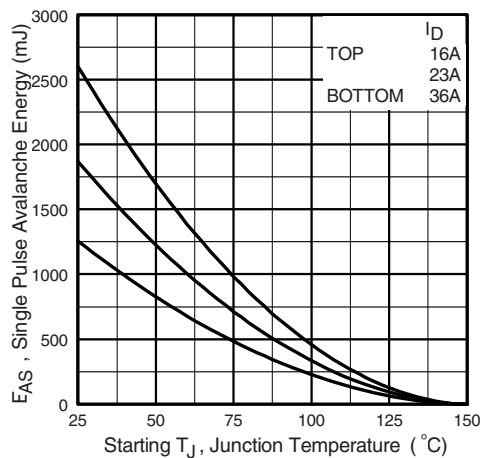
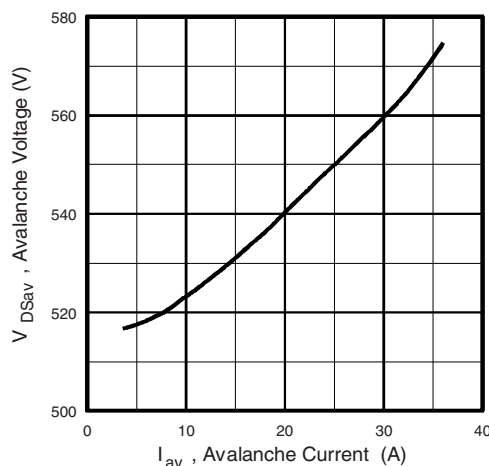
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$		500	-	-	V
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$		2.0	-	4.0	V
Gate-source leakage	I_{GSS}	$V_{GS} = \pm 30\text{ V}$		-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	$V_{DS} = 500\text{ V}$, $V_{GS} = 0\text{ V}$		-	-	25	μA
		$V_{DS} = 400\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 150\text{ }^\circ\text{C}$		-	-	250	
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 22\text{ A}^b$	-	-	0.13	Ω
Forward transconductance	g_{fs}	$V_{DS} = 50\text{ V}$, $I_D = 22\text{ A}^b$		20	-	-	S
Dynamic							
Input capacitance	C_{iss}	$V_{GS} = 0\text{ V}$, $V_{DS} = 25\text{ V}$, $f = 1.0\text{ MHz}$, see fig. 5		-	5579	-	pF
Output capacitance	C_{oss}			-	810	-	
Reverse transfer capacitance	C_{rss}			-	36	-	
Output capacitance	C_{oss}	$V_{GS} = 0\text{ V}$	$V_{DS} = 1.0\text{ V}$, $f = 1.0\text{ MHz}$	-	7905	-	
			$V_{DS} = 400\text{ V}$, $f = 1.0\text{ MHz}$	-	221	-	
Effective output capacitance	$C_{oss\text{ eff.}}$		$V_{DS} = 0\text{ V to } 400\text{ V}$	-	400	-	
Total gate charge	Q_g	$V_{GS} = 10\text{ V}$	$I_D = 36\text{ A}$, $V_{DS} = 400\text{ V}$, see fig. 6 and 13 ^b	-	-	180	nC
Gate-source charge	Q_{gs}			-	-	46	
Gate-drain charge	Q_{gd}			-	-	71	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 250\text{ V}$, $I_D = 36\text{ A}$, $R_G = 2.15\text{ }\Omega$, $R_D = 7.0\text{ }\Omega$, see fig. 10 ^b		-	23	-	ns
Rise time	t_r			-	98	-	
Turn-off delay time	$t_{d(off)}$			-	52	-	
Fall time	t_f			-	80	-	
Drain-source body diode characteristics							
Continuous source-drain diode current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	36	A
Pulsed diode forward current ^a	I_{SM}			-	-	144	
Body diode voltage	V_{SD}	$T_J = 25\text{ }^\circ\text{C}$, $I_S = 36\text{ A}$, $V_{GS} = 0\text{ V}^b$		-	-	1.5	V
Body diode reverse recovery time	t_{rr}	$T_J = 25\text{ }^\circ\text{C}$, $I_F = 36\text{ A}$, $dI/dt = 100\text{ A}/\mu\text{s}^b$		-	570	860	ns
Body diode reverse recovery charge	Q_{rr}			-	8.6	13	μC
Forward turn-on time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)					

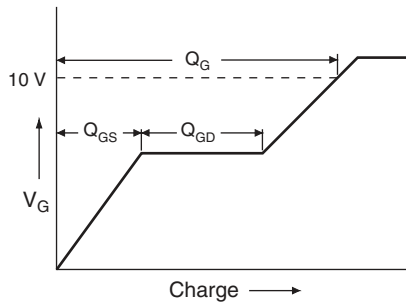
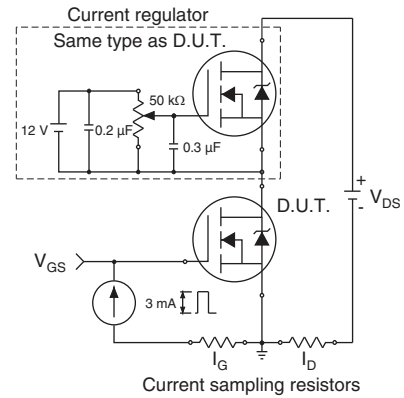
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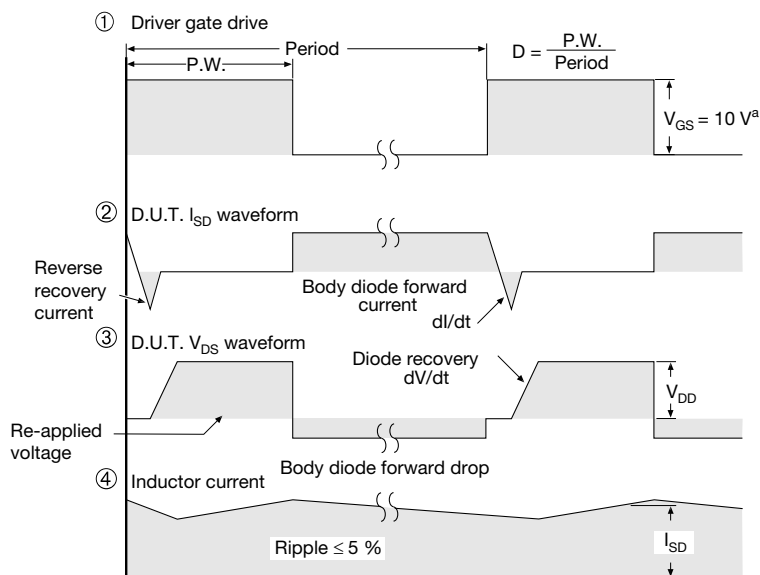
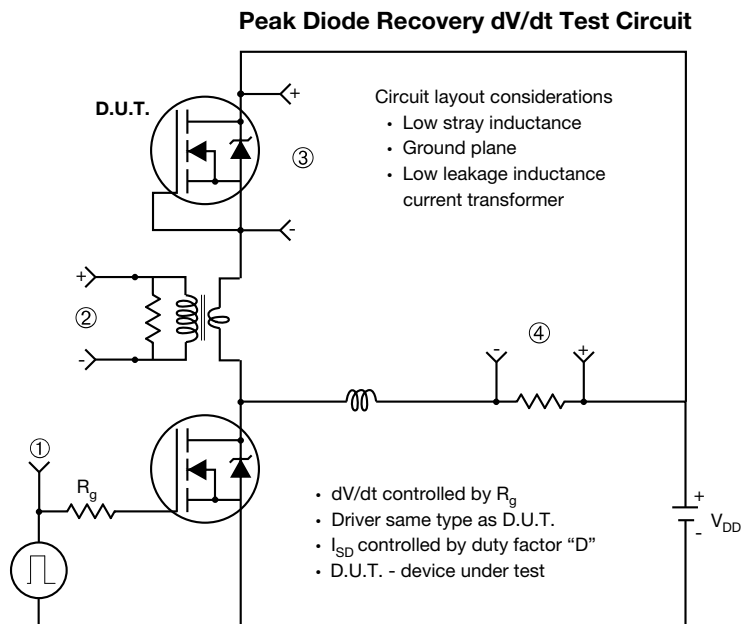
- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$
c. $C_{oss\text{ eff.}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS}

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Fig. 1 - Typical Output Characteristics

Fig. 4 - Normalized On-Resistance vs. Temperature

Fig. 2 - Typical Output Characteristics

Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

Fig. 3 - Typical Transfer Characteristics

Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage


Fig. 7 - Typical Source-Drain Diode Forward Voltage

Fig. 8 - Maximum Safe Operating Area

Fig. 9 - Maximum Drain Current vs. Case Temperature

Fig. 10a - Switching Time Test Circuit

Fig. 10b - Switching Time Waveforms


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

Fig. 12a - Unclamped Inductive Test Circuit

Fig. 12b - Unclamped Inductive Waveforms

Fig. 12c - Maximum Avalanche Energy vs. Drain Current

Fig. 12d - Maximum Avalanche Energy vs. Drain Current


Fig. 13a - Basic Gate Charge Waveform

Fig. 13b - Gate Charge Test Circuit



Note

a. $V_{GS} = 5\text{ V}$ for logic level devices

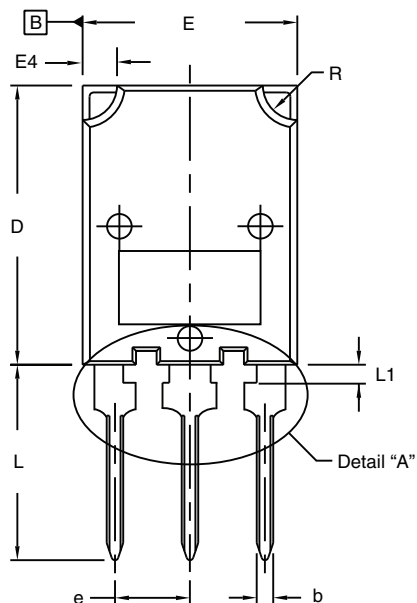
Fig. 14 - For N-Channel

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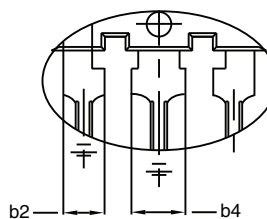
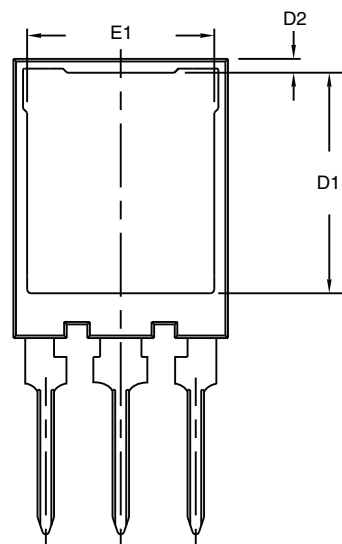
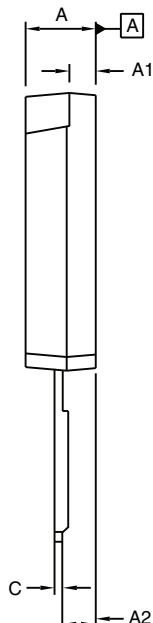
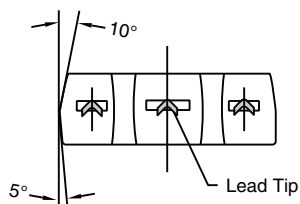


TO-274AA (High Voltage)

VERSION 1: FACILITY CODE = Y



⌀ 0.10 (0.25) ⌀ B A ⌀



Detail "A"
Scale: 2:1

DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.70	5.30	0.185	0.209
A1	1.50	2.50	0.059	0.098
A2	2.25	2.65	0.089	0.104
b	1.30	1.60	0.051	0.063
b2	1.80	2.20	0.071	0.087
b4	3.00	3.25	0.118	0.128
c ⁽¹⁾	0.38	0.89	0.015	0.035
D	19.80	20.80	0.780	0.819

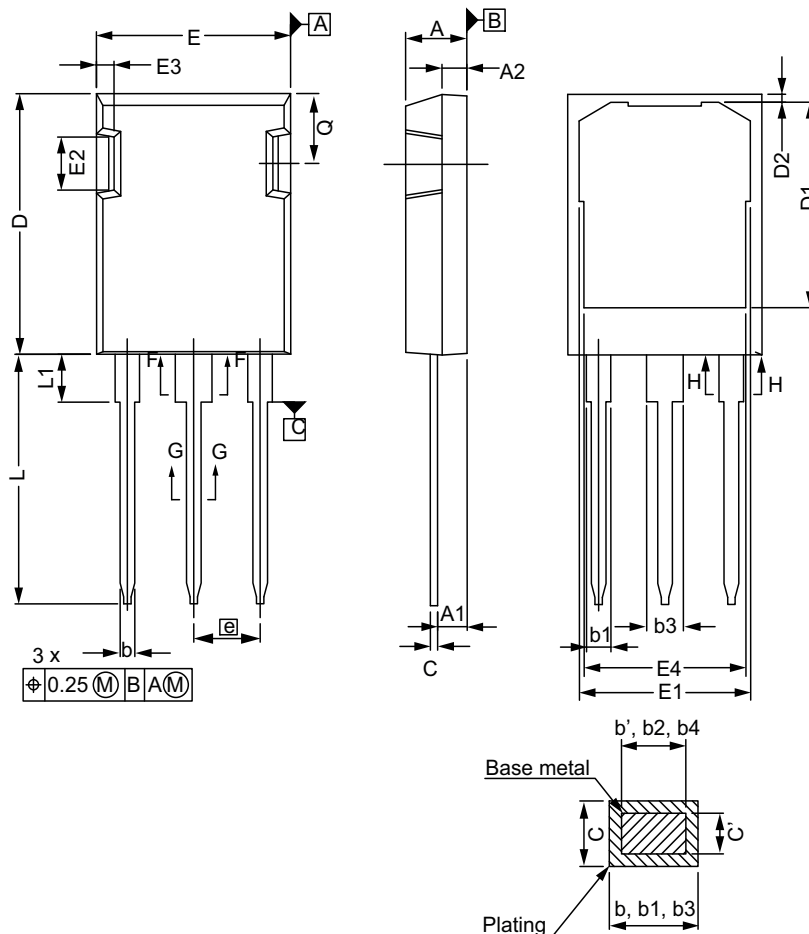
DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
D1	15.50	16.10	0.610	0.634
D2	0.70	1.30	0.028	0.051
E	15.10	16.10	0.594	0.634
E1	13.30	13.90	0.524	0.547
e	5.45 BSC		0.215 BSC	
L	13.70	14.70	0.539	0.579
L1	1.00	1.60	0.039	0.063
R	2.00	3.00	0.079	0.118

Notes

- Dimensioning and tolerancing per ASME Y14.5M-1994
- Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outer extremes of the plastic body
- Outline conforms to JEDEC® outline to TO-274AA
- ⁽¹⁾ Dimension measured at tip of lead



VERSION 2: FACILITY CODE = N



SECTION "F-F", "G-G" AND "H-H"
SCALE: NONE

MILLIMETERS		
DIM.	MIN.	MAX.
A	4.83	5.21
A1	2.29	2.54
A2	1.91	2.16
b'	1.07	1.28
b	1.07	1.33
b1	1.91	2.41
b2	1.91	2.16
b3	2.87	3.38
b4	2.87	3.13
c'	0.55	0.65
c	0.55	0.68
D	20.80	21.10

MILLIMETERS		
DIM.	MIN.	MAX.
D1	16.25	17.65
D2	0.50	0.80
E	15.75	16.13
E1	13.10	14.15
E2	3.68	5.10
E3	1.00	1.90
E4	12.38	13.43
e	5.44 BSC	
N	3	
L	19.81	20.32
L1	3.70	4.00
Q	5.49	6.00

ECN: E20-0538-Rev. C, 19-Oct-2020
DWG: 5975

Notes

- Dimensioning and tolerancing per ASME Y14.5M-1994
- Outline conforms to JEDEC® outline to TO-274AD
- Dimensions are measured in mm, angles are in degree
- Metal surfaces are tin plated, except area of cut



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