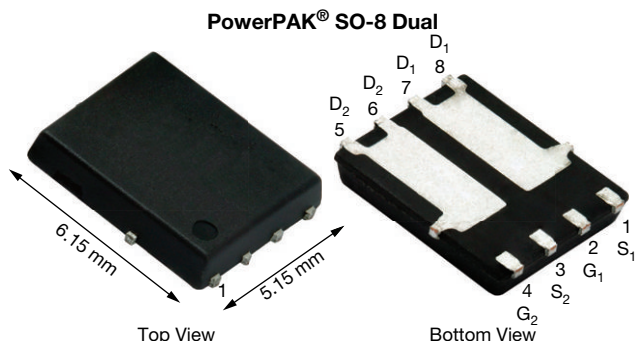


Dual N-Channel 100 V (D-S) MOSFET



FEATURES

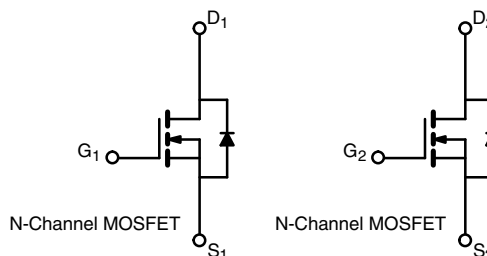
- TrenchFET® power MOSFET
- PWM optimized
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- System power DC/DC



PRODUCT SUMMARY	
V _{DS} (V)	100
R _{DS(on)} max. (Ω) at V _{GS} = 10 V	0.0186
R _{DS(on)} max. (Ω) at V _{GS} = 7.5 V	0.0225
Q _g typ. (nC)	13.1
I _D (A)	28.7 ^a
Configuration	Dual

ORDERING INFORMATION	
Package	PowerPAK SO-8
Lead (Pb)-free and halogen-free	Si7252ADP-T1-GE3

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)				
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-source voltage	V _{DS}	100	V	
Gate-source voltage	V _{GS}	± 20		
Continuous drain current (T _J = 150 °C)	T _C = 25 °C	28.7 ^a	A	
	T _C = 70 °C	23 ^a		
	T _A = 25 °C	9.3 ^a		
	T _A = 70 °C	7.4 ^a		
Pulsed drain current (V _{GS} = 10 V, t = 100 μs)	I _{DM}	70		
Source-drain current diode current	T _C = 25 °C	30.7		
	T _A = 25 °C	3.3 ^{b, c}		
Single pulse avalanche current	L = 0.1 mH	10	mJ	
		5		
Maximum power dissipation	T _C = 25 °C	33.8		



(not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection

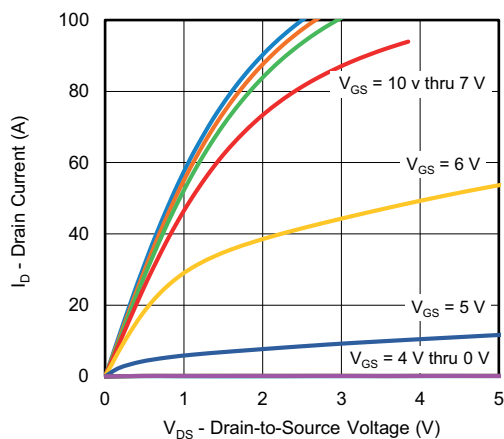
- e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
- f. Maximum under steady state conditions is 85 °C/W



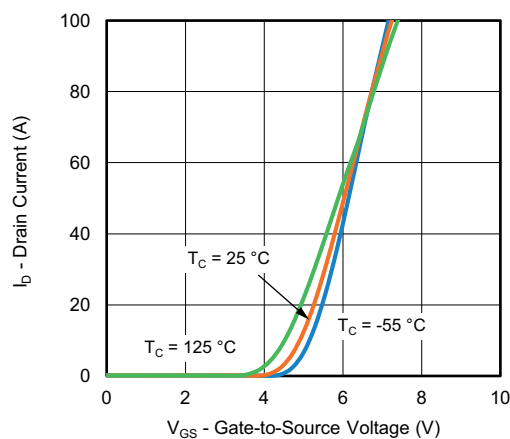
SPECIFICATIONS ($T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$	100	-	-	V
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	$I_D = 10\text{ mA}$	-	81	-	mV/ $^{\circ}\text{C}$
$V_{GS(th)}$ temperature coefficient	$\Delta V_{GS(th)}/T_J$	$I_D = 250\text{ }\mu\text{A}$	-	-7.4	-	
Gate threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2	-	4	V
Gate-body leakage	I_{GSS}	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 20\text{ V}$	-	-	100	nA
Zero gate voltage drain current	I_{DSS}	$V_{DS} = 100\text{ V}$, $V_{GS} = 0\text{ V}$	-	-	1	μA
		$V_{DS} = 100\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 85\text{ }^{\circ}\text{C}$	-	-	10	
On-state drain current ^b	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}$, $V_{GS} = 10\text{ V}$	40	-	-	A
Drain-source on-state resistance ^b	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$, $I_D = 10\text{ A}$	-	0.0155	0.0186	Ω
		$V_{GS} = 7.5\text{ V}$, $I_D = 10\text{ A}$	-	0.0175	0.0225	
Forward transconductance ^b	g_{fs}	$V_{DS} = 15\text{ V}$, $I_D = 10\text{ A}$	-	22	-	S
Dynamic ^a						
Input capacitance	C_{iss}	$V_{DS} = 50\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$	-	1266	-	pF
Output capacitance	C_{oss}		-	123	-	
Reverse transfer capacitance	C_{rss}		-	6	-	
Total gate charge	Q_g	$V_{DS} = 50\text{ V}$, $V_{GS} = 10\text{ V}$, $I_D = 10\text{ A}$	-	17.4	26.5	nC
Gate-source charge	Q_{gs}	$V_{DS} = 50\text{ V}$, $V_{GS} = 7.5\text{ V}$, $I_D = 10\text{ A}$	-	13.1	20	
Gate-drain charge	Q_{gd}		-	7.1	-	
			-	2.3	-	
Gate resistance	R_g	$f = 1\text{ MHz}$	0.2	0.75</		



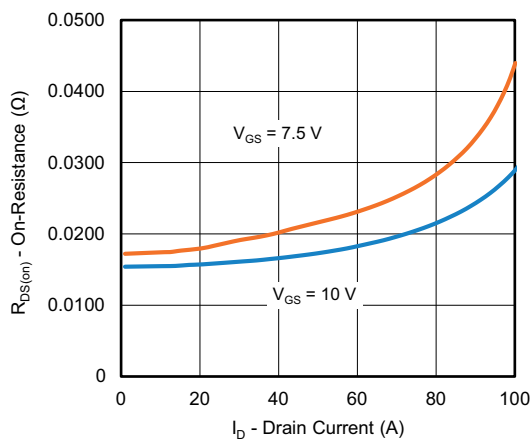
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



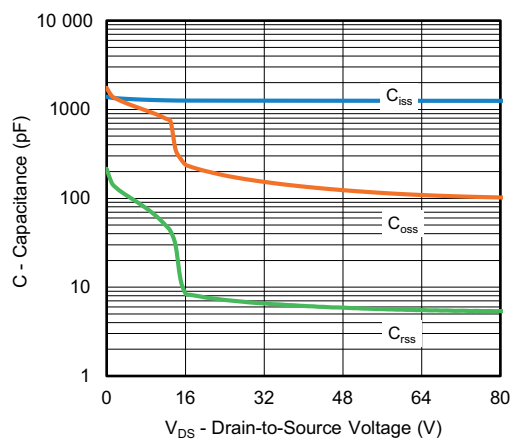
Output Characteristics



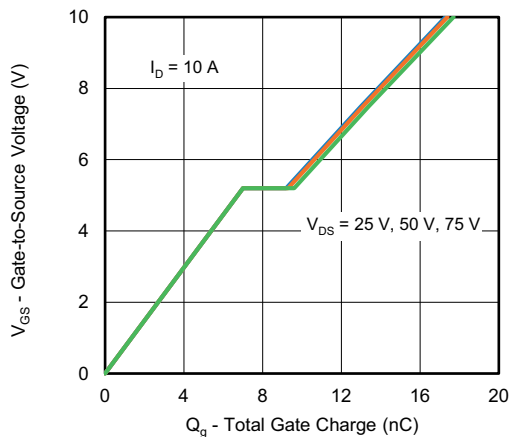
Transfer Characteristics



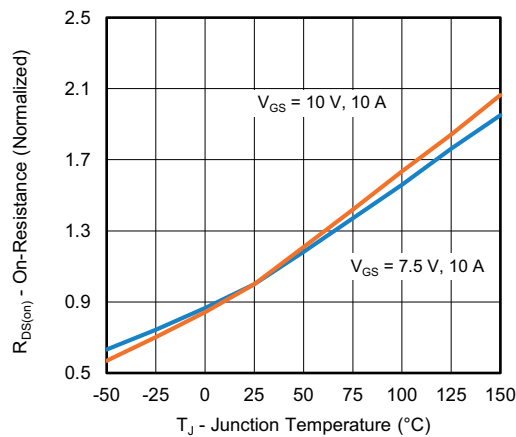
On-Resistance vs. Drain Current



Capacitance



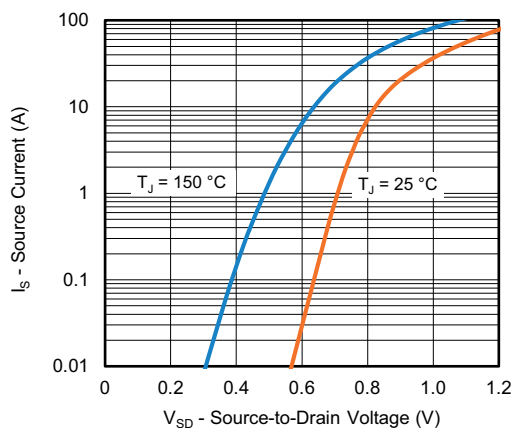
Gate Charge



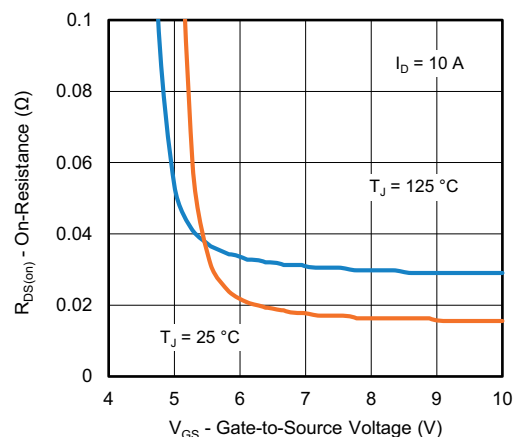
On-Resistance vs. Junction Temperature



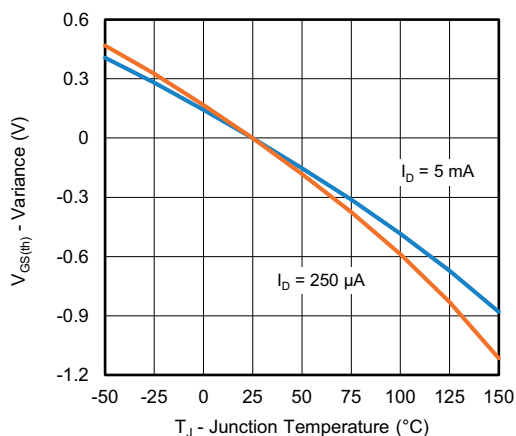
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



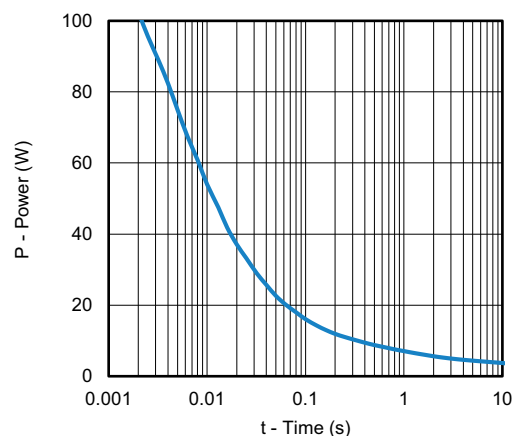
Source-Drain Diode Forward Voltage



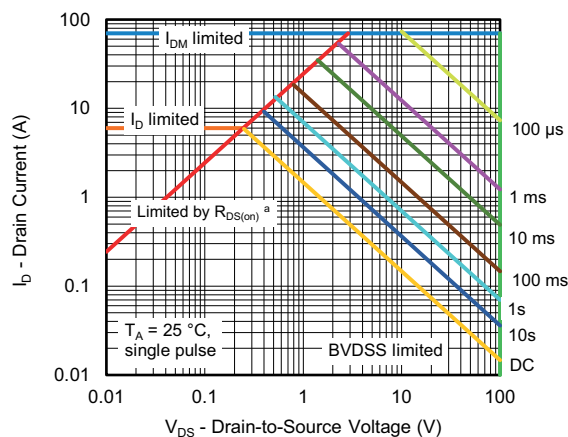
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



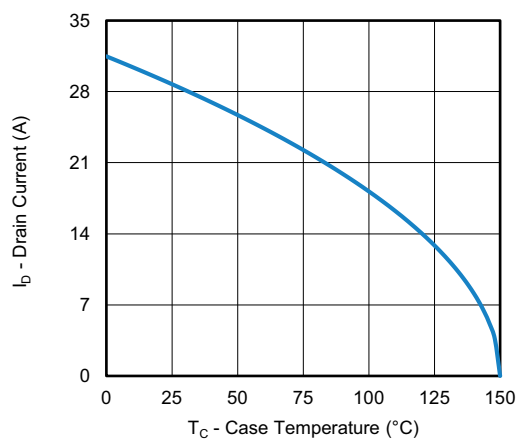
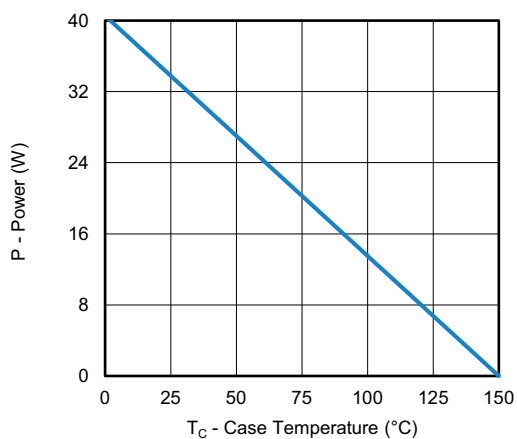
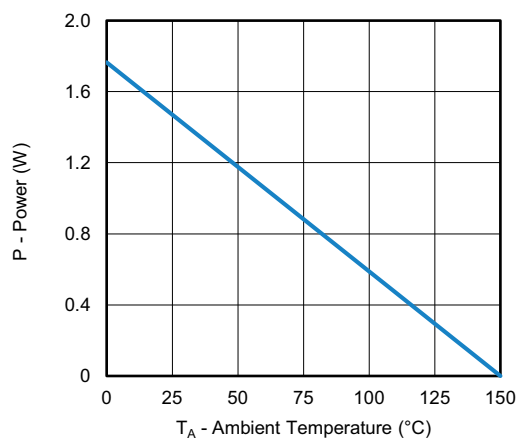
Single Pulse Power



Safe Operating Area, Junction-to-Ambient

Note

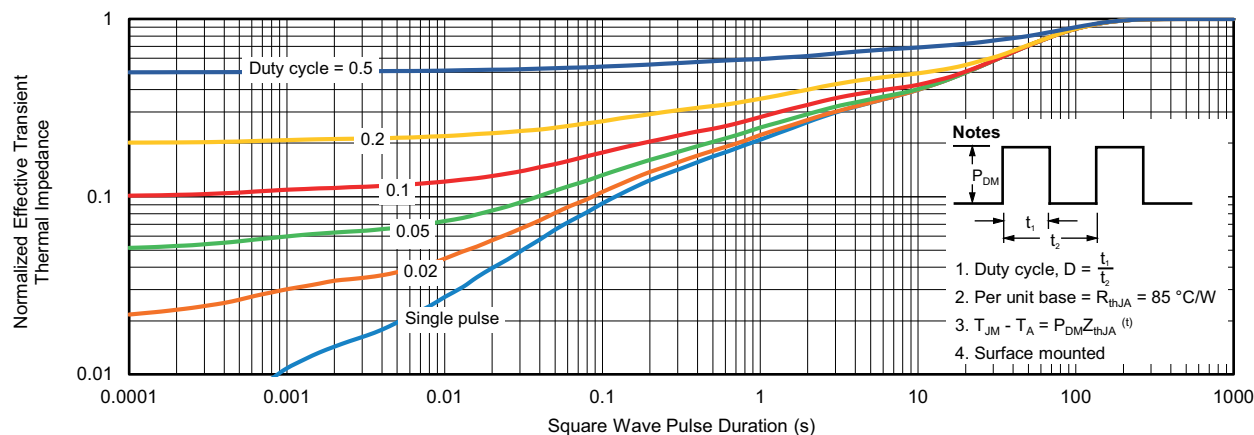
a. $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Current Derating ^a

Power, Junction-to-Case

Power, Junction-to-Ambient
Note

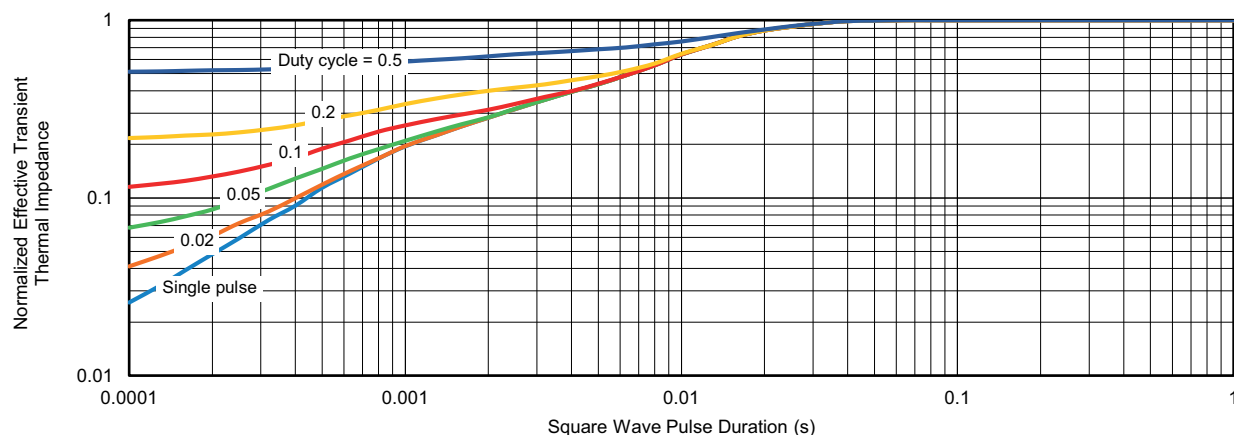
- a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



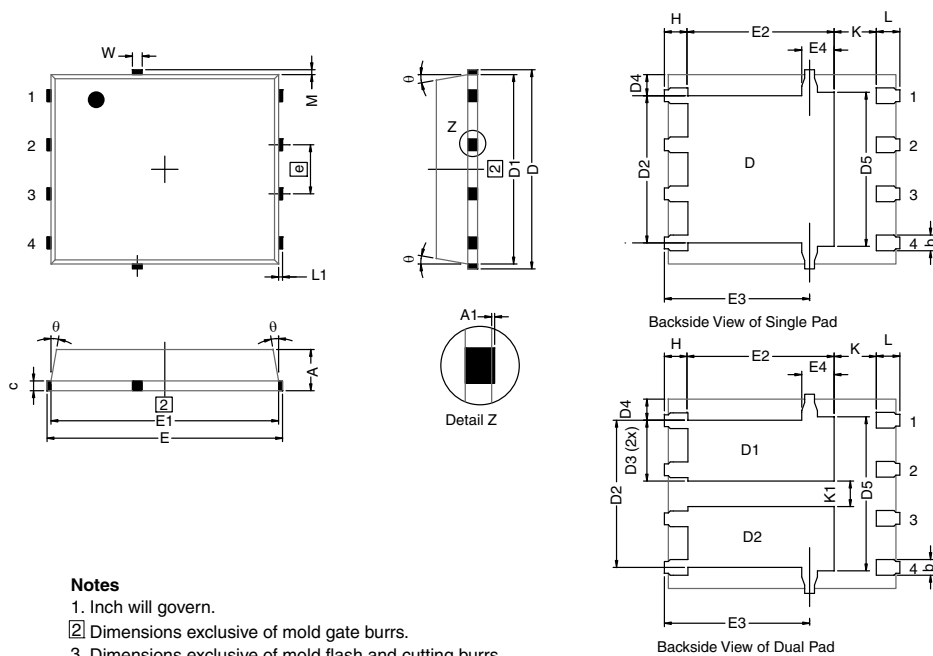
Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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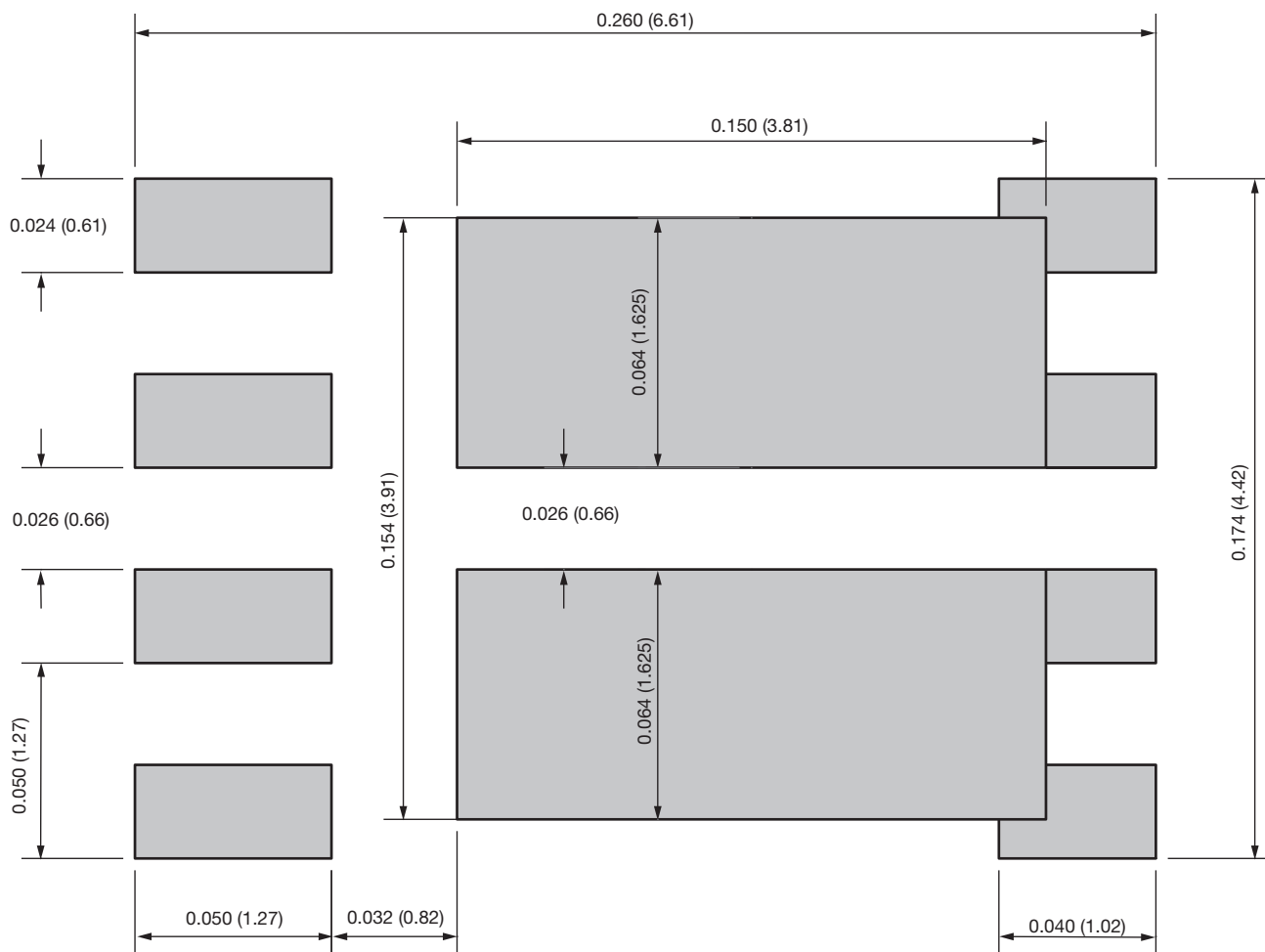
PowerPAK® SO-8, (Single/Dual)



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.97	1.04	1.12	0.038	0.041	0.044
A1		-	0.05	0	-	0.002
b	0.33	0.41	0.51	0.013	0.016	0.020
c	0.23	0.28	0.33	0.009	0.011	0.013
D	5.05	5.15	5.26	0.199	0.203	0.207
D1	4.80	4.90	5.00	0.189	0.193	0.197
D2	3.56	3.76	3.91	0.140	0.148	0.154
D3	1.32	1.50	1.68	0.052	0.059	0.066
D4	0.57 typ.			0.0225 typ.		
D5	3.98 typ.			0.157 typ.		
E	6.05	6.15	6.25	0.238	0.242	0.246
E1	5.79	5.89	5.99	0.228	0.232	0.236
E2	3.48	3.66	3.84	0.137	0.144	0.151
E3	3.68	3.78	3.91	0.145	0.149	0.154
E4	0.75 typ.			0.030 typ.		
e	1.27 BSC			0.050 BSC		
K	1.27 typ.			0.050 typ.		
K1	0.56	-	-	0.022	-	-
H	0.51	0.61	0.71	0.020	0.024	



Recommended Land Pattern PowerPAK® SO-8 Dual



Note

- Dimensions in inches (millimeters)

ECN: S24-0458-Rev. A, 06-May-2024
DWG: 3026



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