# MOSFET – Power, P-Channel, High Side Load Switch with Level-Shift, SC-88

## 8 V, ±1.3 A

# NTJD1155L

The NTJD1155L integrates a P and N-Channel MOSFET in a single package. This device is particularly suited for portable electronic equipment where low control signals, low battery voltages and high load currents are needed. The P-Channel device is specifically designed as a load switch using **onsemi** state-of-the-art trench technology. The N-Channel, with an external resistor (R1), functions as a level-shift to drive the P-Channel. The N-Channel MOSFET has internal ESD protection and can be driven by logic signals as low as 1.5 V. The NTJD1155L operates on supply lines from 1.8 to 8.0 V and can drive loads up to 1.3 A with 8.0 V applied to both $V_{IN}$ and $V_{ON/OFF}$.

### Features

- Extremely Low $R_{DS(on)}$ P-Channel Load Switch MOSFET
- Level Shift MOSFET is ESD Protected
- Low Profile, Small Footprint Package
- $V_{IN}$ Range 1.8 to 8.0 V
- ON/OFF Range 1.5 to 8.0 V
- These Devices are Pb-Free and are RoHS Compliant

### MAXIMUM RATINGS ($T_J$ = 25 °C unless otherwise noted)

| Rating | | | Symbol | Value | Unit |
|---|---|---|---|---|---|
| Input Voltage ($V_{DSS}$, P-Ch) | | | $V_{IN}$ | 8.0 | V |
| ON/OFF Voltage ($V_{GS}$, N-Ch) | | | $V_{ON/OFF}$ | 8.0 | V |
| Continuous Load Current (Note 1) | Steady State | $T_A$ = 25 °C | $I_L$ | ±1.3 | A |
| | | $T_A$ = 85 °C | | ±0.9 | |
| Power Dissipation (Note 1) | Steady State | $T_A$ = 25 °C | $P_D$ | 0.40 | W |
| | | $T_A$ = 85 °C | | 0.20 | |
| Pulsed Load Current | $t_p$ = 10 μs | | $I_{LM}$ | ±3.9 | A |
| Operating Junction and Storage Temperature | | | $T_J$, $T_{STG}$ | −55 to 150 | °C |
| Source Current (Body Diode) | | | $I_S$ | −0.4 | A |
| Lead Temperature for Soldering Purposes (1/8″ from case for 10 s) | | | $T_L$ | 260 | °C |

### THERMAL CHARACTERISTICS

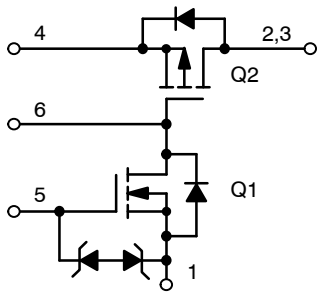
| Characteristic | Symbol | Max | Unit |
|---|---|---|---|
| Junction-to-Ambient – Steady State (Note 1) | $R_{\theta JA}$ | 320 | °C/W |
| Junction-to-Foot – Steady State (Note 1) | $R_{\theta JF}$ | 220 | |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface-mounted on FR4 board using 1 inch sq pad size (Cu area = 1.127 in sq [1 oz] including traces).

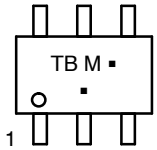
| $V_{(BR)DSS}$ | $R_{DS(on)}$ TYP | $I_D$ MAX |
|---|---|---|
| 8.0 V | 130 mΩ @ −4.5 V | ±1.3 A |
| | 170 mΩ @ −2.5 V | |
| | 260 mΩ @ −1.8 V | |

### SIMPLIFIED SCHEMATIC



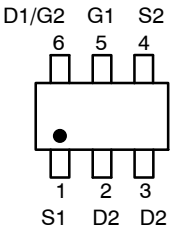

**SC-88**
**(SOT-363)**
**CASE 419B-02**
**STYLE 30**

**MARKING DIAGRAM**




TB = Device Code
M = Date Code
▪ = Pb-Free Package
(Note: Microdot may be in either location)

### PIN ASSIGNMENT




### ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| NTJD1155LT1G, NTJD1155LT2G | SC-88 (Pb-Free) | 3000/Tape & Reel |

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25 °C unless otherwise noted)

| Characteristic | Symbol | Test Condition | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | | |
| Q2 Drain-to-Source Breakdown Voltage | $V_{IN}$ | $V_{GS2}$ = 0 V, $I_{D2}$ = 250 μA | | −8.0 | | | V |
| Forward Leakage Current | $I_{FL}$ | $V_{GS1}$ = 0 V, $V_{DS2}$ = −8.0 V | $T_J$ = 25 °C | | | 1.0 | μA |
| | | | $T_J$ = 125 °C | | | 10 | |
| Q1 Gate-to-Source Leakage Current | $I_{GSS}$ | $V_{DS1}$ = 0 V, $V_{GS1}$ = ±8.0 V | | | | ±100 | nA |
| Q1 Diode Forward On-Voltage | $V_{SD}$ | $I_S$ = −0.4 A, $V_{GS1}$ = 0 V | | | −0.8 | −1.1 | V |
| **ON CHARACTERISTICS** | | | | | | | |
| ON/OFF Voltage | $V_{ON/OFF}$ | | | 1.5 | | 8.0 | V |
| Q1 Gate Threshold Voltage | $V_{GS1(th)}$ | $V_{GS1}$ = $V_{DS1}$, $I_D$ = 250 μA | | 0.4 | | 1.0 | V |
| Input Voltage | $V_{IN}$ | $V_{GS1}$ = $V_{DS1}$, $I_D$ = 250 μA | | 1.8 | | 8.0 | V |
| Q2 Drain-to-Source On Resistance | $R_{DS(on)}$ | $V_{ON/OFF}$ = 1.5 V | $V_{IN}$ = 4.5 V, $I_L$ = 1.2 A | | 130 | 175 | mΩ |
| | | | $V_{IN}$ = 2.5 V, $I_L$ = 1.0 A | | 170 | 220 | |
| | | | $V_{IN}$ = 1.8 V, $I_L$ = 0.7 A | | 260 | 320 | |
| Load Current | $I_L$ | $V_{DROP}$ ≤ 0.2 V, $V_{IN}$ = 5.0 V, $V_{ON/OFF}$ = 1.5 V | | 1.0 | | | A |
| | | $V_{DROP}$ ≤ 0.3 V, $V_{IN}$ = 2.5 V, $V_{ON/OFF}$ = 1.5 V | | 1.0 | | | |

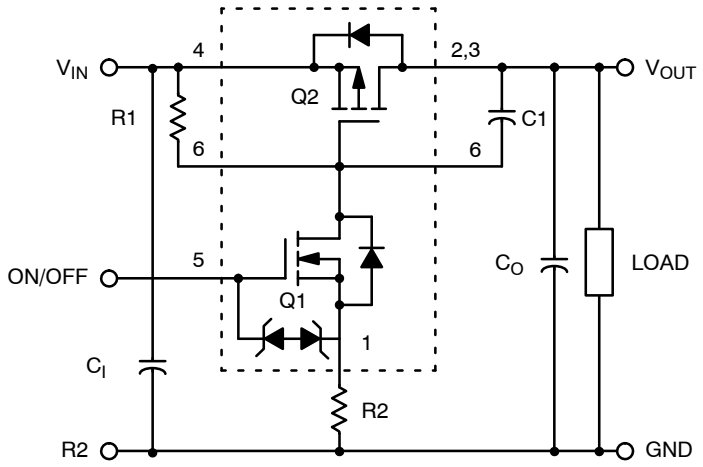



**Figure 1. Load Switch Application**

| Components | Description | Values |
|---|---|---|
| R1 | Pullup Resistor | Typical 10 kΩ to 1.0 MΩ* |
| R2 | Optional Slew-Rate Control | Typical 0 to 100 kΩ* |
| $C_O$, $C_I$ | Output Capacitance | Usually < 1.0 μF |
| C1 | Optional In-Rush Current Control | Typical ≤ 1000 pF |

* Minimum R1 value should be at least 10 x R2 to ensure Q1 turn-on.

## TYPICAL PERFORMANCE CURVES ($T_J$ = 25 °C unless otherwise noted)

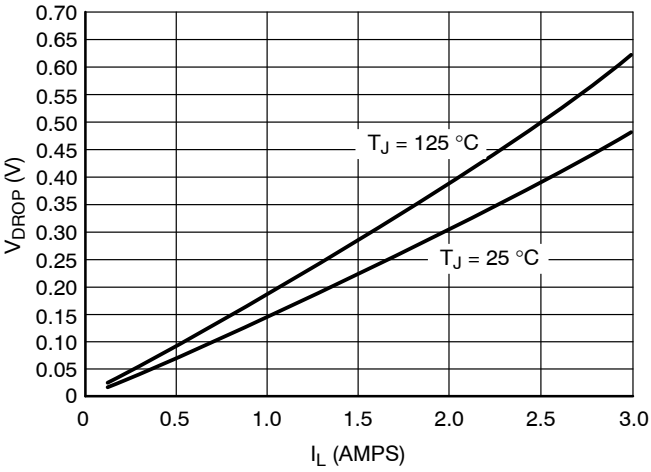



**Figure 2. $V_{drop}$ vs. $I_L$ @ $V_{in}$ = 2.5 V**

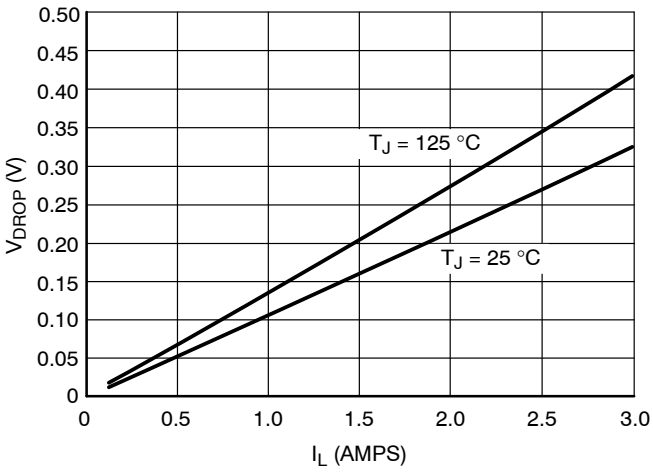



**Figure 3. $V_{drop}$ vs. $I_L$ @ $V_{in}$ = 4.5 V**

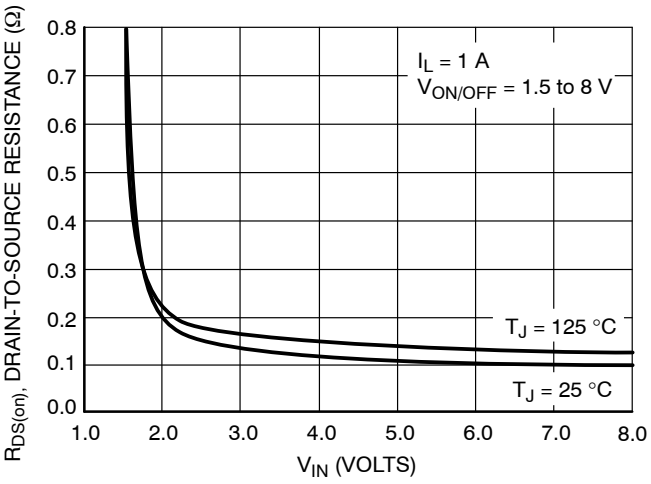



**Figure 4. On-Resistance vs. Input Voltage**

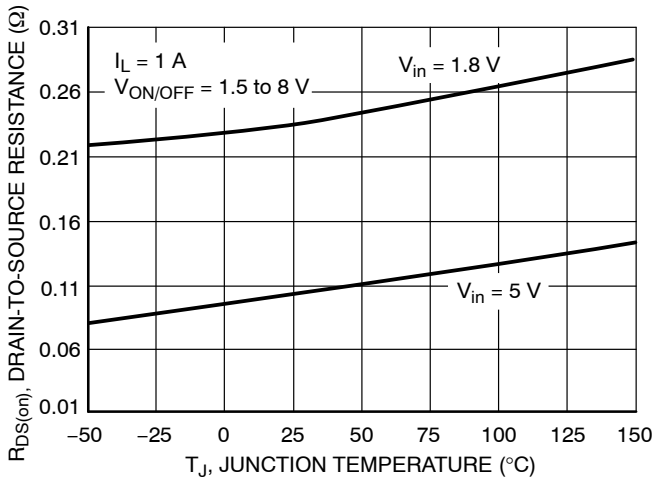



**Figure 5. On-Resistance Variation with Temperature**

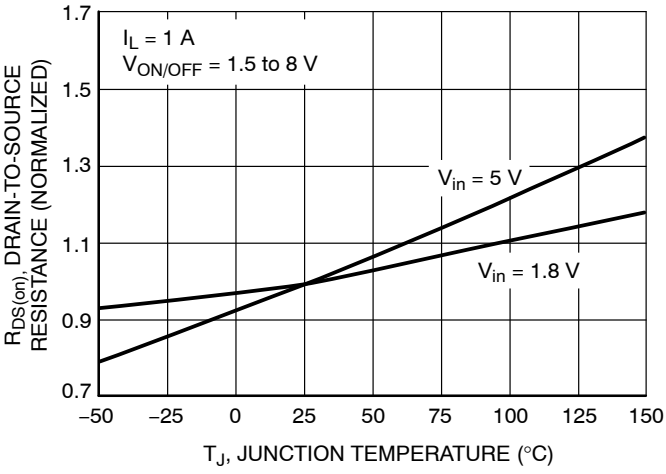



**Figure 6. Normalized On-Resistance Variation with Temperature**

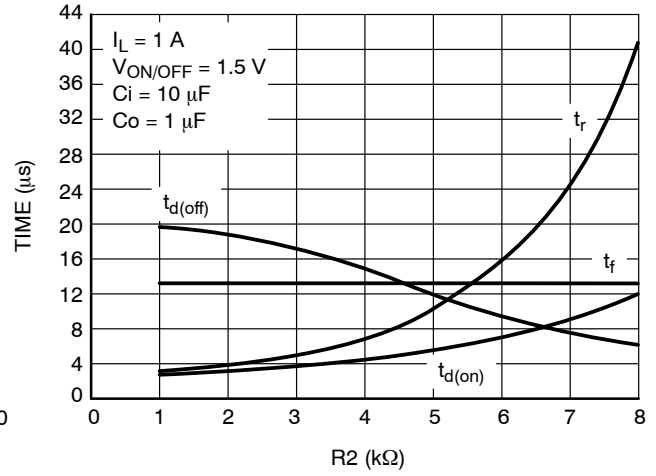



**Figure 7. Switching Variation R2 @ $V_{in}$ = 4.5 V, R1 = 20 kΩ**

## TYPICAL PERFORMANCE CURVES ($T_J$ = 25°C unless otherwise noted)

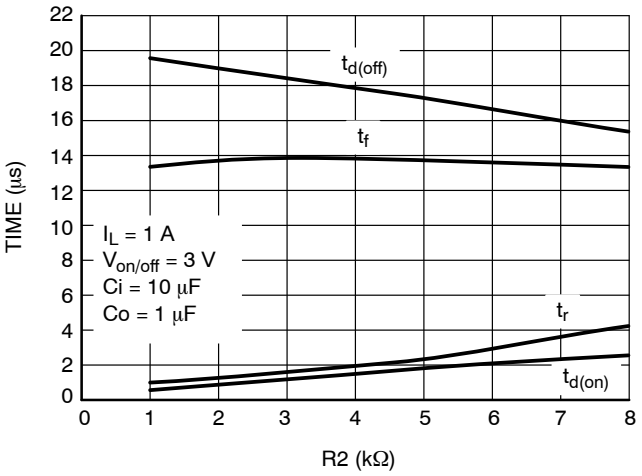



**Figure 8. Switching Variation**
**R2 @ $V_{in}$ = 4.5 V, R1 = 20 kΩ**

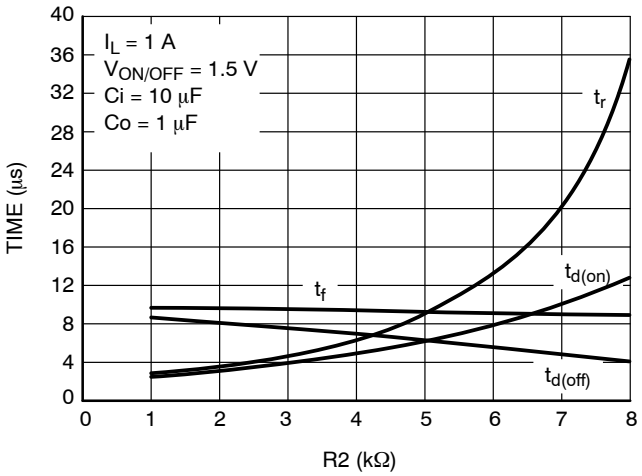



**Figure 9. Switching Variation**
**R2 @ $V_{in}$ = 2.5 V, R1 = 20 kΩ**

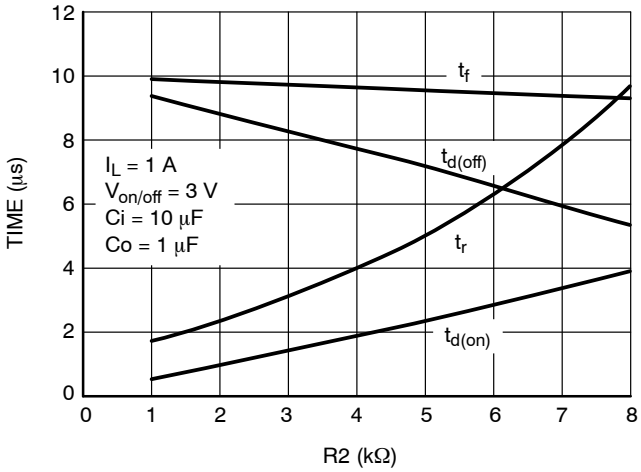



**Figure 10. Switching Variation**
**R2 @ $V_{in}$ = 2.5 V, R1 = 20 kΩ**

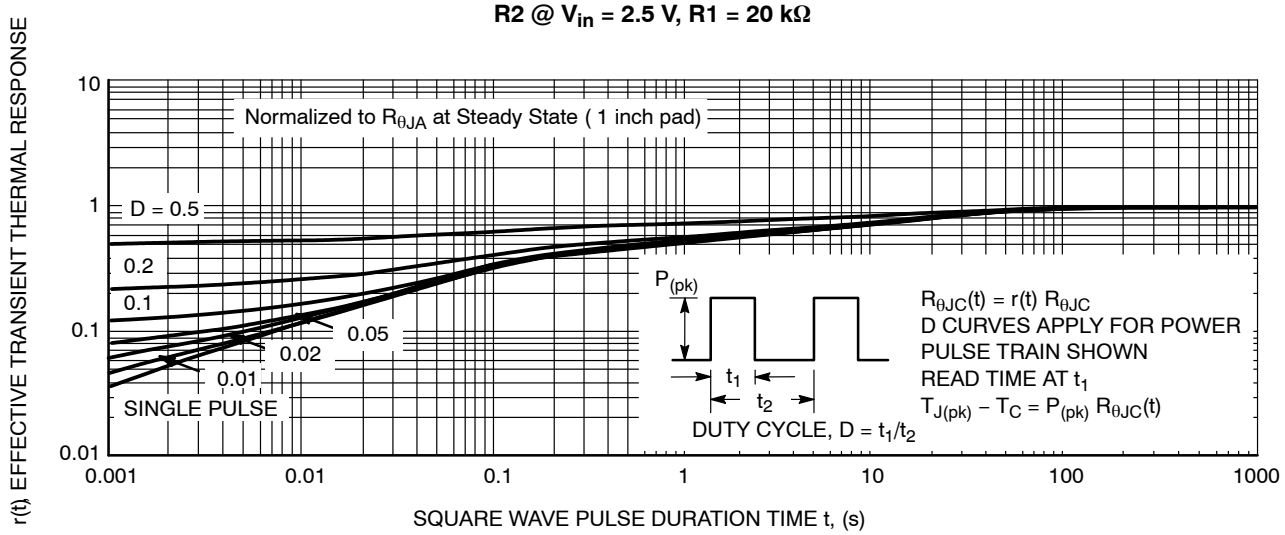



**Figure 11. FET Thermal Response**

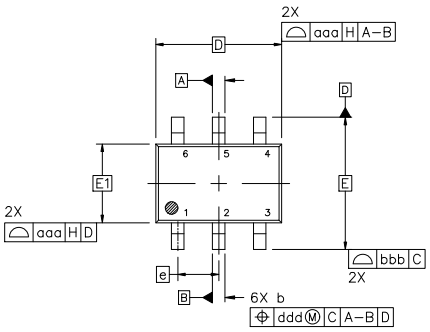
## REVISION HISTORY

| Revision | Description of Changes | Date |
|---|---|---|
| 7 | Document rebranded to **onsemi** format. | 10/16/2025 |

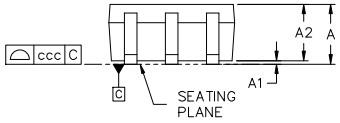
This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

**SC−88 2.00x1.25x0.90, 0.65P**
CASE 419B−02
ISSUE Z

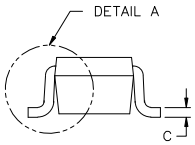
DATE 18 APR 2024



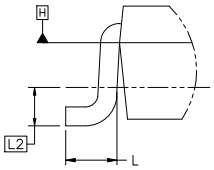

TOP VIEW




SIDE VIEW




END VIEW

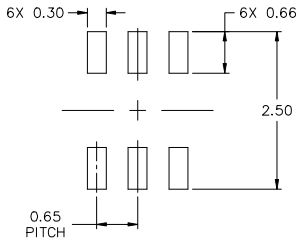



DETAIL A
SCALE 2:1

NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5−2018.
2. ALL DIMENSION ARE IN MILLIMETERS.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.20 PER END.
4. DIMENSIONS D AND E1 AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AND DATUM H.
5. DATUMS A AND B ARE DETERMINED AT DATUM H.
6. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.08 AND 0.15 FROM THE TIP.
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF DIMENSION b AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.

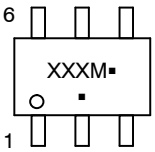
| | MILLIMETERS | | |
|---|---|---|---|
| DIM | MIN. | NOM. | MAX. |
| A | −−− | −−− | 1.10 |
| A1 | 0.00 | −−− | 0.10 |
| A2 | 0.70 | 0.90 | 1.00 |
| b | 0.15 | 0.20 | 0.25 |
| c | 0.08 | 0.15 | 0.22 |
| D | 2.00 BSC | | |
| E | 2.10 BSC | | |
| E1 | 1.25 BSC | | |
| e | 0.65 BSC | | |
| L | 0.26 | 0.36 | 0.46 |
| L2 | 0.15 BSC | | |
| aaa | 0.15 | | |
| bbb | 0.30 | | |
| ccc | 0.10 | | |
| ddd | 0.10 | | |




RECOMMENDED MOUNTING FOOTPRINT*

* FOR ADDITIONAL INFORMATION ON OUR Pb−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

## GENERIC MARKING DIAGRAM*




XXX = Specific Device Code
M = Date Code*
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

**STYLES ON PAGE 2**

| | | | |
|---|---|---|---|
| **DOCUMENT NUMBER:** | **98ASB42985B** | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red. | |
| **DESCRIPTION:** | **SC−88 2.00x1.25x0.90, 0.65P** | | **PAGE 1 OF 2** |

**SC−88 2.00x1.25x0.90, 0.65P**
CASE 419B−02
ISSUE Z

DATE 18 APR 2024

STYLE 1:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

STYLE 2:
CANCELLED

STYLE 3:
CANCELLED

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. COLLECTOR
4. EMITTER
5. BASE
6. ANODE

STYLE 5:
PIN 1. ANODE
2. ANODE
3. COLLECTOR
4. EMITTER
5. BASE
6. CATHODE

STYLE 6:
PIN 1. ANODE 2
2. N/C
3. CATHODE 1
4. ANODE 1
5. N/C
6. CATHODE 2

STYLE 7:
PIN 1. SOURCE 2
2. DRAIN 2
3. GATE 1
4. SOURCE 1
5. DRAIN 1
6. GATE 2

STYLE 8:
CANCELLED

STYLE 9:
PIN 1. EMITTER 2
2. EMITTER 1
3. COLLECTOR 1
4. BASE 1
5. BASE 2
6. COLLECTOR 2

STYLE 10:
PIN 1. SOURCE 2
2. SOURCE 1
3. GATE 1
4. DRAIN 1
5. DRAIN 2
6. GATE 2

STYLE 11:
PIN 1. CATHODE 2
2. CATHODE 2
3. ANODE 1
4. CATHODE 1
5. CATHODE 1
6. ANODE 2

STYLE 12:
PIN 1. ANODE 2
2. ANODE 2
3. CATHODE 1
4. ANODE 1
5. ANODE 1
6. CATHODE 2

STYLE 13:
PIN 1. ANODE
2. N/C
3. COLLECTOR
4. EMITTER
5. BASE
6. CATHODE

STYLE 14:
PIN 1. VREF
2. GND
3. GND
4. IOUT
5. VEN
6. VCC

STYLE 15:
PIN 1. ANODE 1
2. ANODE 2
3. ANODE 3
4. CATHODE 3
5. CATHODE 2
6. CATHODE 1

STYLE 16:
PIN 1. BASE 1
2. EMITTER 2
3. COLLECTOR 2
4. BASE 2
5. EMITTER 1
6. COLLECTOR 1

STYLE 17:
PIN 1. BASE 1
2. EMITTER 1
3. COLLECTOR 2
4. BASE 2
5. EMITTER 2
6. COLLECTOR 1

STYLE 18:
PIN 1. VIN1
2. VCC
3. VOUT2
4. VIN2
5. GND
6. VOUT1

STYLE 19:
PIN 1. I OUT
2. GND
3. GND
4. V CC
5. V EN
6. V REF

STYLE 20:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

STYLE 21:
PIN 1. ANODE 1
2. N/C
3. ANODE 2
4. CATHODE 2
5. N/C
6. CATHODE 1

STYLE 22:
PIN 1. D1 (i)
2. GND
3. D2 (i)
4. D2 (c)
5. VBUS
6. D1 (c)

STYLE 23:
PIN 1. Vn
2. CH1
3. Vp
4. N/C
5. CH2
6. N/C

STYLE 24:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE

STYLE 25:
PIN 1. BASE 1
2. CATHODE
3. COLLECTOR 2
4. BASE 2
5. EMITTER
6. COLLECTOR 1

STYLE 26:
PIN 1. SOURCE 1
2. GATE 1
3. DRAIN 2
4. SOURCE 2
5. GATE 2
6. DRAIN 1

STYLE 27:
PIN 1. BASE 2
2. BASE 1
3. COLLECTOR 1
4. EMITTER 1
5. EMITTER 2
6. COLLECTOR 2

STYLE 28:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 29:
PIN 1. ANODE
2. ANODE
3. COLLECTOR
4. EMITTER
5. BASE/ANODE
6. CATHODE

STYLE 30:
PIN 1. SOURCE 1
2. DRAIN 2
3. DRAIN 2
4. SOURCE 2
5. GATE 1
6. DRAIN 1

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

| | | | |
|---|---|---|---|
| **DOCUMENT NUMBER:** | **98ASB42985B** | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. | |
| **DESCRIPTION:** | **SC−88 2.00x1.25x0.90, 0.65P** | | **PAGE 2 OF 2** |

## ADDITIONAL INFORMATION

**TECHNICAL PUBLICATIONS**:
**Technical Library:** www.onsemi.com/design/resources/technical−documentation
**onsemi Website:** www.onsemi.com

**ONLINE SUPPORT**: www.onsemi.com/support
**For additional information, please contact your local Sales Representative at** www.onsemi.com/support/sales