

# NTD110N02R, STD110N02R

## MOSFET – Power, N-Channel, DPAK

24 V, 110 A

### Features

- Planar HD3e Process for Fast Switching Performance
- Low  $R_{DS(on)}$  to Minimize Conduction Loss
- Low  $C_{iss}$  to Minimize Driver Loss
- Low Gate Charge
- Optimized for High Side Switching Requirements in High-Efficiency DC-DC Converters
- S Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	$V_{DSS}$	24	V
Gate-to-Source Voltage – Continuous	$V_{GS}$	$\pm 20$	V
Thermal Resistance – Junction-to-Case	$R_{\theta JC}$	1.35	$^\circ\text{C}/\text{W}$
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	$P_D$	110	W
Drain Current	$I_D$	110	A
– Continuous @ $T_C = 25^\circ\text{C}$ , Chip	$I_D$	110	A
– Continuous @ $T_C = 25^\circ\text{C}$	$I_D$	110	A
Limited by Package	$I_D$	32	A
– Continuous @ $T_A = 25^\circ\text{C}$	$I_D$	32	A
Limited by Wires	$I_D$	110	A
– Single Pulse ( $t_p = 10 \mu\text{s}$ )	$I_D$	110	A
Thermal Resistance	$R_{\theta JA}$	52	$^\circ\text{C}/\text{W}$
– Junction-to-Ambient (Note 1)	$R_{\theta JA}$	52	$^\circ\text{C}/\text{W}$
– Total Power Dissipation @ $T_A = 25^\circ\text{C}$	$P_D$	2.88	W
– Drain Current – Continuous @ $T_A = 25^\circ\text{C}$	$I_D$	17.5	A
Thermal Resistance	$R_{\theta JA}$	100	$^\circ\text{C}/\text{W}$
– Junction-to-Ambient (Note 2)	$R_{\theta JA}$	100	$^\circ\text{C}/\text{W}$
– Total Power Dissipation @ $T_A = 25^\circ\text{C}$	$P_D$	1.5	W
– Drain Current – Continuous @ $T_A = 25^\circ\text{C}$	$I_D$	12.5	A
Operating and Storage Temperature Range	$T_J, T_{stg}$	-55 to 175	$^\circ\text{C}$
Single Pulse Drain-to-Source Avalanche Energy – Starting $T_J = 25^\circ\text{C}$ ( $V_{DD} = 50 \text{ Vdc}$ , $V_{GS} = 10 \text{ Vdc}$ , $I_L = 15.5 \text{ Apk}$ , $L = 1.0 \text{ mH}$ , $R_G = 25 \Omega$ )	$E_{AS}$	120	mJ
Maximum Lead Temperature for Soldering Purposes, (1/8" from case for 10 s)	$T_L$	260	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

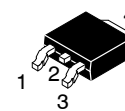
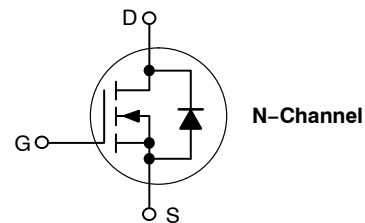
1. When surface mounted to an FR4 board using 0.5 sq in drain pad size.
2. When surface mounted to an FR4 board using the minimum recommended pad size.



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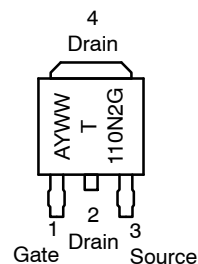
<http://onsemi.com>

$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	$I_D$ MAX
24 V	4.1 m $\Omega$ @ 10 V	110 A



**DPAK  
CASE 369AA  
(Surface Mount)  
STYLE 2**

### MARKING DIAGRAM & PIN ASSIGNMENT



A = Assembly Location\*  
Y = Year  
WW = Work Week  
T110N2 = Device Code  
G = Pb-Free Package

\* The Assembly Location code (A) is front side optional. In cases where the Assembly Location is stamped in the package, the front side assembly code may be blank.

### ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

# NTD110N02R, STD110N02R

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>					
Drain-to-Source Breakdown Voltage (Note 3) (V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA)	V <sub>(BR)DSS</sub>	24	28		V
Positive Temperature Coefficient			15		mV/°C
Zero Gate Voltage Drain Current (V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V) (V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125°C)	I <sub>DSS</sub>			1.5 10	μA
Gate-Body Leakage Current (V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0 V)	I <sub>GSS</sub>			±100	nA

## ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage (Note 3) (V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA)	V <sub>GS(th)</sub>	1.0	1.5 5.0	2.0	V mV/°C
Negative Threshold Temperature Coefficient					
Static Drain-to-Source On-Resistance (Note 3) (V <sub>GS</sub> = 10 V, I <sub>D</sub> = 110 A) (V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 55 A) (V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A) (V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 20 A)	R <sub>DS(on)</sub>		4.1 5.5 3.9 5.5	4.6 6.2	mΩ
Forward Transconductance (V <sub>DS</sub> = 10 V, I <sub>D</sub> = 15 A) (Note 3)	g <sub>FS</sub>		44		Mhos

## DYNAMIC CHARACTERISTICS

Input Capacitance	(V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V, f = 1.0 MHz)	C <sub>iss</sub>	2710	3440	pF
Output Capacitance		C <sub>oss</sub>	1105	1670	
Transfer Capacitance		C <sub>rss</sub>	450	640	

## SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	(V <sub>GS</sub> = 10 V, V <sub>DD</sub> = 10 V, I <sub>D</sub> = 40 A, R <sub>G</sub> = 3.0 Ω)	t <sub>d(on)</sub>	11	22	ns
Rise Time		t <sub>r</sub>	39	80	
Turn-Off Delay Time		t <sub>d(off)</sub>	27	40	
Fall Time		t <sub>f</sub>	21	40	
Gate Charge	(V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 40 A, V <sub>DS</sub> = 10 V) (Note 3)	Q <sub>T</sub>	23.6	28	nC
		Q <sub>GS</sub>	5.1		
		Q <sub>GD</sub>	11		

## SOURCE-DRAIN DIODE CHARACTERISTICS

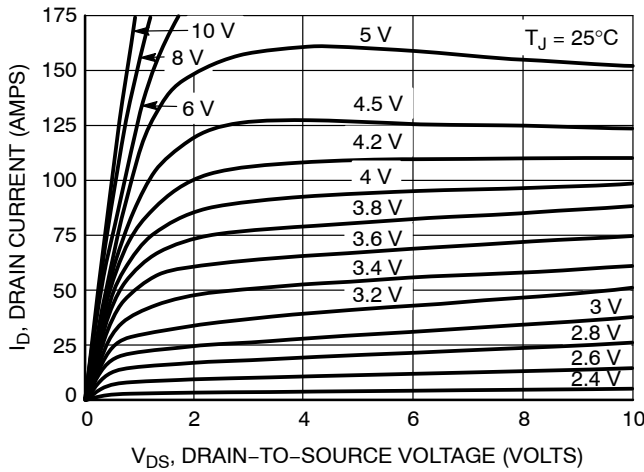
Forward On-Voltage	(I <sub>S</sub> = 20 A, V <sub>GS</sub> = 0 V) (Note 3) (I <sub>S</sub> = 55 A, V <sub>GS</sub> = 0 V) (I <sub>S</sub> = 20 A, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125°C)	V <sub>SD</sub>	0.82 0.99 0.65	1.2	V
Reverse Recovery Time	(I <sub>S</sub> = 30 A, V <sub>GS</sub> = 0 V, di <sub>S</sub> /dt = 100 A/μs) (Note 3)	t <sub>rr</sub>	36.5		ns
		t <sub>a</sub>	30		
		t <sub>b</sub>	25		
Reverse Recovery Stored Charge		Q <sub>rr</sub>	0.048		μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

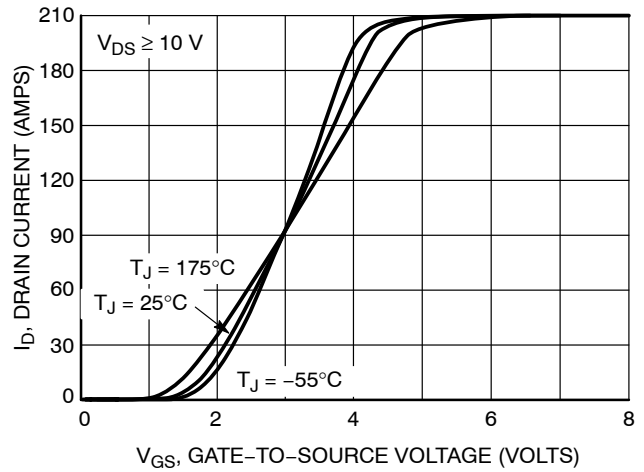
3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

4. Switching characteristics are independent of operating junction temperatures.

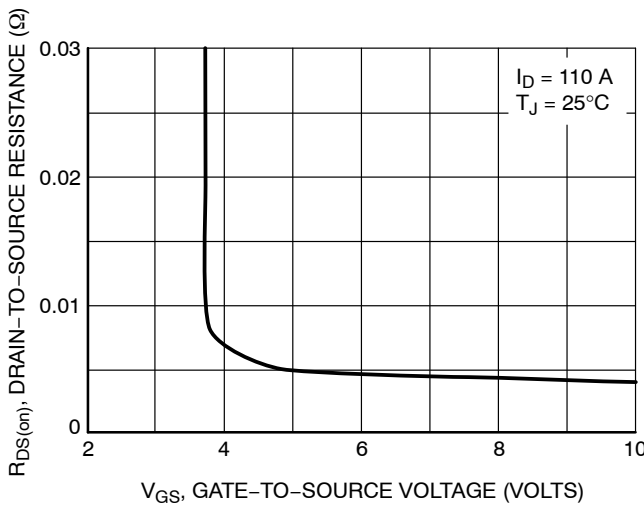
# NTD110N02R, STD110N02R



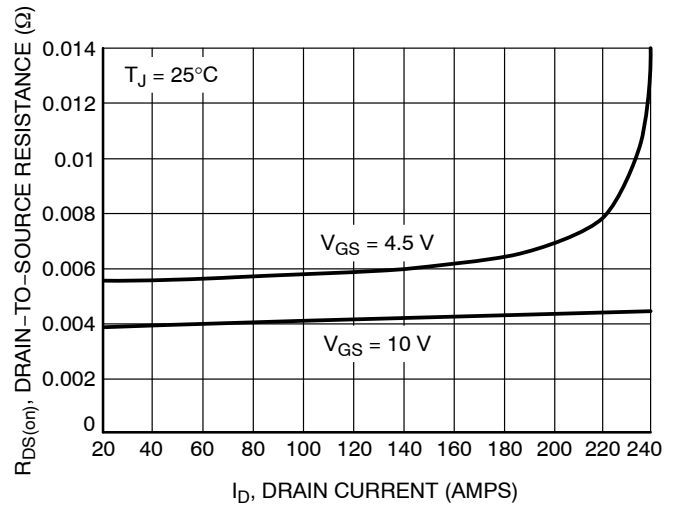
**Figure 1. On-Region Characteristics**



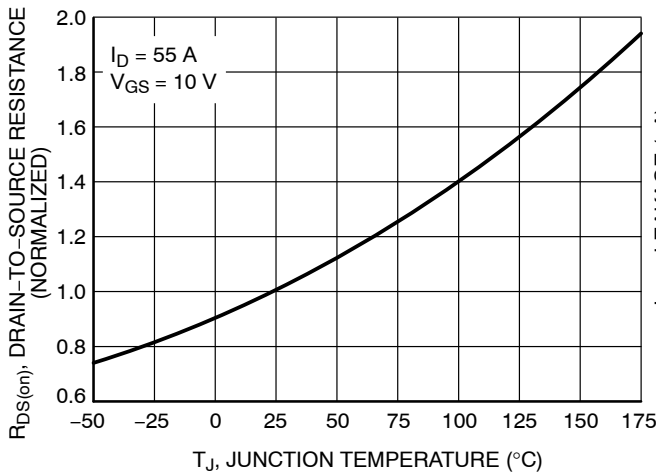
**Figure 2. Transfer Characteristics**



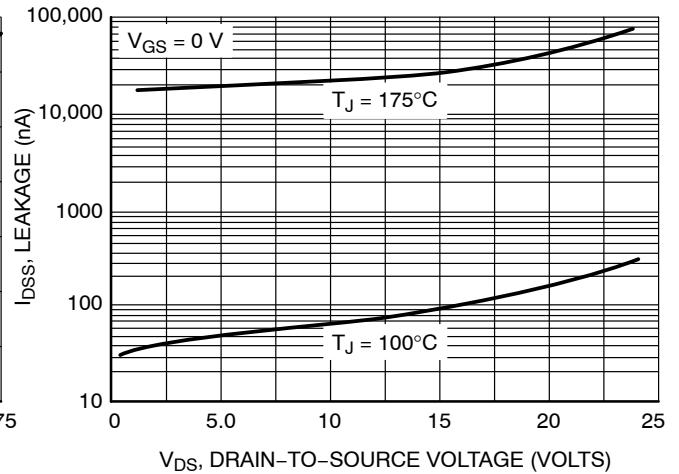
**Figure 3. On-Resistance versus Gate-to-Source Voltage**



**Figure 4. On-Resistance versus Drain Current and Gate Voltage**

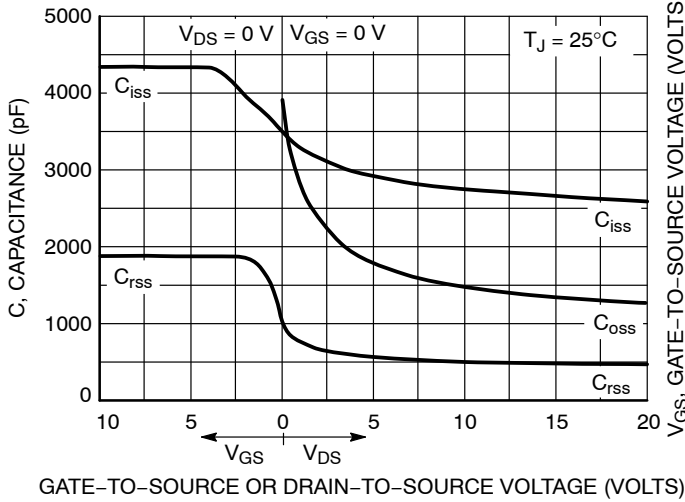


**Figure 5. On-Resistance Variation with Temperature**

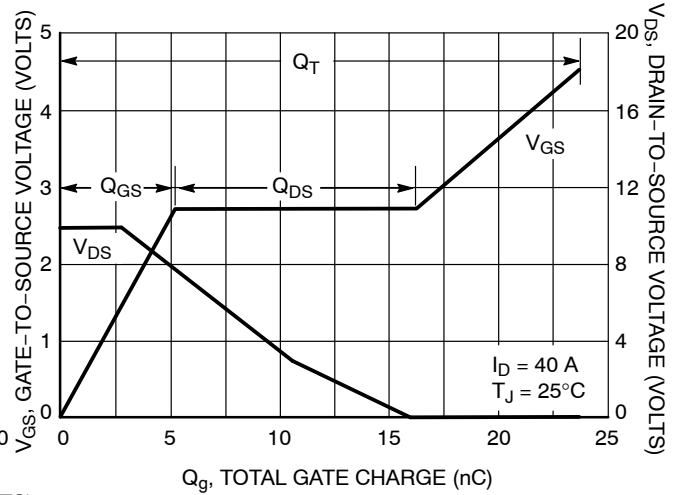


**Figure 6. Drain-to-Source Leakage Current versus Voltage**

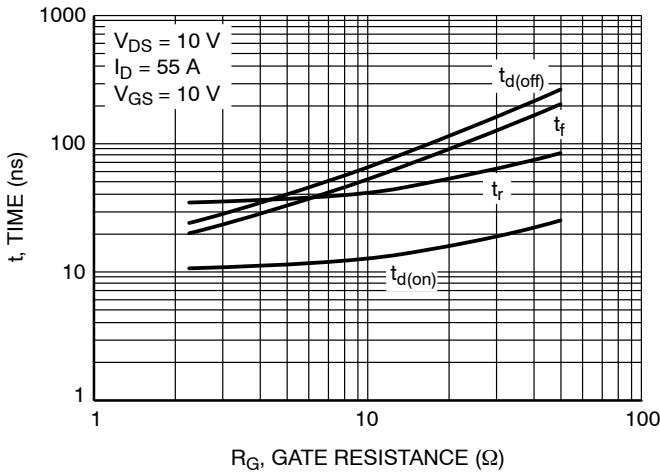
# NTD110N02R, STD110N02R



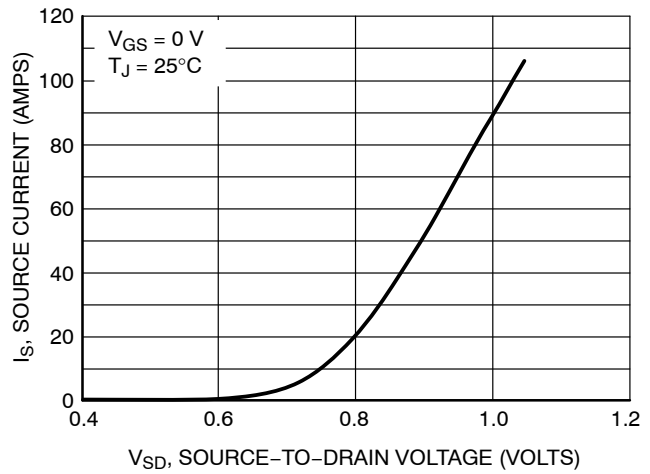
**Figure 7. Capacitance Variation**



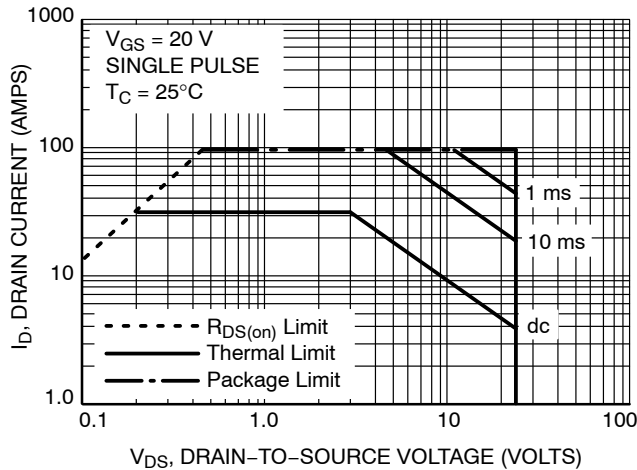
**Figure 8. Gate-to-Source and Drain-to-Source Voltage versus Total Charge**



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

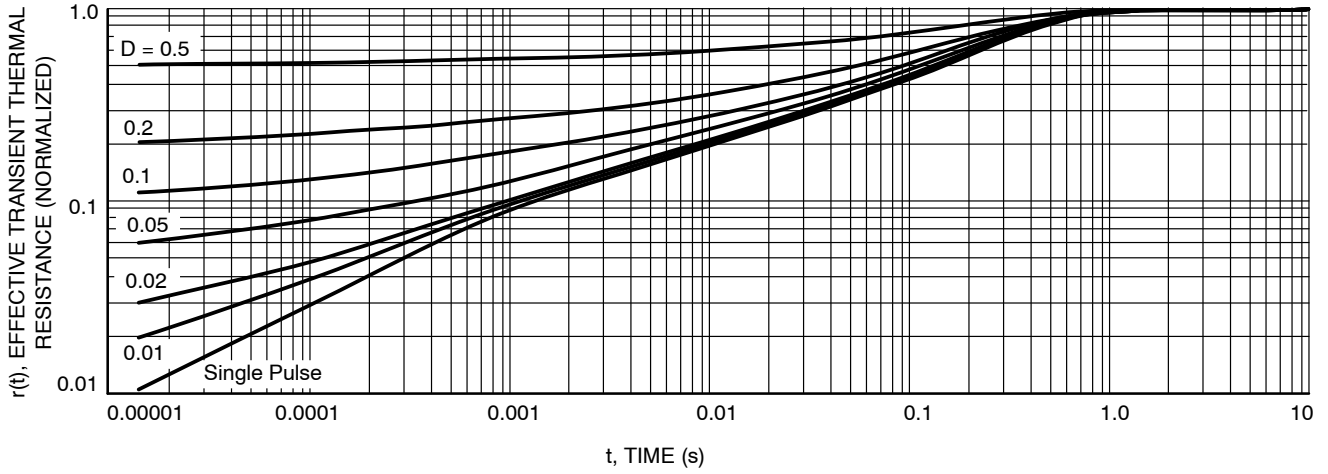


**Figure 10. Diode Forward Voltage versus Current**



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

# NTD110N02R, STD110N02R



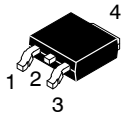
**Figure 12. Thermal Response**

## ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
NTD110N02RT4G	DPAK (Pb-Free)	2500 / Tape & Reel
STD110N02RT4G*	DPAK (Pb-Free)	2500 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*S Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable.



**DPAK-3 6.10x6.54x2.28, 2.29P**  
CASE 369AA  
ISSUE C

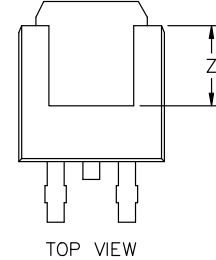
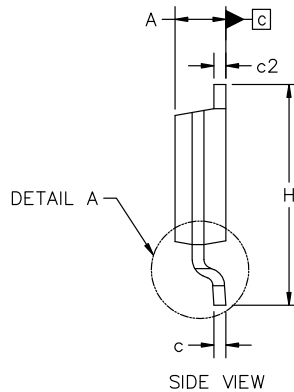
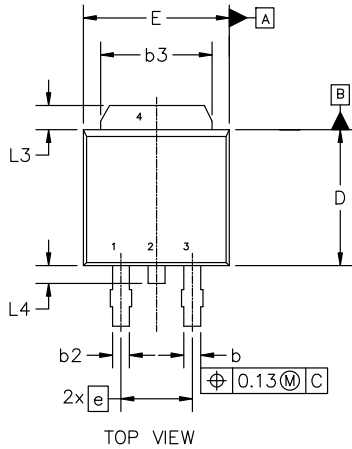
DATE 14 MAY 2026

SCALE 1:1

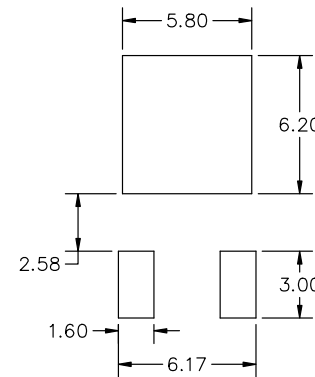
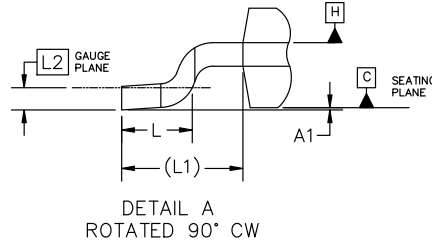
NOTES

1. DIMENSION AND TOLERANCING PER ASME Y14.5 2018
2. CONTROLLING DIMENSION: MILLIMETERS
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION b3, L3, AND Z
4. DIMENSION D AND E DO NOT INCLUDED MOLD FLASH, PROTRUSION, OR BURRS.
5. DIMENSION D AND E ARE DETERMINED AT OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H

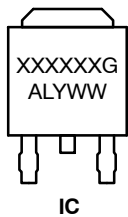
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.18	2.28	2.38
A1	0.00	---	0.13
b	0.63	0.76	0.89
b2	0.76	0.95	1.14
b3	4.57	5.02	5.46
c	0.46	0.54	0.61
c2	0.46	0.54	0.61
D	5.97	6.10	6.22
E	6.35	6.54	6.73
e	2.29 BSC		
H	9.40	9.91	10.41
L	1.40	1.59	1.78
L1	2.74 REF		
L2	0.51 BSC		
L3	0.89	---	1.27
L4	---	---	1.01
Z	3.93	---	---



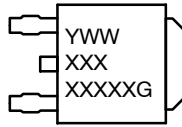
RECOMMENDED MOUNTING FOOTPRINT



**GENERIC MARKING DIAGRAM\***



IC



Discrete

- XXXXXX = Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.

<b>DOCUMENT NUMBER:</b>	<b>98AON13126D</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>DPAK-3 6.10x6.54x2.28, 2.29P</b>	<b>PAGE 1 OF 1</b>

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