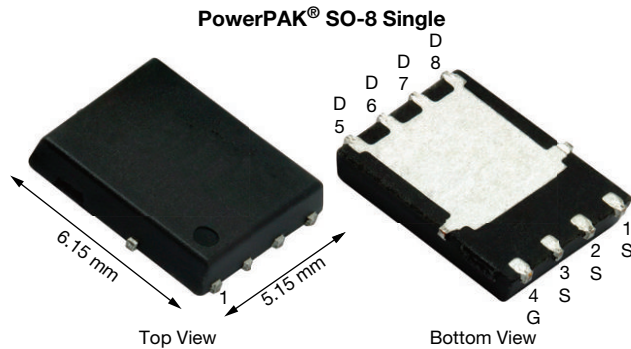


## N-Channel 40 V (D-S) 150 °C MOSFET



### FEATURES

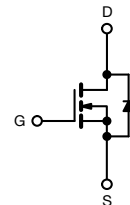
- TrenchFET® Gen IV power MOSFET
- Tuned for the lowest  $R_{DS(on)}$ - $Q_{oss}$  FOM
- 100 %  $R_g$  and UIS tested
- $Q_{gd}/Q_{gs}$  ratio < 1 optimizes switching characteristics
- Optimized for wave soldering
- Flexible leads increase resilience to board flexing
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

### APPLICATIONS

- Synchronous rectification
- High power density DC/DC
- DC/AC inverters
- Switch mode power supplies



N-Channel MOSFET

PRODUCT SUMMARY	
$V_{DS}$ (V)	40
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 10$ V	0.0042
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS} = 4.5$ V	0.0061
$Q_g$ typ. (nC)	12.4
$I_D$ (A) <sup>a</sup>	81.2
Configuration	Single

ORDERING INFORMATION	
Package	PowerPAK SO-8
Lead (Pb)-free and halogen-free	SiRA74DP-T1-GE3

ABSOLUTE MAXIMUM RATINGS ( $T_A = 25$ °C, unless otherwise noted)				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		$V_{DS}$	40	V
Gate-source voltage		$V_{GS}$	+20 / -16	
Continuous drain current ( $T_J = 150$ °C)	$T_C = 25$ °C	$I_D$	81.2	A
	$T_C = 70$ °C		64.2	
	$T_A = 25$ °C		24 <sup>b</sup>	
	$T_A = 70$ °C		19.2 <sup>b</sup>	
Pulsed drain current ( $t = 100$ $\mu$ s)		$I_{DM}$	150	A
Continuous source-drain diode current	$T_C = 25$ °C	$I_S$	42	
	$T_A = 25$ °C		3.7 <sup>b, c</sup>	
Single pulse avalanche current	L = 0.1 mH	$I_{AS}$	20	mJ
Single pulse avalanche energy		$E_{AS}$	20	
Maximum power dissipation	$T_C = 25$ °C	$P_D$	46.2	W
	$T_C = 70$ °C		29.6	
	$T_A = 25$ °C		4.1 <sup>b</sup>	
	$T_A = 70$ °C		2.6 <sup>b</sup>	
Operating junction and storage temperature range		$T_J, T_{stg}$	-55 to +150	°C
Soldering recommendations (peak temperature) <sup>c</sup>			260	

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient <sup>b</sup>	$t < 10$ s	$R_{thJA}$	25	30	°C/W
Maximum junction-to-case (drain)	Steady state	$R_{thJC}$	2.1	2.7	

#### Notes

- $T_C = 25$  °C
- Surface mounted on 1" x 1" FR4 board
- $t = 10$  s
- See solder profile ([www.vishay.com/doc?73257](http://www.vishay.com/doc?73257)). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
- Maximum under steady state conditions is 75 °C/W



SPECIFICATIONS ( $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Static</b>						
Drain-source breakdown voltage	$V_{DS}$	$V_{GS} = 0\text{ V}$ , $I_D = 250\text{ }\mu\text{A}$	40	-	-	V
$V_{DS}$ temperature coefficient	$\Delta V_{DS}/T_J$	$I_D = 1\text{ mA}$	-	24	-	mV/ $^\circ\text{C}$
$V_{GS(th)}$ temperature coefficient	$\Delta V_{GS(th)}/T_J$	$I_D = 250\text{ }\mu\text{A}$	-	-6.1	-	
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	1.0	-	2.4	V
Gate-source leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}$ , $V_{GS} = +20 / -16\text{ V}$	-	-	100	nA
Zero gate voltage drain current	$I_{DSS}$	$V_{DS} = 40\text{ V}$ , $V_{GS} = 0\text{ V}$	-	-	1	$\mu\text{A}$
		$V_{DS} = 40\text{ V}$ , $V_{GS} = 0\text{ V}$ , $T_J = 70\text{ }^\circ\text{C}$	-	-	15	
On-state drain current <sup>a</sup>	$I_{D(on)}$	$V_{DS} \geq 10\text{ V}$ , $V_{GS} = 10\text{ V}$	30	-	-	A
Drain-source on-state resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$ , $I_D = 10\text{ A}$	-	0.0035	0.0042	$\Omega$
		$V_{GS} = 4.5\text{ V}$ , $I_D = 10\text{ A}$	-	0.0050	0.0061	
Forward transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 15\text{ V}$ , $I_D = 10\text{ A}$	-	50	-	S
<b>Dynamic <sup>b</sup></b>						
Input capacitance	$C_{ISS}$	$V_{DS} = 20\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 1\text{ MHz}$	-	2000	-	$\mu\text{F}$
Output capacitance	$C_{OSS}$		-	390	-	
Reverse transfer capacitance	$C_{RSS}$		-	18	-	
Total gate charge	$Q_g$	$V_{DS} = 20\text{ V}$ , $V_{GS} = 10\text{ V}$ , $I_D = 10\text{ A}$	-	27	41	nC
		$V_{DS} = 20\text{ V}$ , $V_{GS} = 4.5\text{ V}$ , $I_D = 10\text{ A}$	-	12.4	19	
Gate-source charge	$Q_{gs}$		-	6.3	-	
Gate-drain charge	$Q_{gd}$		-	2.1	-	
Output charge	$Q_{OSS}$	$V_{DS} = 20\text{ V}$ , $V_{GS} = 0\text{ V}$	-	16	-	
Gate resistance	$R_g$	$f = 1\text{ MHz}$	0.8	1.45	2.5	$\Omega$
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 20\text{ V}$ , $R_L = 2\text{ }\Omega$ , $I_D \cong 10\text{ A}$ , $V_{GEN} = 10\text{ V}$ , $R_g = 1\text{ }\Omega$	-	12	24	ns
Rise time	$t_r$		-	5	10	
Turn-off delay time	$t_{d(off)}$		-	25	50	
Fall time	$t_f$		-	5	10	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 20\text{ V}$ , $R_L = 2\text{ }\Omega$ , $I_D \cong 10\text{ A}$ , $V_{GEN} = 4.5\text{ V}$ , $R_g = 1\text{ }\Omega$	-	25	50	
Rise time	$t_r$		-	55	110	
Turn-off delay time	$t_{d(off)}$		-	22	44	
Fall time	$t_f$		-	8	16	
<b>Drain-Source Body Diode Characteristics</b>						
Continuous source-drain diode current	$I_S$	$T_C = 25\text{ }^\circ\text{C}$	-	-	46.2	A
Pulse diode forward current	$I_{SM}$		-	-	150	
Body diode voltage	$V_{SD}$	$I_S = 5\text{ A}$ , $V_{GS} = 0\text{ V}$	-	0.74	1.1	V
Body diode reverse recovery time	$t_{rr}$	$I_F = 10\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $T_J = 25\text{ }^\circ\text{C}$	-	24	48	ns
Body diode reverse recovery charge	$Q_{rr}$		-	13	26	nC
Reverse recovery fall time	$t_a$		-	12	-	ns
Reverse recovery rise time	$t_b$		-	12	-	

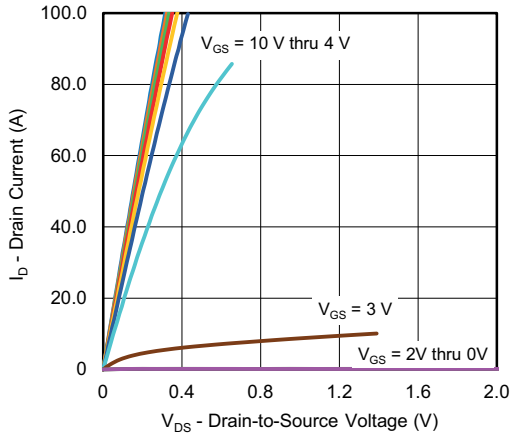
**Notes**

- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$   
b. Guaranteed by design, not subject to production testing

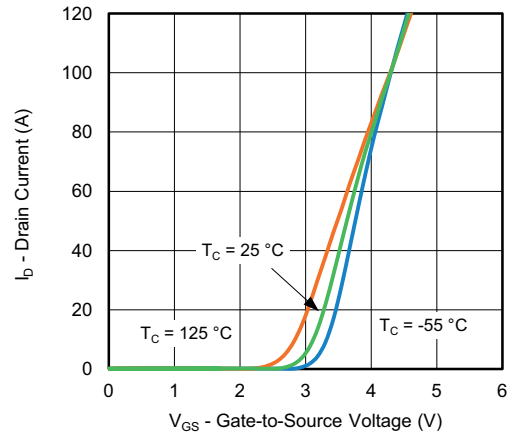
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



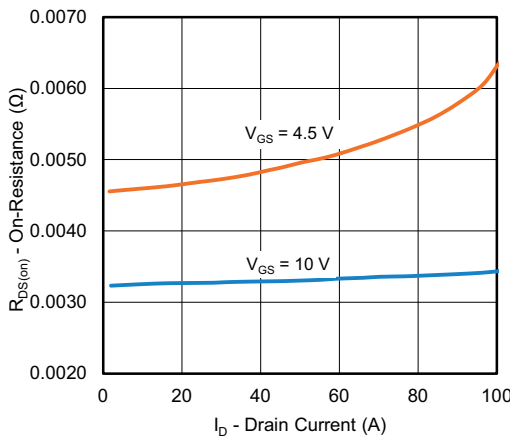
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



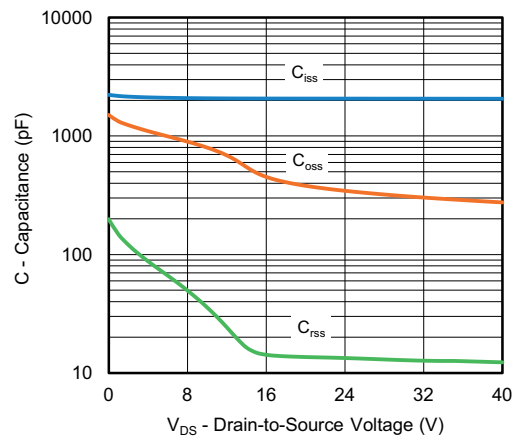
**Output Characteristics**



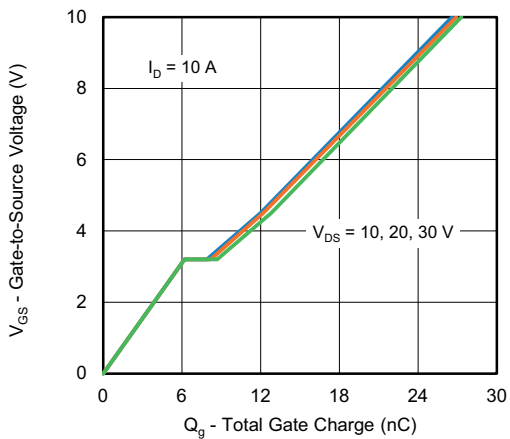
**Transfer Characteristics**



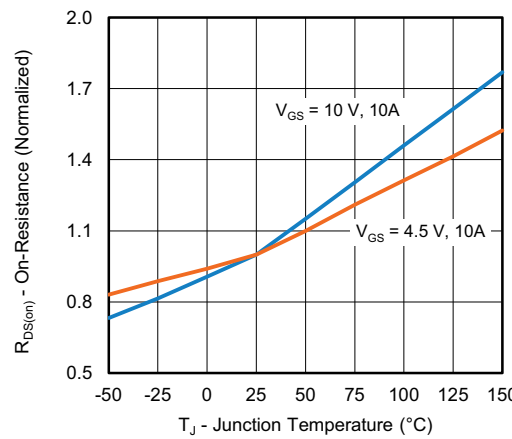
**On-Resistance vs. Drain Current and Gate Voltage**



**Capacitance**



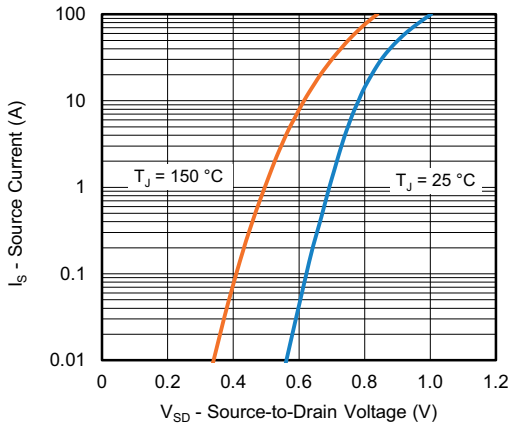
**Gate Charge**



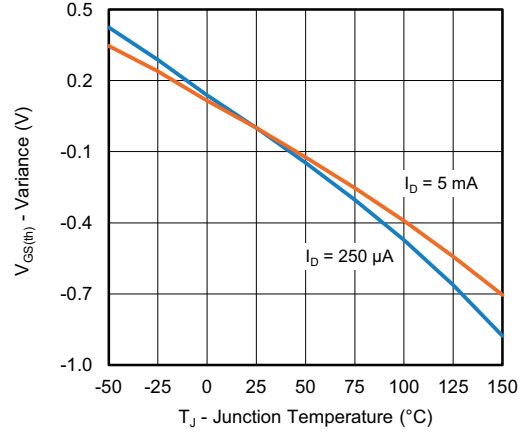
**On-Resistance vs. Junction Temperature**



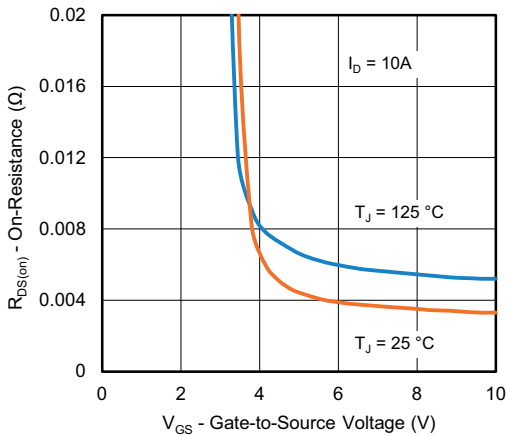
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



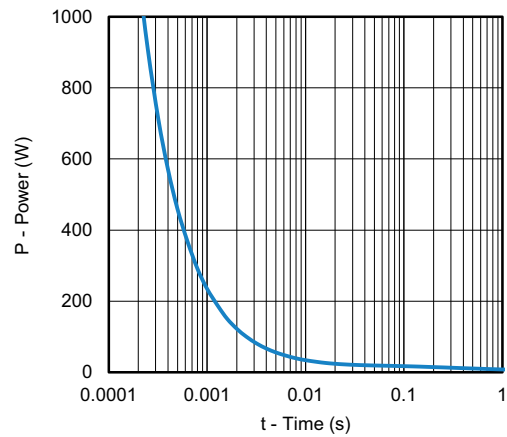
**Source-Drain Diode Forward Voltage**



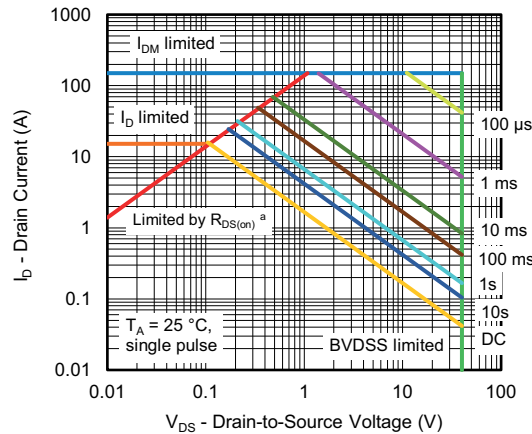
**Threshold Voltage**



**On-Resistance vs. Gate-to-Source Voltage**



**Single Pulse Power, Junction-to-Ambient**



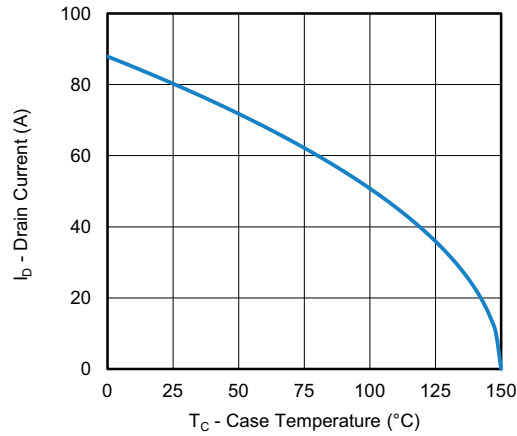
**Safe Operating Area, Junction-to-Ambient**

**Note**

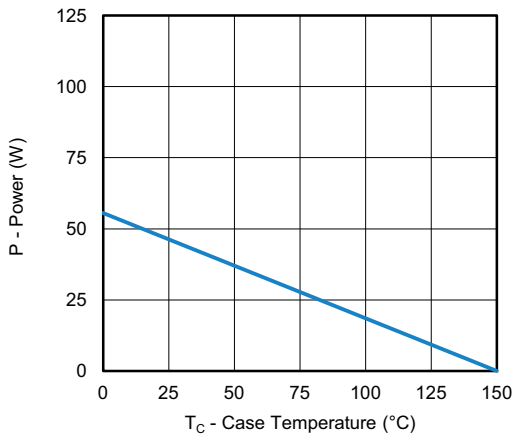
a.  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified



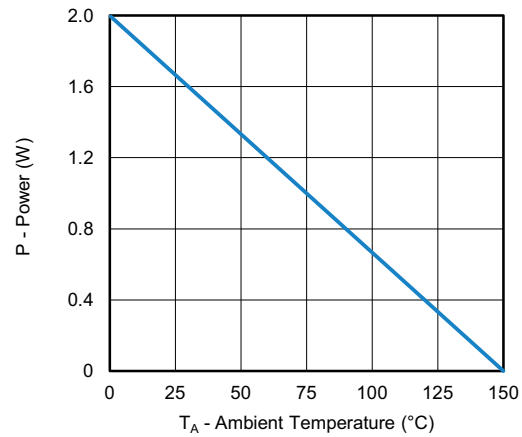
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



**Current Derating <sup>a</sup>**



**Power, Junction-to-Case**



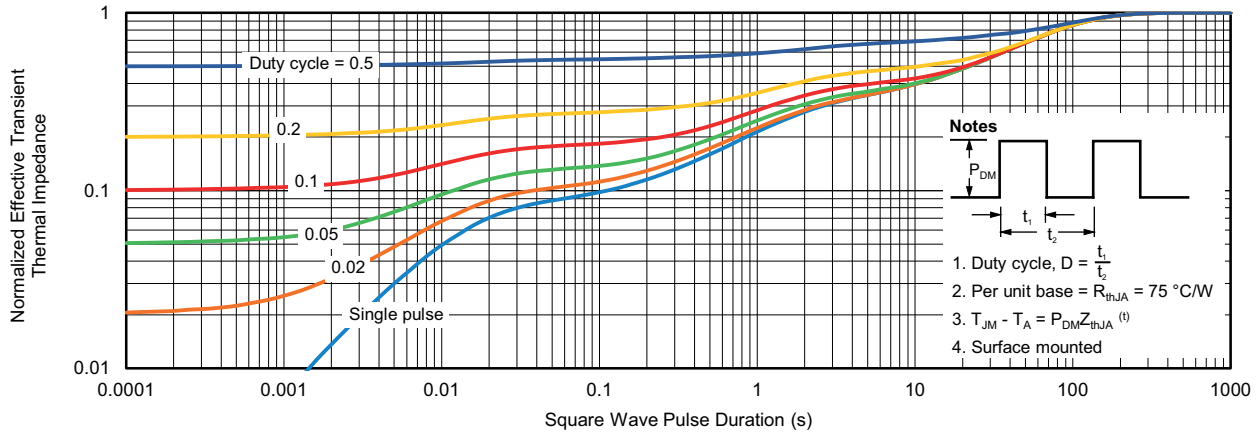
**Power, Junction-to-Ambient**

**Note**

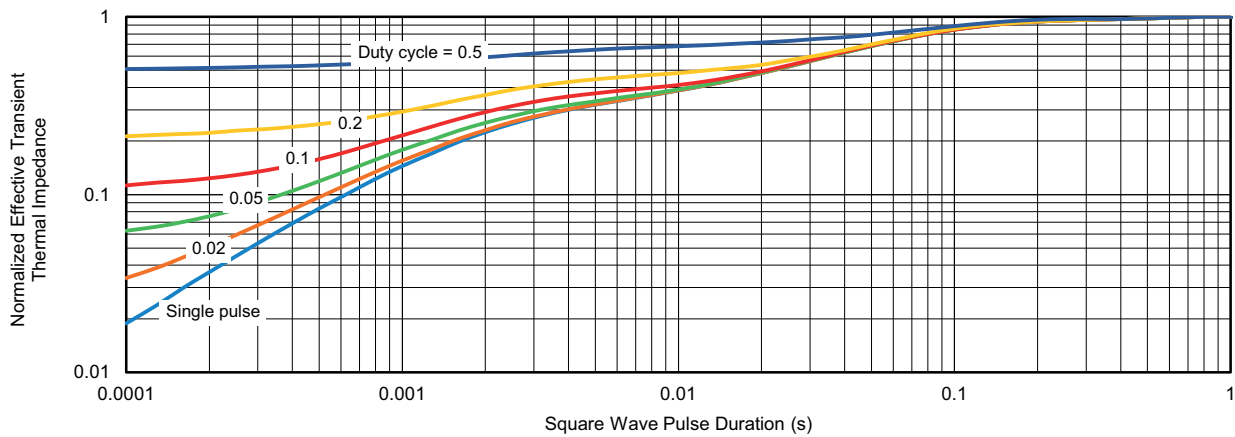
- a. The power dissipation P<sub>D</sub> is based on T<sub>J</sub> max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)



**Normalized Thermal Transient Impedance, Junction-to-Ambient**

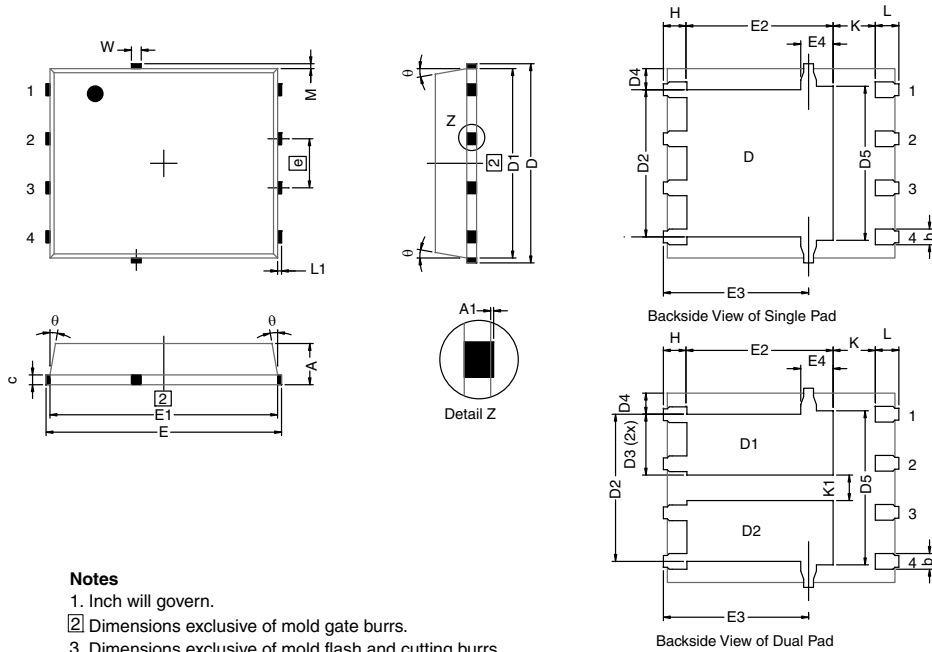


**Normalized Thermal Transient Impedance, Junction-to-Case**

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see [www.vishay.com/ppg?77640](http://www.vishay.com/ppg?77640).



# PowerPAK<sup>®</sup> SO-8, (Single/Dual)



- Notes**
1. Inch will govern.
  2. Dimensions exclusive of mold gate burrs.
  3. Dimensions exclusive of mold flash and cutting burrs.

DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.97	1.04	1.12	0.038	0.041	0.044
A1		-	0.05	0	-	0.002
b	0.33	0.41	0.51	0.013	0.016	0.020
c	0.23	0.28	0.33	0.009	0.011	0.013
D	5.05	5.15	5.26	0.199	0.203	0.207
D1	4.80	4.90	5.00	0.189	0.193	0.197
D2	3.56	3.76	3.91	0.140	0.148	0.154
D3	1.32	1.50	1.68	0.052	0.059	0.066
D4	0.57 typ.			0.0225 typ.		
D5	3.98 typ.			0.157 typ.		
E	6.05	6.15	6.25	0.238	0.242	0.246
E1	5.79	5.89	5.99	0.228	0.232	0.236
E2	3.48	3.66	3.84	0.137	0.144	0.151
E3	3.68	3.78	3.91	0.145	0.149	0.154
E4	0.75 typ.			0.030 typ.		
e	1.27 BSC			0.050 BSC		
K	1.27 typ.			0.050 typ.		
K1	0.56	-	-	0.022	-	-
H	0.51	0.61	0.71	0.020	0.024	0.028
L	0.51	0.61	0.71	0.020	0.024	0.028
L1	0.06	0.13	0.20	0.002	0.005	0.008
θ	0°	-	12°	0°	-	12°
W	0.15	0.25	0.36	0.006	0.010	0.014
M	0.125 typ.			0.005 typ.		

ECN: S17-0173-Rev. L, 13-Feb-17  
DWG: 5881

## RECOMMENDED MINIMUM PADS FOR PowerPAK® SO-8 Single



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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