HS8MA2

30V Pch+Nch Power MOSFET

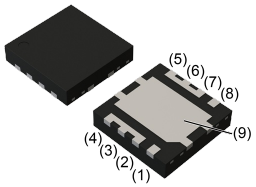
Datasheet

Symbol	Tr1:Pch	Tr2:Nch
V_{DSS}	-30V	30V
$R_{DS(on)}$(Max.)	80mΩ	35mΩ
I_D	±5.5A	±7.0A
P_D	4.0W	

●Outline

DFN3333-9DC

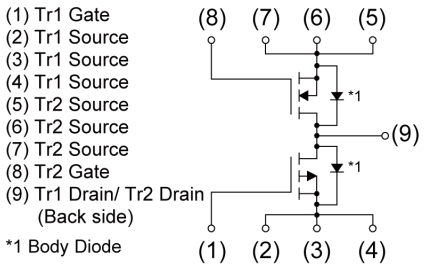
HSML3333L9



●Features

1) Low on - resistance
2) Small Surface Mount Package
3) Pb-free plating ; RoHS compliant
4) Halogen Free

●Inner circuit



●Application

Switching

Motor Drive

●Packaging specifications

Type	Packing	Embossed Tape
	Reel size (mm)	180
	Tape width (mm)	12
	Quantity (pcs)	1000
	Taping code	TCR1
	Marking	HS8MA2

●Absolute maximum ratings (T_a = 25°C ,unless otherwise specified)

Parameter		Symbol	Value		Unit
			Tr1:Pch	Tr2:Nch	
Drain - Source voltage		V_{DSS}	-30	30	V
Continuous drain current		I_D*1	±5.5	±7.0	A
Pulsed drain current		I_{DP}*2	±30	±30	A
Gate - Source voltage		V_{GSS}	±20	±20	V
Power dissipation	total	P_D*1	4.0		W
		P_D*3	2.0		
Junction temperature		T_j	150		℃
Operating junction and storage temperature range		T_{stg}	-55 to +150		℃

●Thermal resistance

Parameter	Symbol	Values			Unit
		Min.	Typ.	Max.	
Thermal resistance, junction - ambient	R_{thJA} *3	-	-	83.3	℃/W

●Electrical characteristics (T_a = 25°C)

Parameter	Symbol	Type	Conditions	Values			Unit
				Min.	Typ.	Max.	
Drain - Source breakdown voltage	$V_{(BR)DSS}$	Tr1	V_{GS} = 0V, I_D = -1mA	-30	-	-	V
		Tr2	V_{GS} = 0V, I_D = 1mA	30	-	-	
Breakdown voltage temperature coefficient	$\frac{\Delta V_{(BR)DSS}}{\Delta T_j}$	Tr1	I_D = -1mA, referenced to 25℃	-	-22	-	mV/℃
		Tr2	I_D = 1mA, referenced to 25℃	-	21	-	
Zero gate voltage drain current	I_{DSS}	Tr1	V_{DS} = -30V, V_{GS} = 0V	-	-	-1	μA
		Tr2	V_{DS} = 30V, V_{GS} = 0V	-	-	1	
Gate - Source leakage current	I_{GSS}	Tr1	V_{GS} = ±20V, VDS = 0V	-	-	±100	nA
		Tr2	V_{GS} = ±20V, VDS = 0V	-	-	±100	
Gate threshold voltage	$V_{GS(th)}$	Tr1	V_{DS} = -10V, I_D = -1mA	-1.0	-	-2.5	V
		Tr2	V_{DS} = 10V, I_D = 1mA	1.0	-	2.5	
Gate threshold voltage temperature coefficient	$\frac{\Delta V_{GS(th)}}{\Delta T_j}$	Tr1	I_D = -1mA, referenced to 25℃	-	2.9	-	mV/℃
		Tr2	I_D = 1mA, referenced to 25℃	-	-3	-	
Static drain - source on - state resistance	$R_{DS(on)}$ *4	Tr1	V_{GS} = -10V, I_D = -5.5A	-	55	80	mΩ
			V_{GS} = -4.5V, I_D = -5.5A	-	80	115	
		Tr2	V_{GS} = 10V, I_D = 7.0A	-	25	35	
			V_{GS} = 4.5V, I_D = 7.0A	-	40	56	
Gate resistance	R_G	Tr1	f=1MHz, open drain	-	10	-	Ω
		Tr2		-	3	-	
Forward Transfer Admittance	$\|Y_{fs}\|$ *4	Tr1	V_{DS} = -5V, I_D = -3A	1.9	-	-	S
		Tr2	V_{DS} = 5V, I_D = 4.5A	1.4	-	-	

*1 Pw ≤ 1s, Limited only by maximum temperature allowed.

*2 Pw ≤ 10μs, Duty cycle ≤ 1%

*3 Mounted on a ceramic board (30×30×0.8mm)

*4 Pulsed

●Electrical characteristics (T_a = 25°C)

<Tr1>

Parameter	Symbol	Conditions	Values			Unit
			Min.	Typ.	Max.	
Input capacitance	C_{iss}	V_{GS} = 0V	-	320	-	pF
Output capacitance	C_{oss}	V_{DS} = -10V	-	68	-	
Reverse transfer capacitance	C_{rss}	f = 1MHz	-	54	-	
Turn - on delay time	$t_{d(on)}$ *4	V_{DD} ≃ -15V, V_{GS} = -10V	-	7.9	-	ns
Rise time	t_r *4	I_D = -1.5A	-	16.8	-	
Turn - off delay time	$t_{d(off)}$ *4	R_L = 10Ω	-	27.6	-	
Fall time	t_f *4	R_G = 10Ω	-	8.5	-	

<Tr2>

Parameter	Symbol	Conditions	Values			Unit
			Min.	Typ.	Max.	
Input capacitance	C_{iss}	V_{GS} = 0V	-	365	-	pF
Output capacitance	C_{oss}	V_{DS} = 10V	-	62	-	
Reverse transfer capacitance	C_{rss}	f = 1MHz	-	50	-	
Turn - on delay time	$t_{d(on)}$ *4	V_{DD} ≃ 15V, V_{GS} = 10V	-	7.2	-	ns
Rise time	t_r *4	I_D = 2.2A	-	8.0	-	
Turn - off delay time	$t_{d(off)}$ *4	R_L = 6.8Ω	-	12.0	-	
Fall time	t_f *4	R_G = 10Ω	-	5.7	-	

●Gate charge characteristics (T_a = 25°C)

<Tr1>

Parameter	Symbol	Conditions		Values			Unit
				Min.	Typ.	Max.	
Total gate charge	Q_g*4	V_{DD} ≃ -15V I_D = -3A	V_{GS} = -10V	-	7.8	-	nC
			V_{GS} = -4.5V	-	4.3	-	
Gate - Source charge	Q_{gs}*4			-	1.6	-	
Gate - Drain charge	Q_{gd}*4			-	1.5	-	

<Tr2>

Parameter	Symbol	Conditions		Values			Unit
				Min.	Typ.	Max.	
Total gate charge	Q_g*4	V_{DD} ≃ 15V I_D = 4.5A	V_{GS} = 10V	-	8.4	-	nC
			V_{GS} = 4.5V	-	4.7	-	
Gate - Source charge	Q_{gs}*4			-	1.7	-	
Gate - Drain charge	Q_{gd}*4			-	1.6	-	

●Body diode electrical characteristics (Source-Drain) (T_a = 25°C)

<Tr1>

Parameter	Symbol	Conditions	Values			Unit
			Min.	Typ.	Max.	
Continuous forward current	I_S	T_a = 25°C	-	-	-1.0	A
Pulse forward current	I_{SP}*2		-	-	-30	
Forward voltage	V_{SD}*4	V_{GS} = 0V, I_S = -1.0A	-	-	-1.2	V

<Tr2>

Parameter	Symbol	Conditions	Values			Unit
			Min.	Typ.	Max.	
Continuous forward current	I_S	T_a = 25°C	-	-	1.0	A
Pulse forward current	I_{SP}*2		-	-	30	
Forward voltage	V_{SD}*4	V_{GS} = 0V, I_S = 1.0A	-	-	1.2	V

●Electrical characteristic curves <Tr1>

Fig.1 Power Dissipation Derating Curve

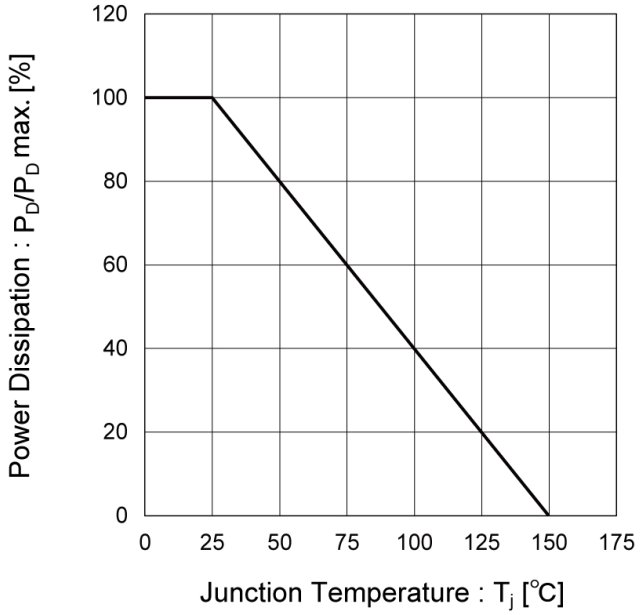


Fig.2 Maximum Safe Operating Area

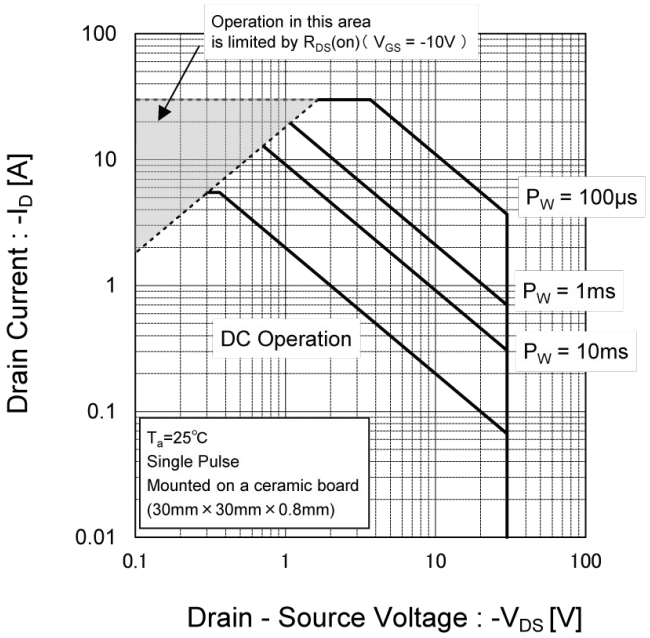


Fig.3 Normalized Transient Thermal Resistance vs. Pulse Width

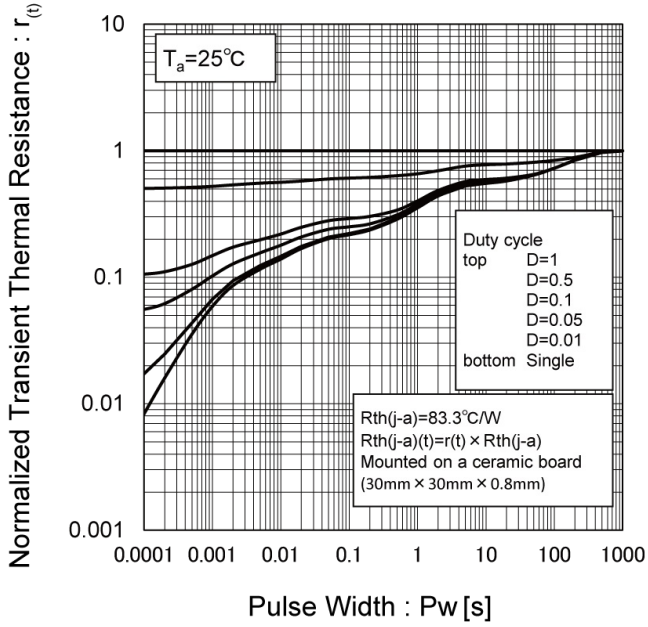
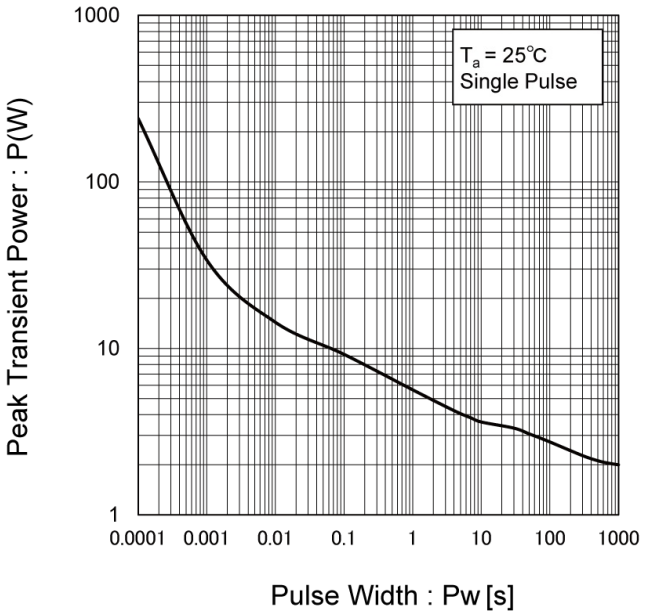


Fig.4 Single Pulse Maximum Power Dissipation



●Electrical characteristic curves <Tr1>

Fig.5 Typical Output Characteristics(I)

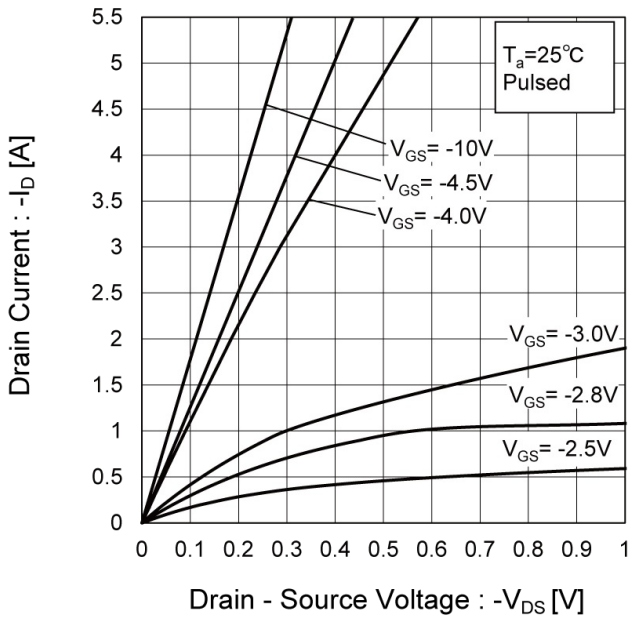


Fig.6 Typical Output Characteristics(II)

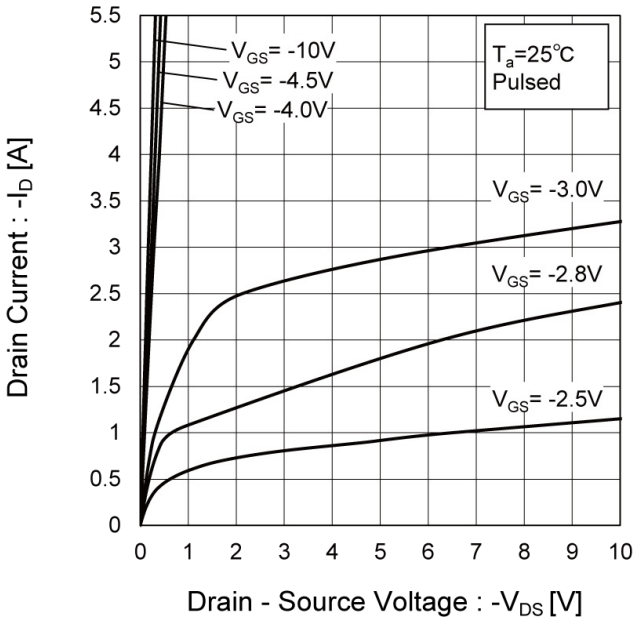
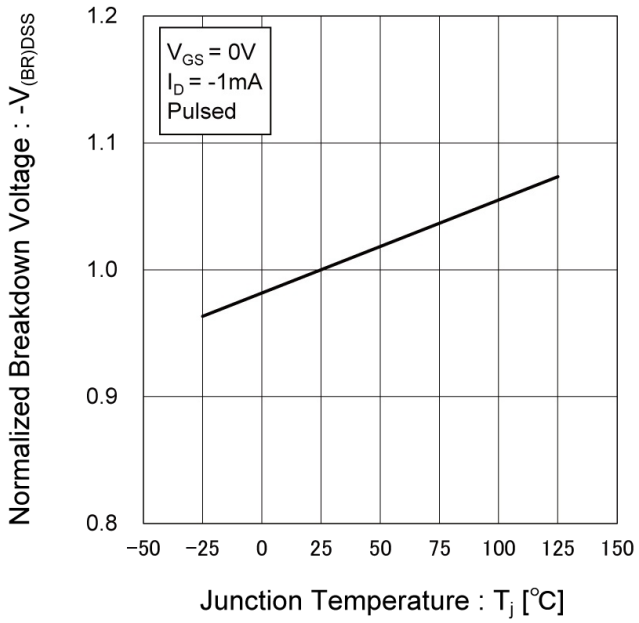


Fig.7 Breakdown Voltage vs. Junction Temperature



●Electrical characteristic curves <Tr1>

Fig.8 Typical Transfer Characteristics

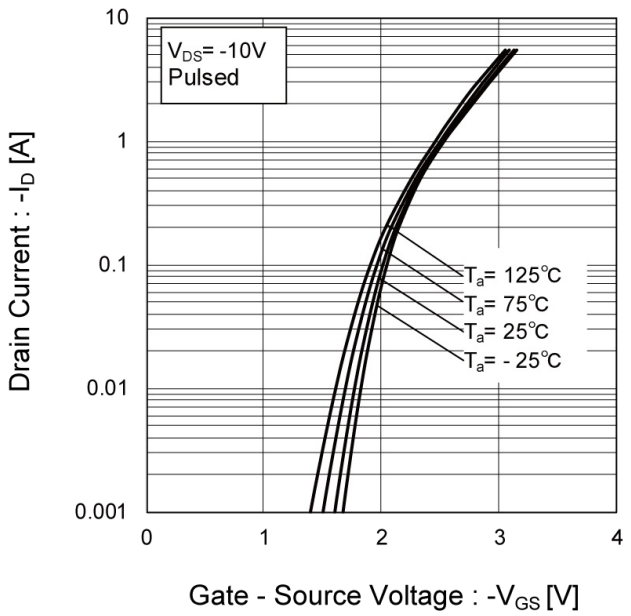


Fig.9 Gate Threshold Voltage vs. Junction Temperature

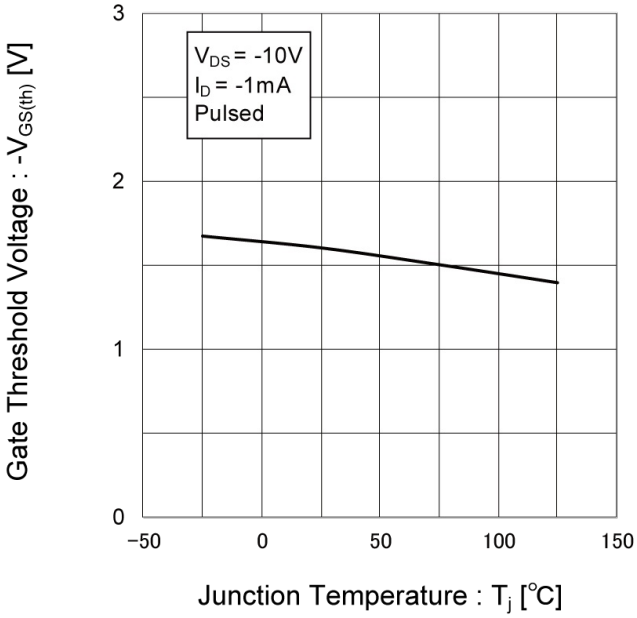
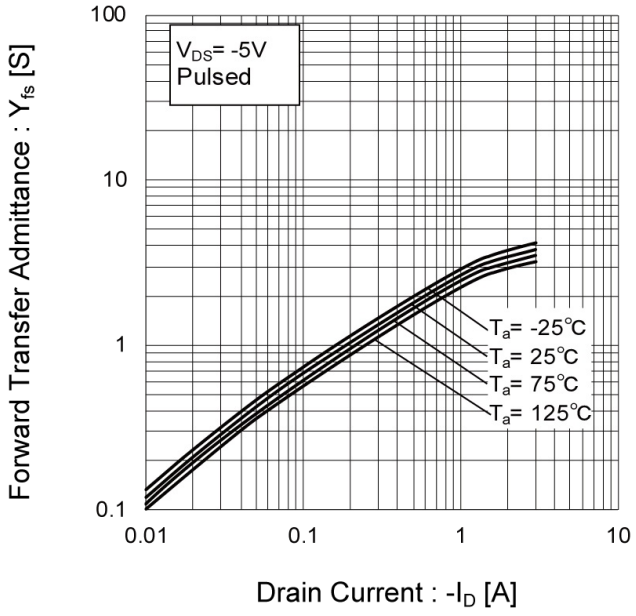


Fig.10 Forward Transfer Admittance vs. Drain Current



●Electrical characteristic curves <Tr1>

Fig.11 Drain Current Derating Curve

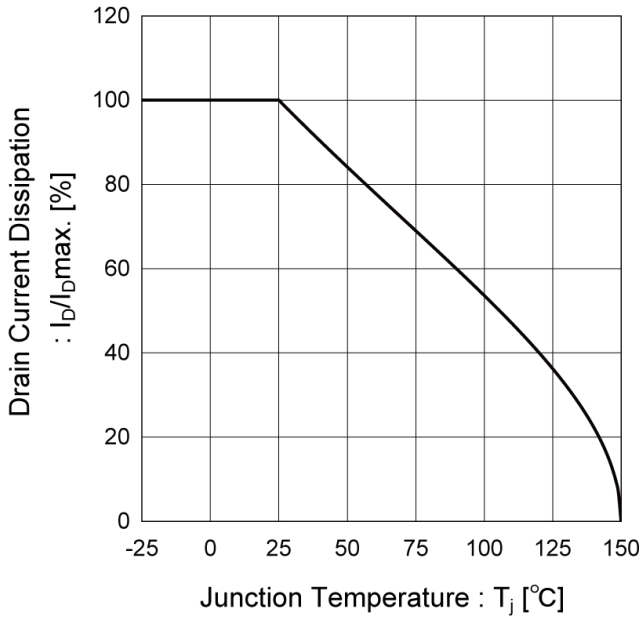


Fig.12 Static Drain - Source On - State Resistance vs. Gate Source Voltage

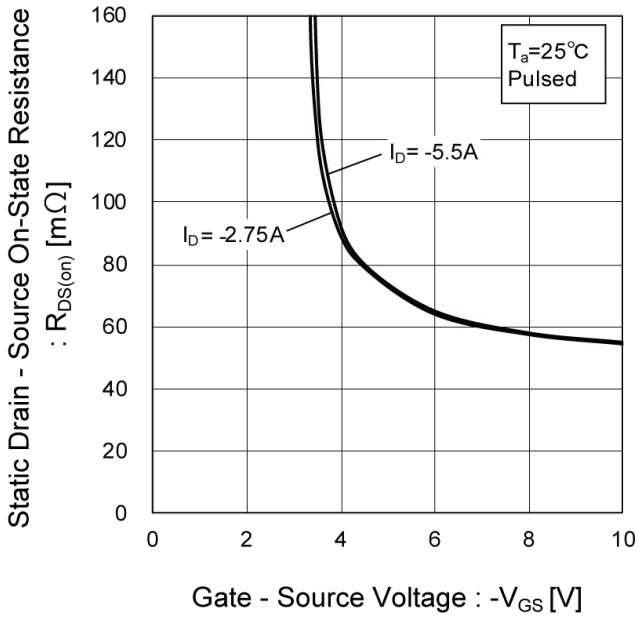
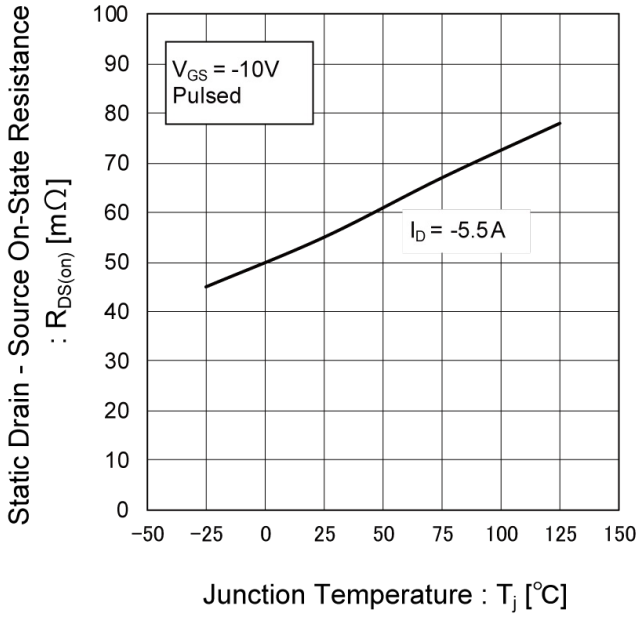


Fig.13 Static Drain - Source On - State Resistance vs. Junction Temperature



●Electrical characteristic curves <Tr1>

Fig.14 Static Drain - Source On - State Resistance vs. Drain Current (I)

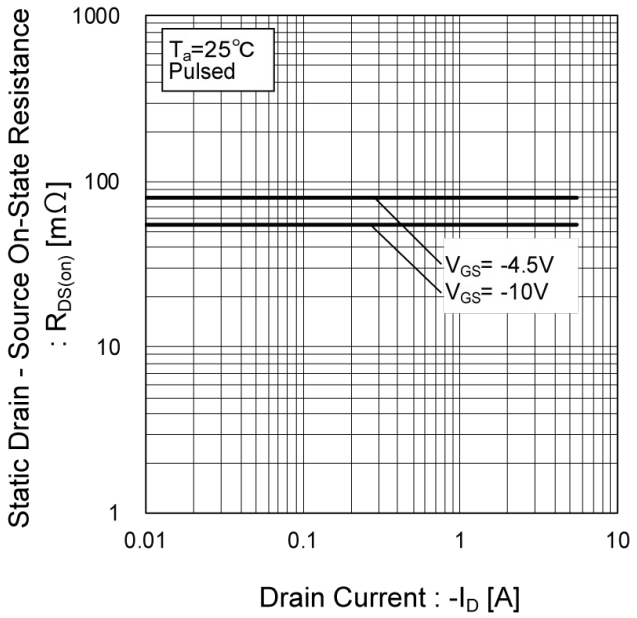


Fig.15 Static Drain - Source On - State Resistance vs. Drain Current (II)

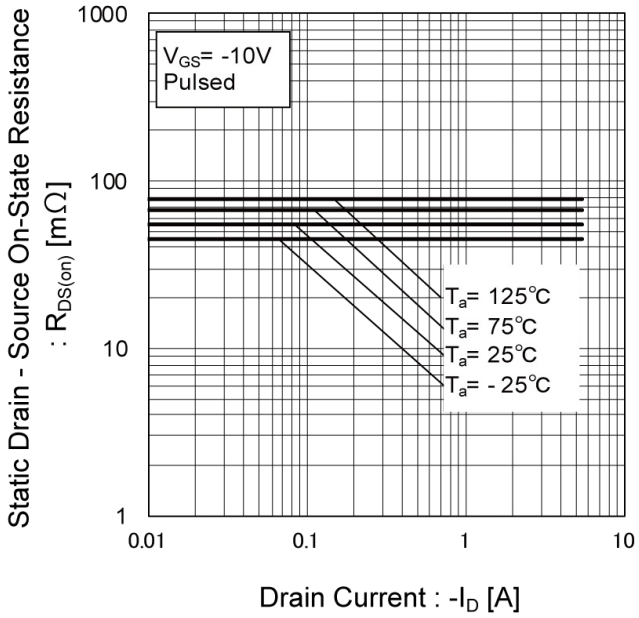
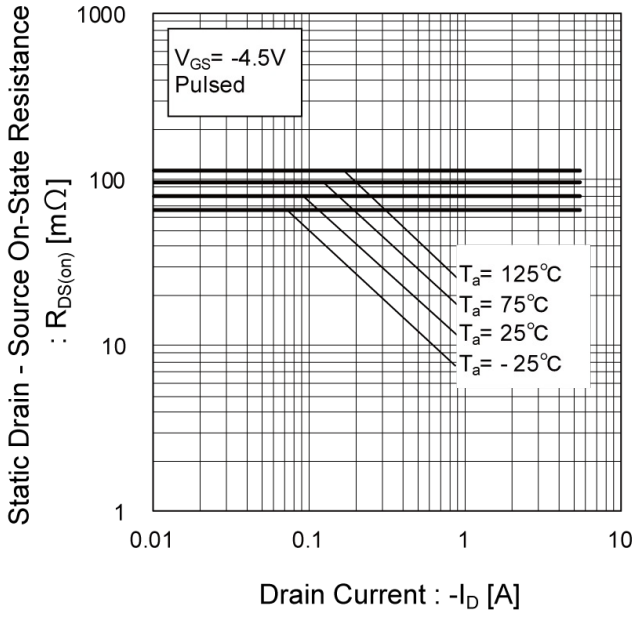


Fig.16 Static Drain - Source On - State Resistance vs. Drain Current (III)



●Electrical characteristic curves <Tr1>

Fig.17 Typical Capacitances vs. Drain - Source Voltage

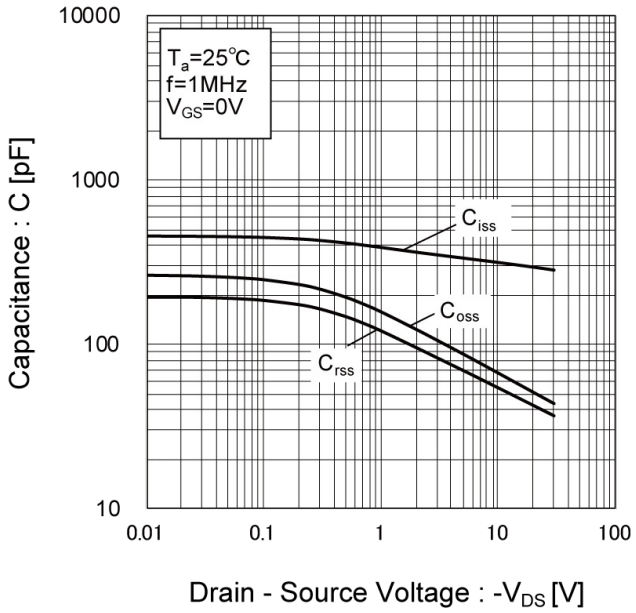


Fig.18 Switching Characteristics

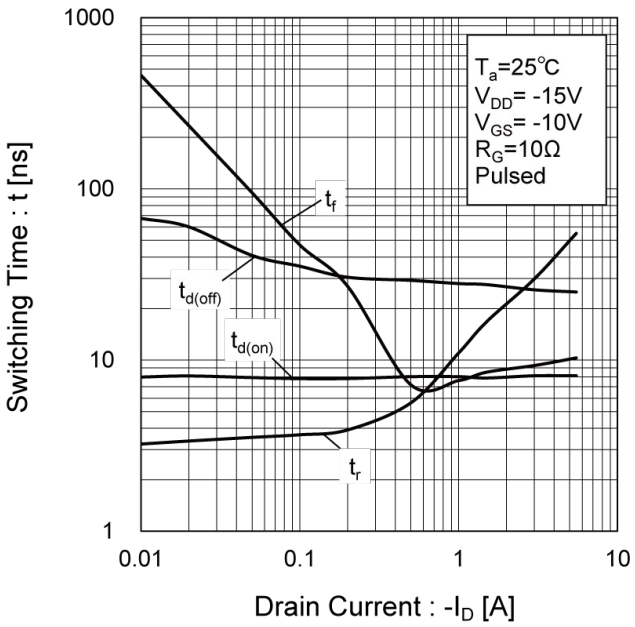


Fig.19 Typical Gate Charge

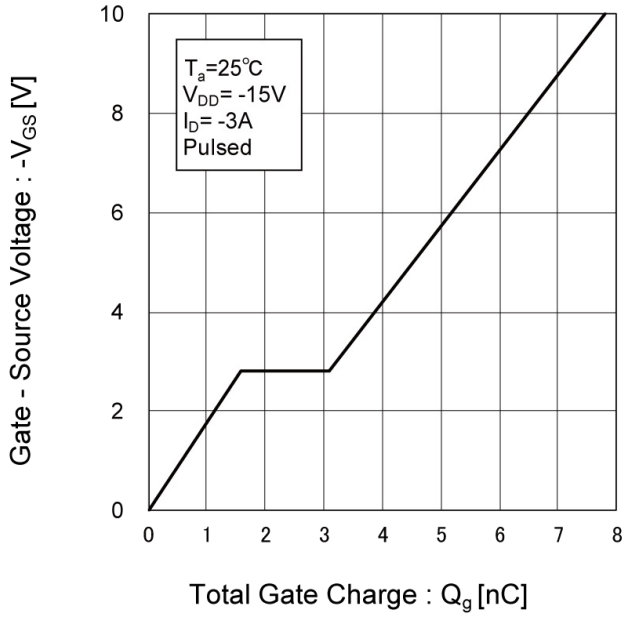
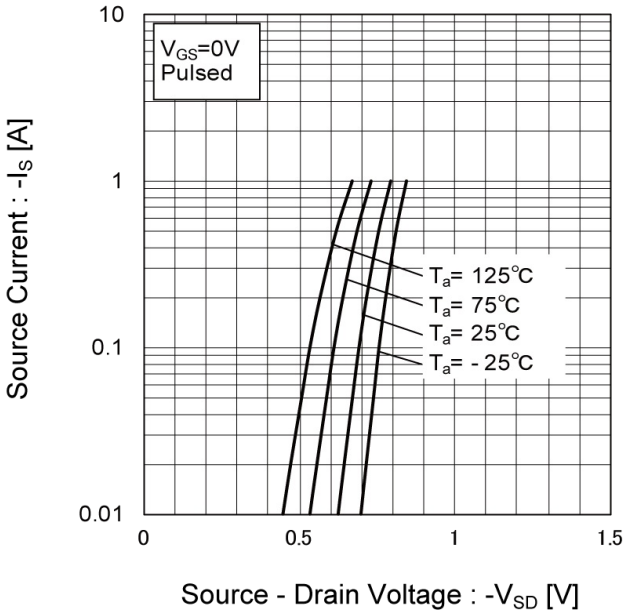


Fig.20 Source Current vs. Source Drain Voltage



●Electrical characteristic curves <Tr2>

Fig.1 Power Dissipation Derating Curve

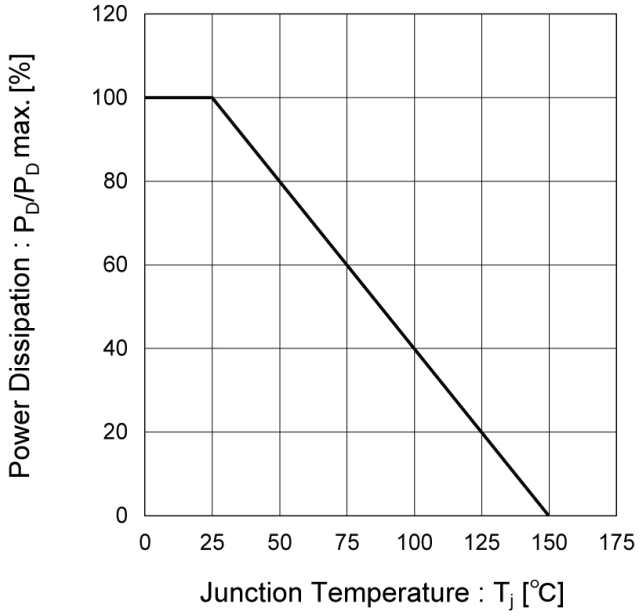


Fig.2 Maximum Safe Operating Area

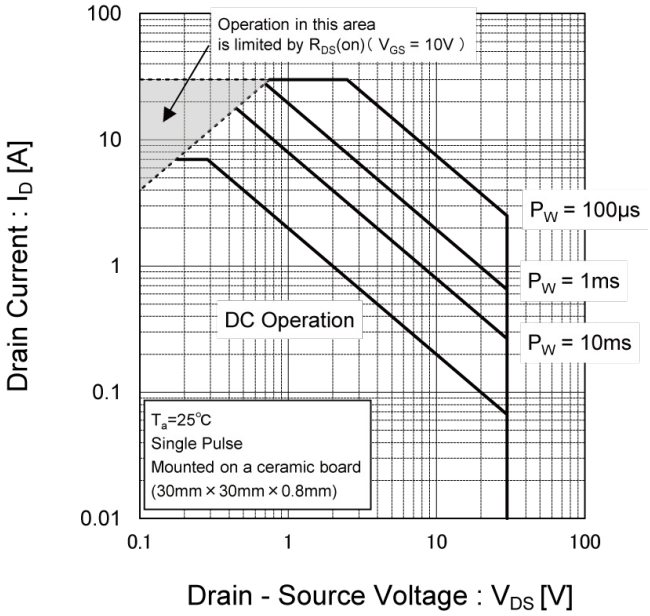


Fig.3 Normalized Transient Thermal Resistance vs. Pulse Width

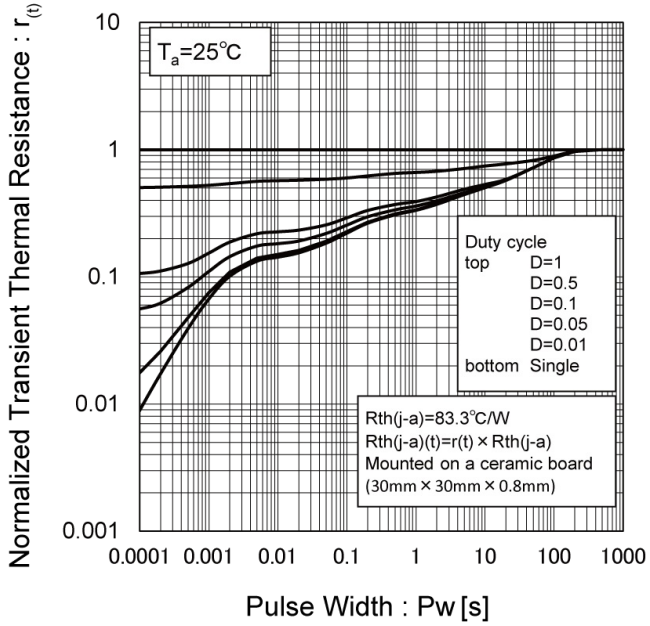
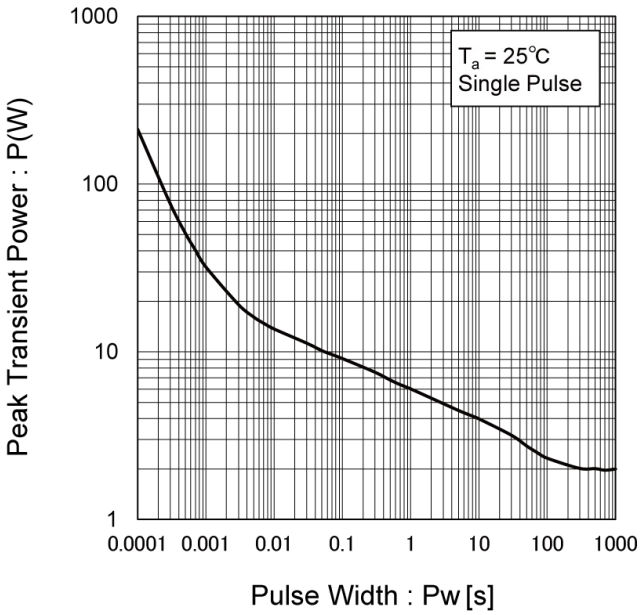


Fig.4 Single Pulse Maximum Power Dissipation



●Electrical characteristic curves <Tr2>

Fig.5 Typical Output Characteristics(I)

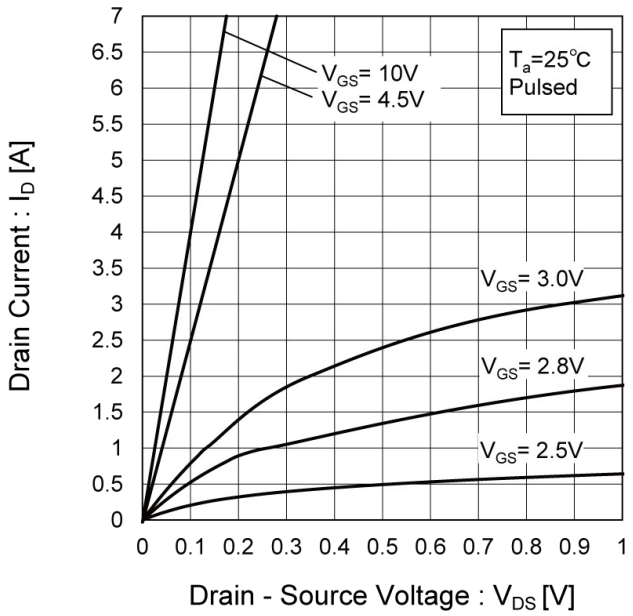


Fig.6 Typical Output Characteristics(II)

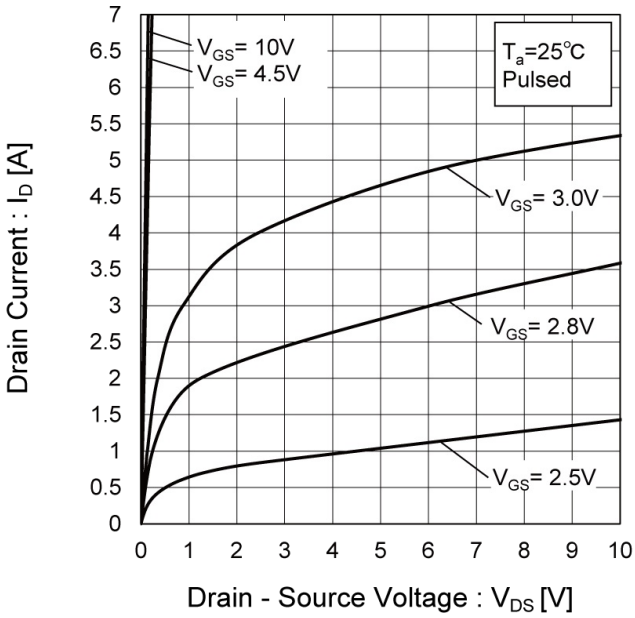
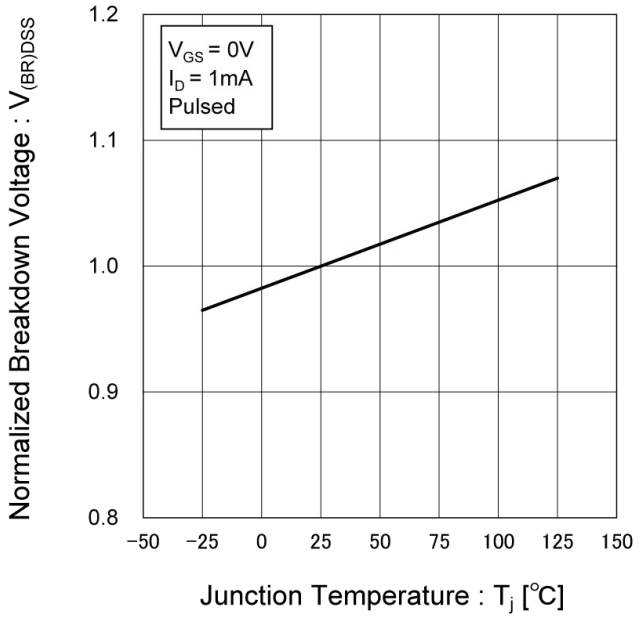


Fig.7 Breakdown Voltage vs. Junction Temperature



●Electrical characteristic curves <Tr2>

Fig.8 Typical Transfer Characteristics

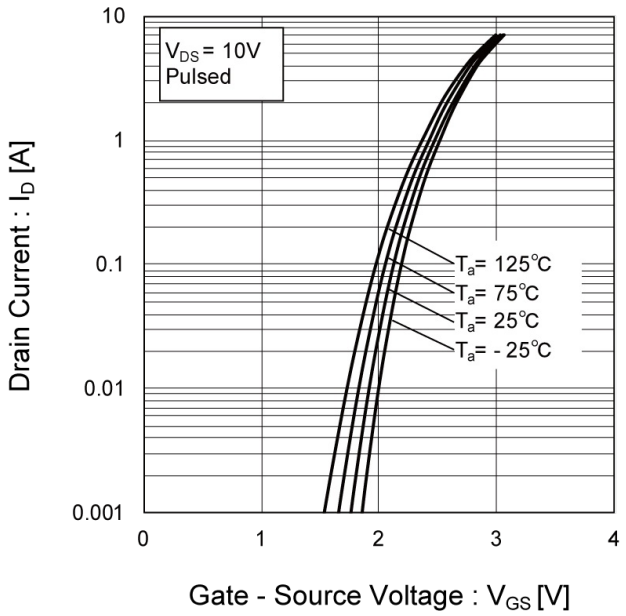


Fig.9 Gate Threshold Voltage vs. Junction Temperature

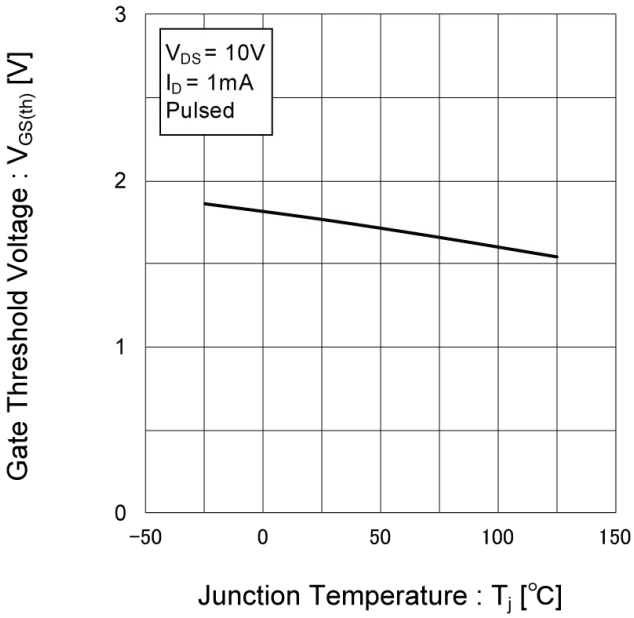
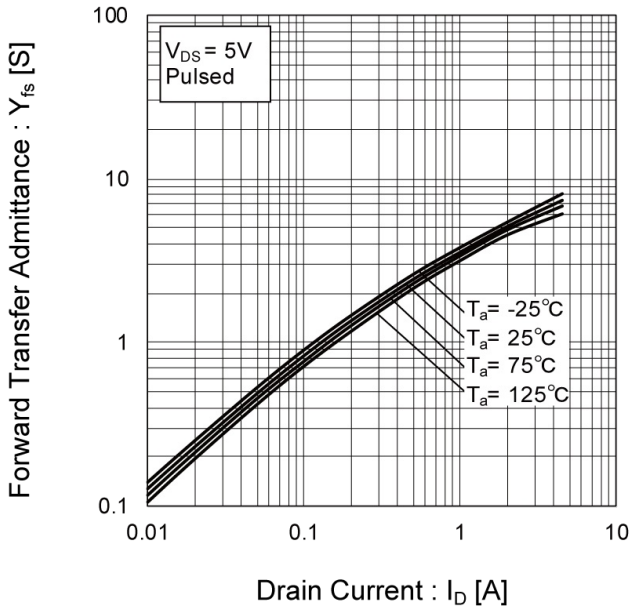


Fig.10 Forward Transfer Admittance vs. Drain Current



●Electrical characteristic curves <Tr2>

Fig.11 Drain Current Derating Curve

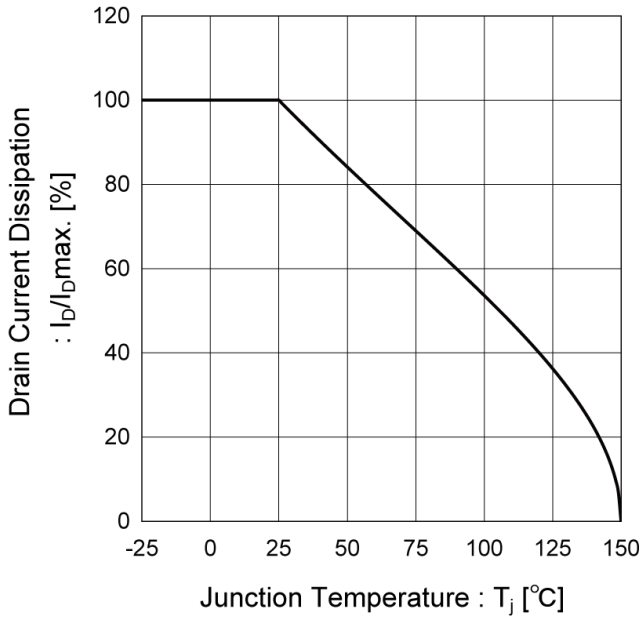


Fig.12 Static Drain - Source On - State Resistance vs. Gate Source Voltage

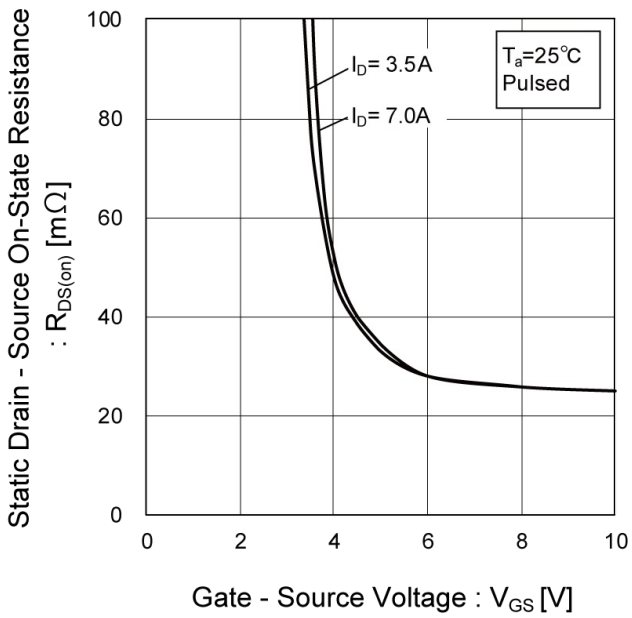
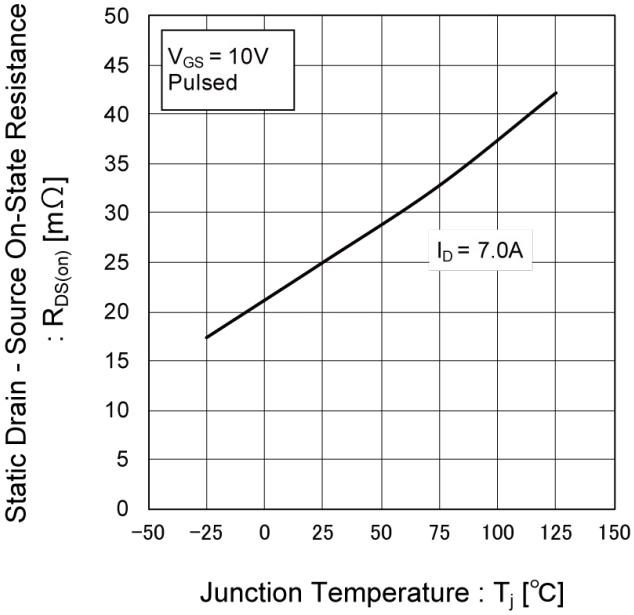


Fig.13 Static Drain - Source On - State Resistance vs. Junction Temperature



●Electrical characteristic curves <Tr2>

Fig.14 Static Drain - Source On - State Resistance vs. Drain Current (I)

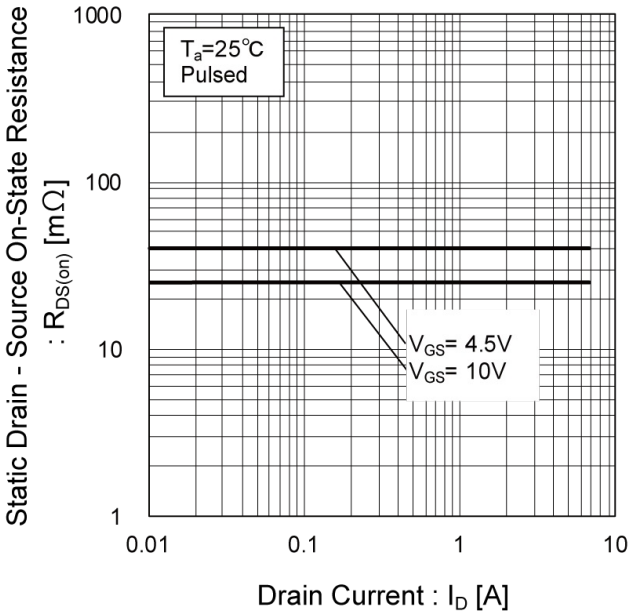


Fig.15 Static Drain - Source On - State Resistance vs. Drain Current (II)

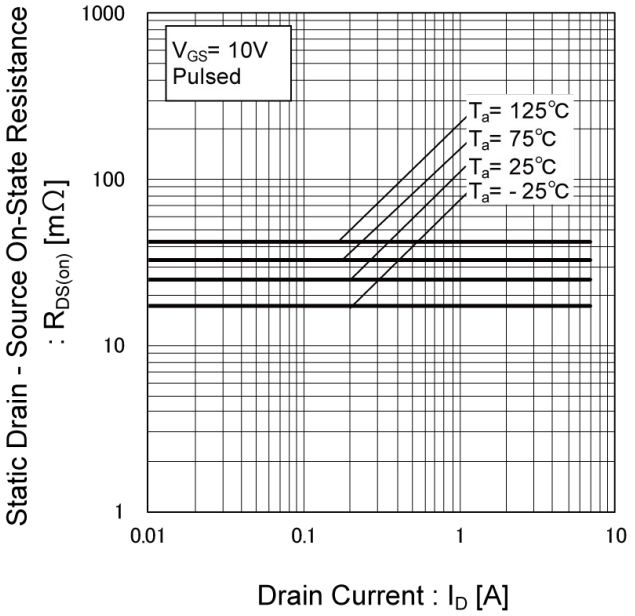
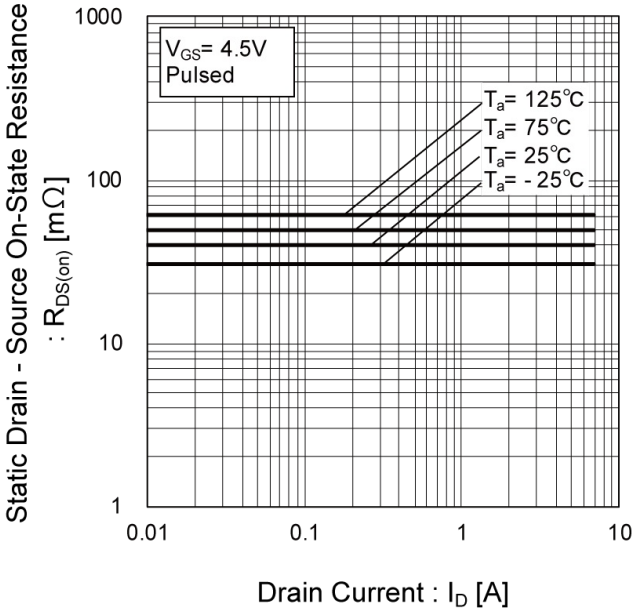


Fig.16 Static Drain - Source On - State Resistance vs. Drain Current (III)



●Electrical characteristic curves <Tr2>

Fig.17 Typical Capacitances vs. Drain - Source Voltage

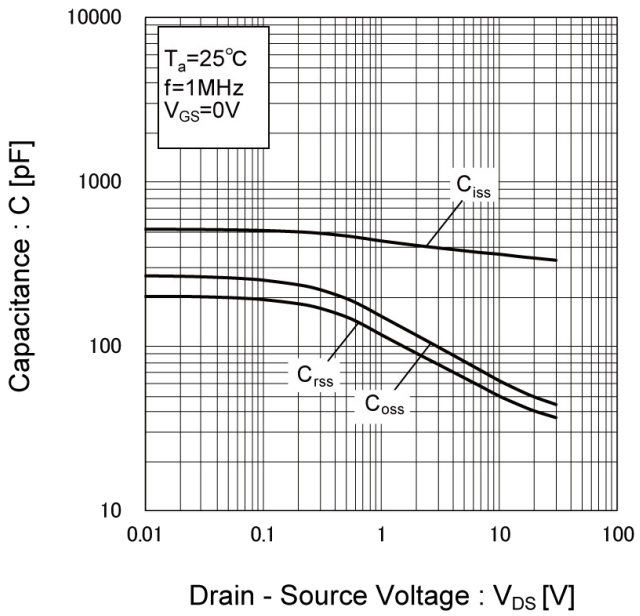


Fig.18 Switching Characteristics

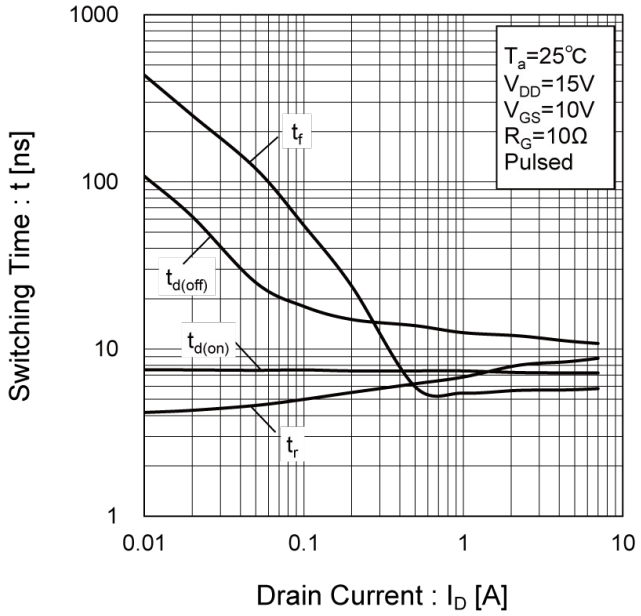


Fig.19 Typical Gate Charge

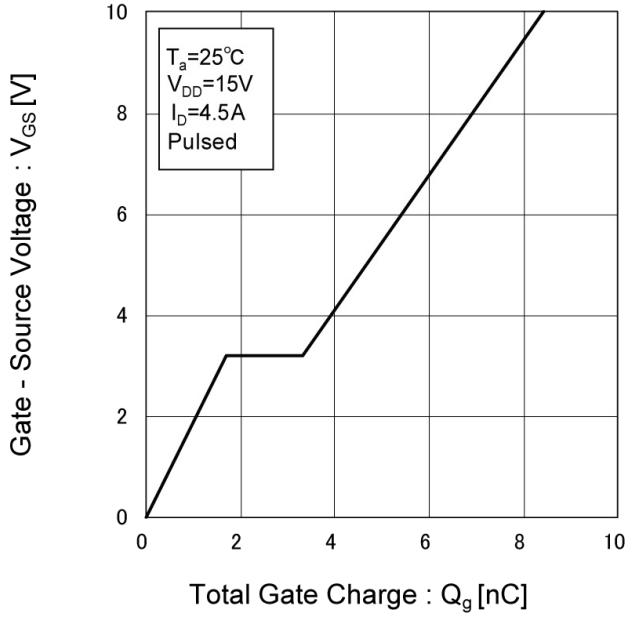
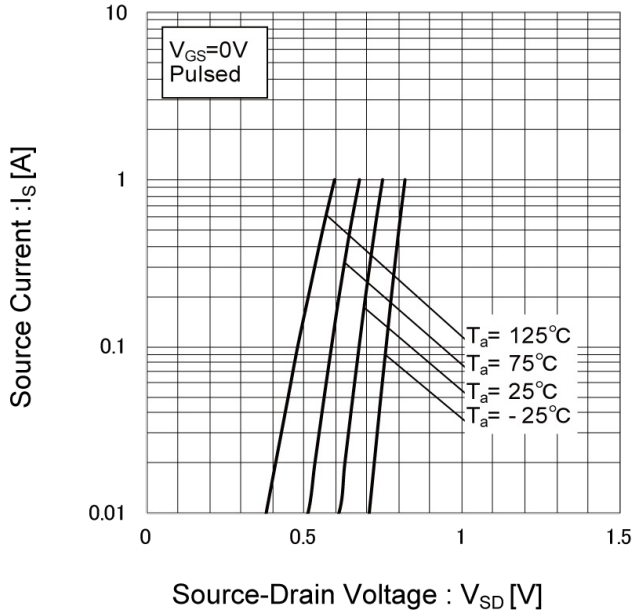


Fig.20 Source Current vs. Source Drain Voltage



●Measurement circuits <Tr1>

Fig.1-1 Switching Time Measurement Circuit

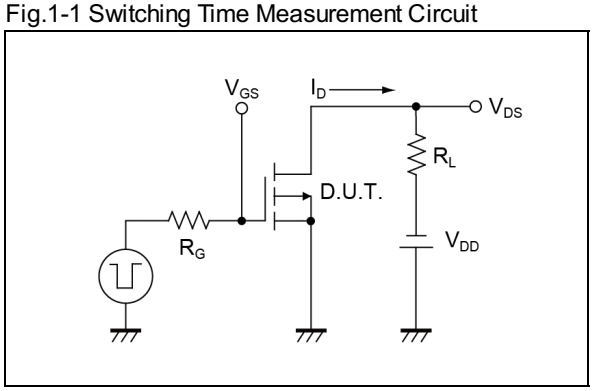


Fig.1-2 Switching Waveforms

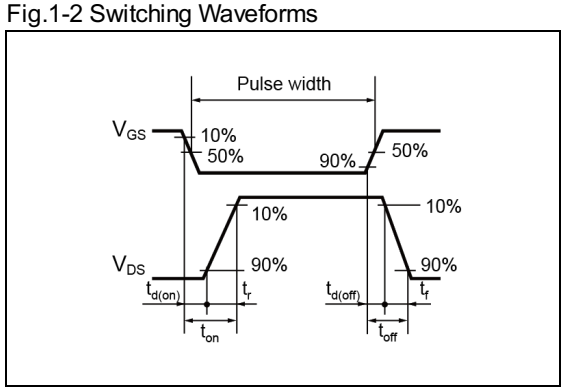


Fig.2-1 Gate Charge Measurement Circuit

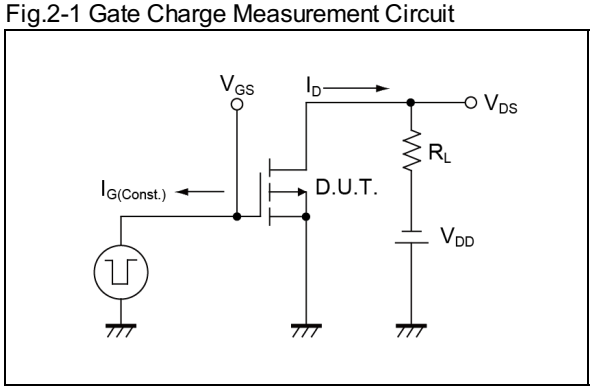
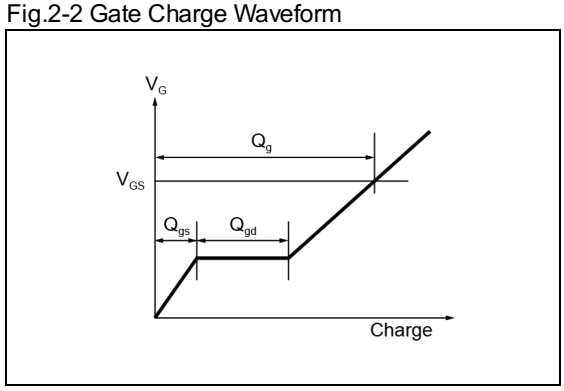


Fig.2-2 Gate Charge Waveform



●Measurement circuits <Tr2>

Fig.3-1 Switching Time Measurement Circuit

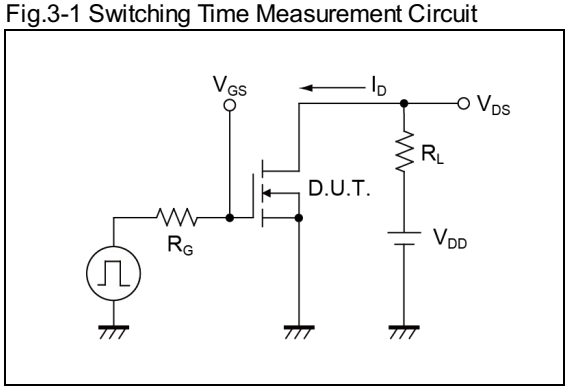


Fig.3-2 Switching Waveforms

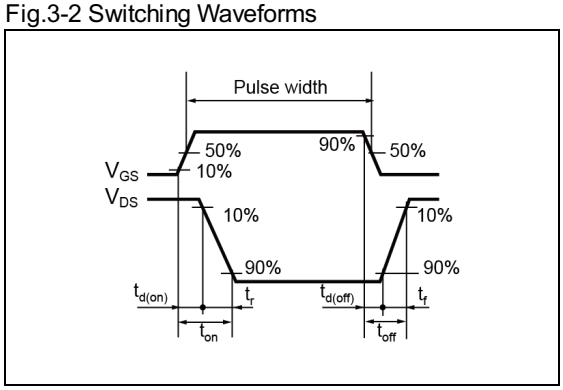


Fig.4-1 Gate Charge Measurement Circuit

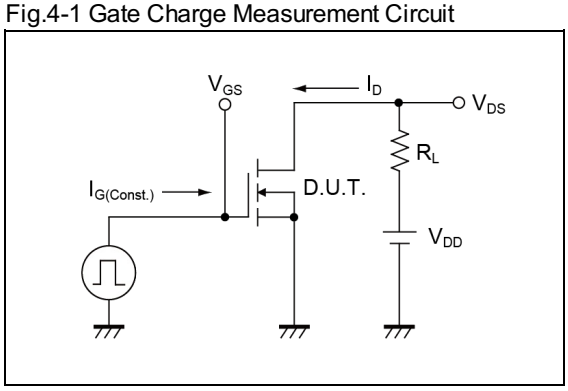
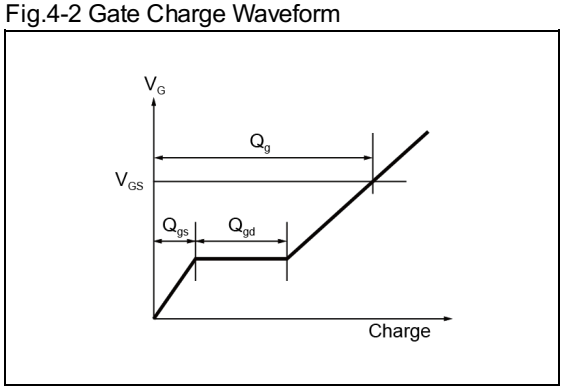


Fig.4-2 Gate Charge Waveform



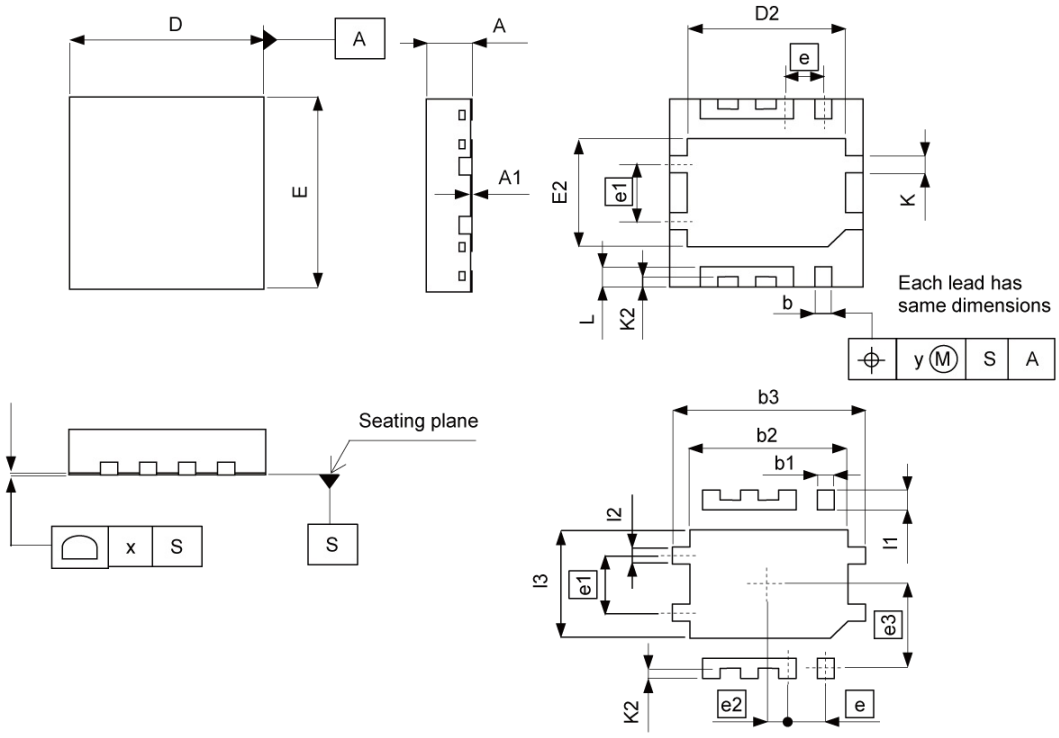
●Notice

This product might cause chip aging and breakdown under the large electrified environment.
Please consider to design ESD protection circuit.

●Dimensions

HSML3333L9

(Drain common)



Pattern of terminal position areas
[Not a recommended pattern of soldering pads]

DIM	MILIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.70	0.80	0.028	0.032
A1	0.00	0.05	0.000	0.002
b	0.25	0.35	0.010	0.014
D	3.20	3.40	0.126	0.134
D2	2.65	2.75	0.104	0.108
E	3.20	3.40	0.126	0.134
E2	1.80	2.00	0.071	0.079
e	0.65		0.026	
e1	1.00		0.039	
K	0.30		0.012	
K2	0.175		0.007	
L	0.30	0.40	0.012	0.016
x	0.10		0.004	
y	0.10		0.004	

DIM	MILIMETERS		INCHES	
	MIN	MAX	MIN	MAX
b1	-	0.45	-	0.018
b2	-	2.75	-	0.108
b3	-	3.40	-	0.134
e2	0.325		0.013	
e3	1.45		0.057	
l1	-	0.50	-	0.020
l2	-	0.35	-	0.014
l3	-	2.00	-	0.079

Dimension in mm/inches