

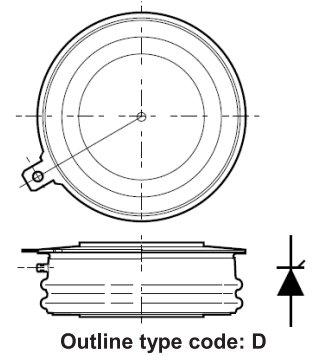


Features

- Double Side Cooling
- High Surge Capability

Applications

- High Power Drives
- High Voltage Power Supplies
- Static Switches



Key Parameters

V _{DRM}	I _{T(AV)}	I _{TSM}	dV/dt*	dI/dt
1800V	860A	11500A	1000V/μs	200A/μs

*Higher dV/dt selections available

Voltage Ratings

Part Number	Repetitive Peak Voltages V _{DRM} and V _{VRRM} V	Conditions
MPRD520T140	1800	T _{vj} = -40°C to +125°C, I _{DRM} = I _{VRRM} = 50mA, V _{DRM} , V _{VRRM} t _p = 10ms, V _{DSM} & V _{VSRM} = V _{DRM} & V _{VRRM} +100V respectively

Current Ratings

T_{case} = 60°C unless stated otherwise

Symbol	Parameter	Test Conditions	Max.	Units
Double Side Cooled				
I _{T(AV)}	Mean on-state current	Half wave resistive load	860	A
I _{T(RMS)}	RMS value	-	1350	
I _T	Continuous (direct) on-state current	-	1220	

Surge Ratings

Symbol	Parameter	Test Conditions	Max.	Units
I _{TSM}	Surge (non-repetitive) on-state current	10ms half sine, T _{case} = 125°C V _R = 0	11.5	kA
I ² t	I ² t for fusing		0.661	MA ² s

Thermal and Mechanical Ratings

Symbol	Parameter	Test Conditions		Min.	Max.	Units
$R_{th(j-c)}$	Thermal resistance – junction to case	Double side cooled	DC	-	0.035	°C/W
$R_{th(c-h)}$	Thermal resistance – case to heatsink	Double side cooled	DC	-	0.01	°C/W
T_{vj}	Virtual junction temperature	Blocking V_{DRM} / V_{RRM}		-	125	°C
T_{stg}	Storage temperature range			-40	140	°C
F_m	Clamping force			8	12	kN

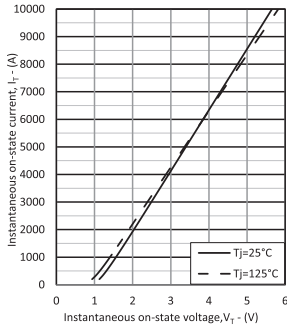
Dynamic Characteristics

Symbol	Parameter	Test Conditions		Min.	Max.	Units
I_{RRM}/I_{DRM}	Peak reverse and off-state current	At V_{RRM}/V_{DRM} , $T_{case} = 125^\circ\text{C}$		-	50	mA
dV/dt	Max. linear rate of rise of off-state voltage	To 67% V_{DRM} , $T_j = 125^\circ\text{C}$, gate open		1000	-	V/ μs
di/dt	Rate of rise of on-state current	From 67% V_{DRM} to 1000A Gate source 30V, 10 Ω , $t_r < 0.5\text{ms}$, $T_j = 125^\circ\text{C}$	Repetitive 50Hz	-	200	A/ μs
			Non-repetitive	-	1000	A/ μs
V_T	On-state voltage	$I_T = 1500\text{A}$, $T_{case} = 125^\circ\text{C}$		-	1.65	V
$V_{T(RO)}$	Threshold voltage	$T_{case} = 125^\circ\text{C}$		-	0.90	V
r_T	On-state slope resistance	$T_{case} = 125^\circ\text{C}$		-	0.50	m Ω
t_{gd}	Delay time	$V_D = 67\% V_{DRM}$, gate source 30V, 10 Ω $t_r = 0.5\mu\text{s}$, $T_j = 25^\circ\text{C}$		-	3.0	μs
t_q	Turn-off time	$T_j = 125^\circ\text{C}$, $V_R = 100\text{V}$, $di/dt = 10\text{A}/\mu\text{s}$, $dV_{DR}/dt = 20\text{V}/\mu\text{s}$ linear to 67% V_{DRM}		-	150	μs
Q_S	Stored charge	$I_T = 1000\text{A}$, $t_p = 1000\mu\text{s}$, $T_j = 125^\circ\text{C}$, $di/dt = 10\text{A}/\mu\text{s}$,		-	1500	μC
I_{RR}	Reverse recovery current			-	105	A
I_L	Latching current	$T_j = 25^\circ\text{C}$,		-	1	A
I_H	Holding current	$T_j = 25^\circ\text{C}$,		-	200	mA

Gate Trigger Characteristics and Ratings

Symbol	Parameter	Test Conditions	Max.	Units
V_{GT}	Gate trigger voltage	$V_{DRM} = 5\text{V}$, $T_{case} = 25^\circ\text{C}$	3	V
V_{GD}	Gate non-trigger voltage	At 40% V_{DRM} , $T_{case} = 125^\circ\text{C}$	0.3	V
I_{GT}	Gate trigger current	$V_{DRM} = 5\text{V}$, $T_{case} = 25^\circ\text{C}$	300	mA
I_{GD}	Gate non-trigger current	At 40% V_{DRM} , $T_{case} = 125^\circ\text{C}$	20	mA

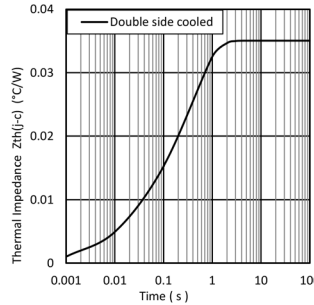
Curves



V_{TM} EQUATION

$$V_{TM} = A + B \ln(I_T) + C I_T + D \ln I_T$$

Where $A = 0.239798$
 $B = 0.138469$
 $C = 0.000533$
 $D = -0.010242$
 These values are valid for $T_j = 125^\circ\text{C}$

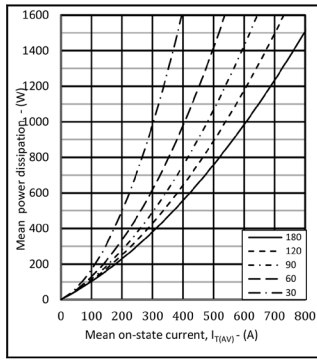


$$R_{th(j-c)}(t) = \sum_{i=1}^n R_{th,i} \left(1 - e^{-\frac{t}{\tau_i}} \right)$$

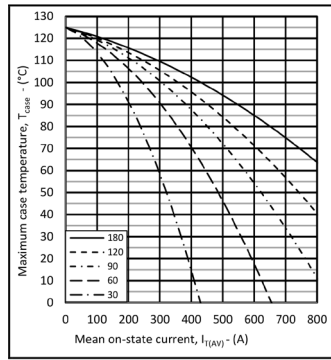
i	τ_i (s)	$R_{th,i}$ ($^\circ\text{C/kW}$)
1	0.5391689	15.7
2	0.1940576	11.19235
3	0.0219527	6.412673
4	0.0021962	1.759765

Maximum & minimum on-state characteristics

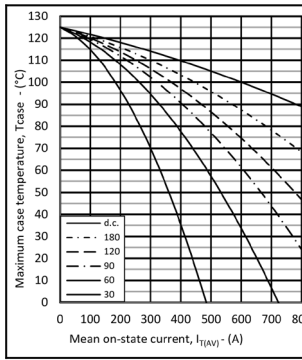
Maximum (limit) transient thermal impedance – junction to case ($^\circ\text{C/W}$)



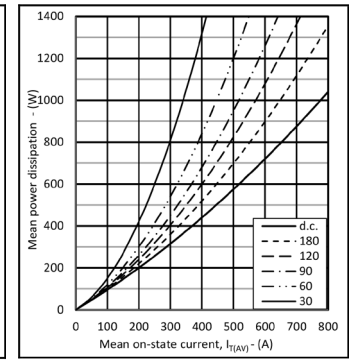
On-state power dissipation – sine wave



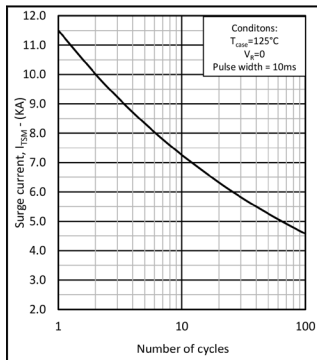
Maximum permissible case temperature, double side cooled – sine wave



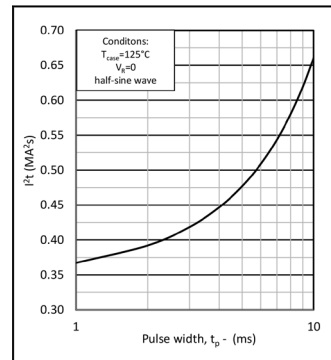
Maximum permissible case temperature, double side cooled – rectangular wave



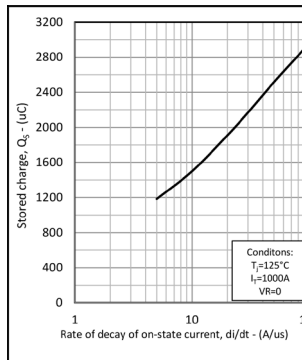
On-state power dissipation – rectangular wave



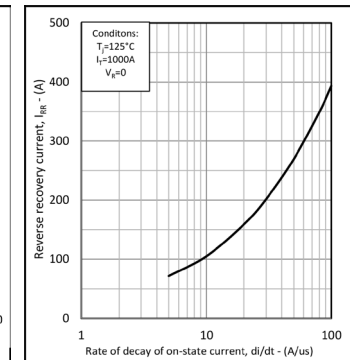
Multi-cycle surge current



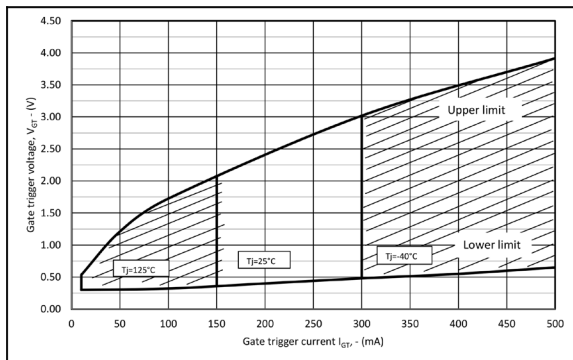
Single-cycle I_T



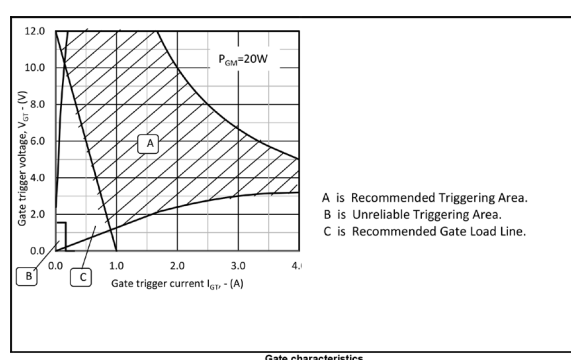
Stored charge vs di/dt



Reverse recovery current vs di/dt

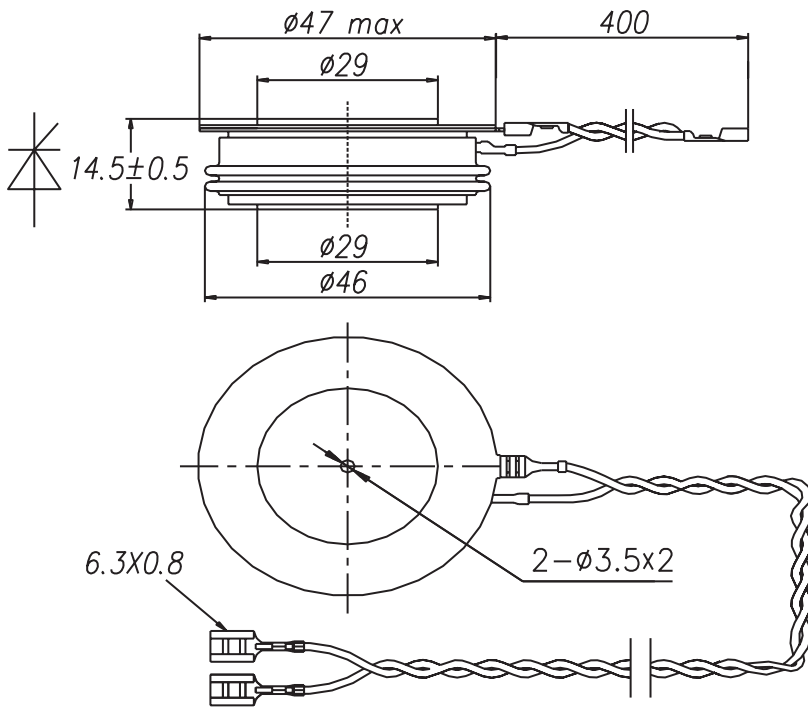


Gate characteristics



Gate characteristics

Diagram



Package outline type code: D

Part Number Table

Description	Part Number
Rectifier Diode Module, 1800V, 520A, D Case Code	MPRD520T140

Dimensions : Millimetres

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