

OptiMOS™-5 Power-Transistor



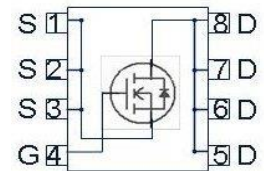
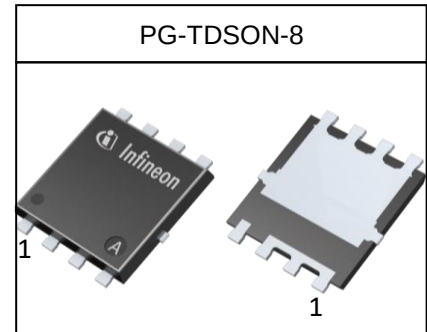
Features

- OptiMOS™ - power MOSFET for automotive applications
- N-channel - Enhancement mode - Normal level
- AEC Q101 qualified
- MSL1 up to 260°C peak reflow
- Green product (RoHS compliant)
- 100% Avalanche tested
- Feasible for automatic optical inspection (AOI)

Type	Package	Marking
IAUC90N10S5N062	PG-TDSON-8	5N10N062

Product Summary

V_{DS}	100	V
$R_{DS(on)}$	6.2	mΩ
I_D	90	A



Maximum ratings, at $T_j=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current ¹⁾	I_D	$T_C=25\text{ °C}, V_{GS}=10\text{V}$	90	A
		$T_C=100\text{ °C}, V_{GS}=10\text{V}$	66	
Pulsed drain current ¹⁾	$I_{D,pulse}$	$T_C=25\text{ °C}$	360	
Avalanche energy, single pulse ¹⁾	E_{AS}	$I_D=45\text{A}$	112	mJ
Avalanche current, single pulse	I_{AS}	-	47	A
Gate source voltage	V_{GS}	-	±20	V
Power dissipation	P_{tot}	$T_C=25\text{ °C}, T_J=175\text{ °C}$	115	W
Operating and storage temperature	T_j, T_{stg}	-	-55 ... +175	°C

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Thermal characteristics¹⁾

Thermal resistance, junction - case	R_{thJC}	-	-	-	1.3	K/W
Thermal resistance, junction - ambient, leaded	R_{thJA}	6 cm ² cooling area ²⁾	-	-	50	

Electrical characteristics, at $T_j=25\text{ °C}$, unless otherwise specified

Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=1mA$	100	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=59\mu A$	2.2	3.0	3.8	
Zero gate voltage drain current	I_{DSS}	$V_{DS}=100V, V_{GS}=0V, T_j=25\text{ °C}$	-	-	1	μA
		$V_{DS}=100V, V_{GS}=0V, T_j=125\text{ °C}^{1)}$	-	-	20	
Gate-source leakage current	I_{GSS}	$V_{GS}=20V, V_{DS}=0V$	-	-	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=6V, I_D=23A$	-	6.5	7.8	m Ω
		$V_{GS}=10V, I_D=45A$	-	5.2	6.2	
Gate resistance ¹⁾	R_G		-	1	-	Ω

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics¹⁾

Input capacitance	C_{iss}	$V_{GS}=0\text{ V}, V_{DS}=50\text{ V},$ $f=1\text{ MHz}$	-	2519	3275	pF
Output capacitance	C_{oss}		-	403	524	
Reverse transfer capacitance	C_{rss}		-	20.5	31	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=50\text{ V}, V_{GS}=10\text{ V},$ $I_D=90\text{ A}, R_G=3.5\Omega$	-	6	-	ns
Rise time	t_r		-	2	-	
Turn-off delay time	$t_{d(off)}$		-	10	-	
Fall time	t_f		-	8	-	

Gate Charge characteristics¹⁾

Gate to source charge	Q_{gs}	$V_{DD}=50\text{ V}, I_D=45\text{ A},$ $V_{GS}=0\text{ to }10\text{ V}$	-	12	16	nC
Gate to drain charge	Q_{gd}		-	7.6	11.4	
Gate charge total	Q_g		-	36	48	
Gate plateau voltage	$V_{plateau}$		-	4.7	-	V

Reverse Diode

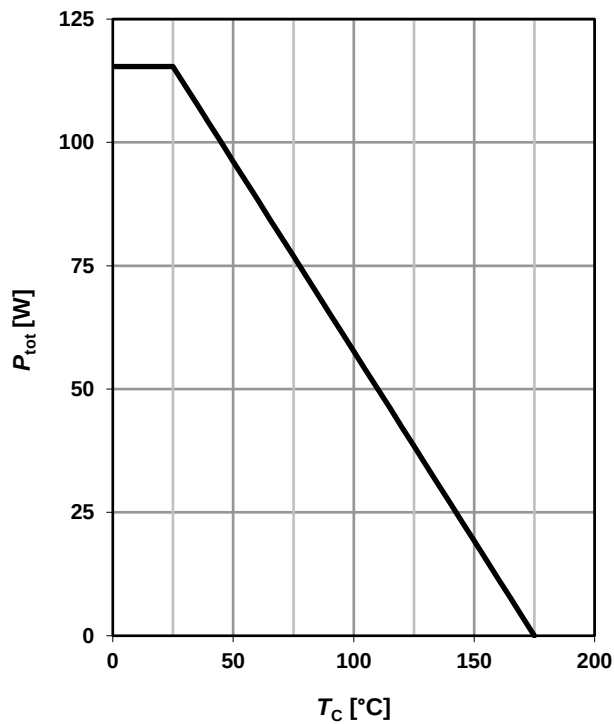
Diode continuous forward current ¹⁾	I_S	$T_C=25^\circ\text{C}$	-	-	90	A
Diode pulse current ¹⁾	$I_{S,pulse}$		-	-	360	
Diode forward voltage	V_{SD}	$V_{GS}=0\text{ V}, I_F=45\text{ A},$ $T_J=25^\circ\text{C}$	-	0.9	1.1	V
Reverse recovery time ¹⁾	t_{rr}	$V_R=50\text{ V}, I_F=50\text{ A},$ $di_F/dt=100\text{ A}/\mu\text{s}$	-	47	-	ns
Reverse recovery charge ¹⁾	Q_{rr}		-	61	-	nC

¹⁾ Defined by design. Not subject to production test.

²⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

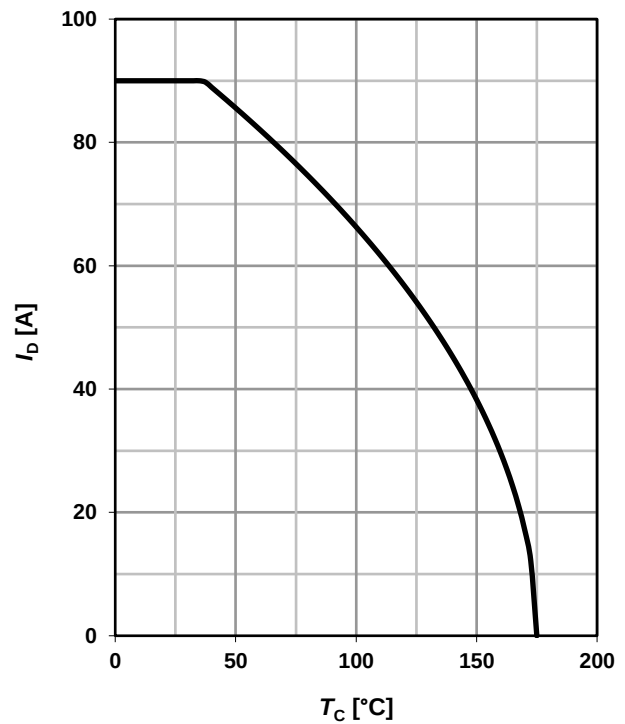
1 Power dissipation

$$P_{\text{tot}} = f(T_C); V_{\text{GS}} \geq 6 \text{ V}$$



2 Drain current

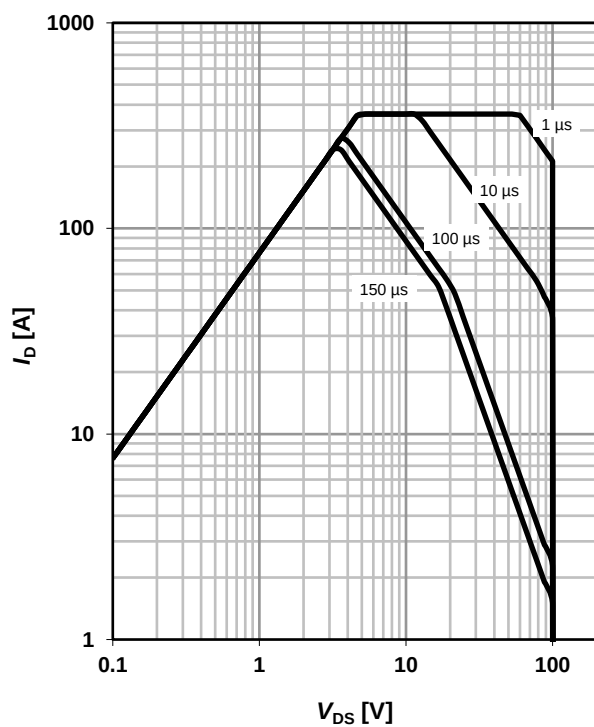
$$I_D = f(T_C); V_{\text{GS}} \geq 6 \text{ V}$$



3 Safe operating area

$$I_D = f(V_{\text{DS}}); T_C = 25^\circ\text{C}; D = 0$$

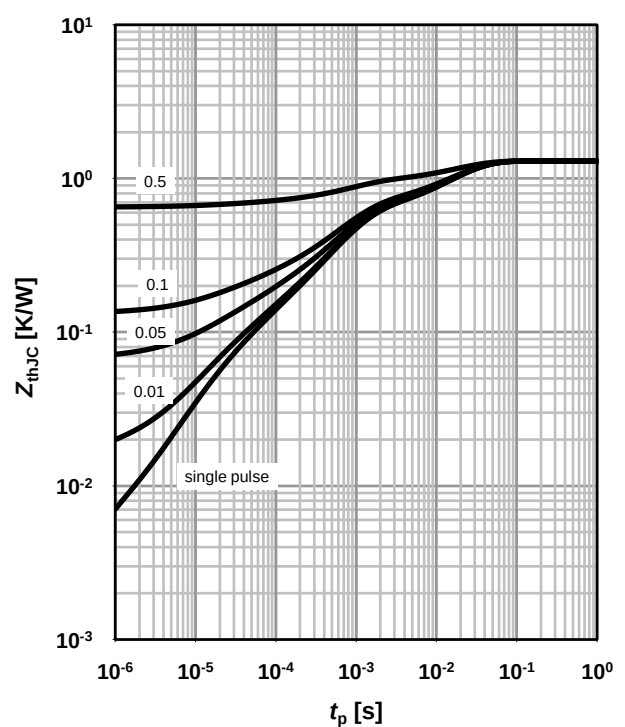
parameter: t_p



4 Max. transient thermal impedance

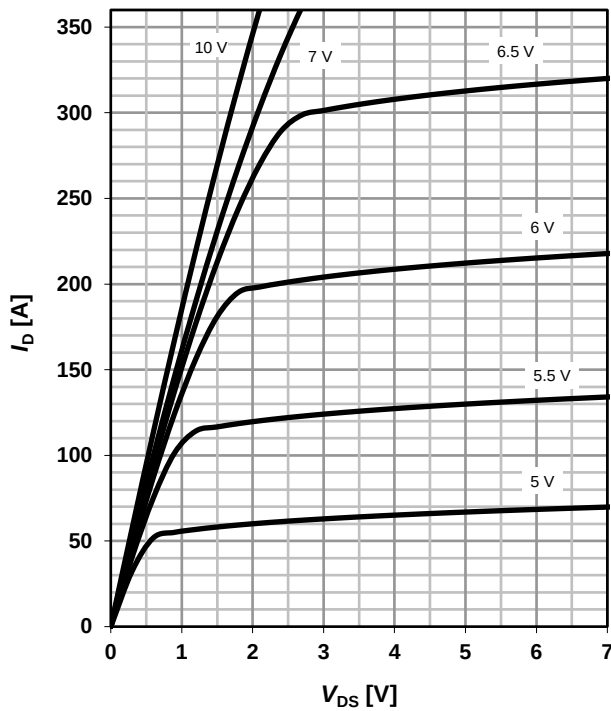
$$Z_{\text{thJC}} = f(t_p)$$

parameter: $D = t_p/T$



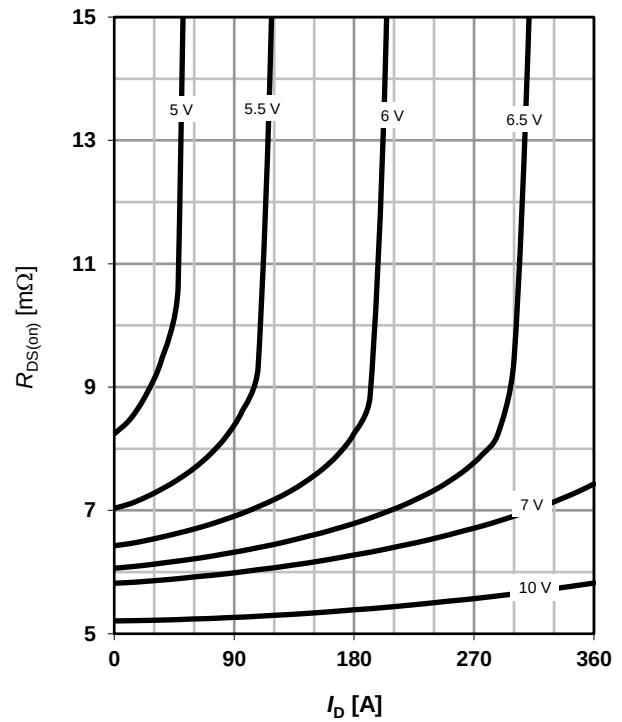
5 Typ. output characteristics

 $I_D = f(V_{DS}); T_j = 25^\circ\text{C}$

parameter: V_{GS}


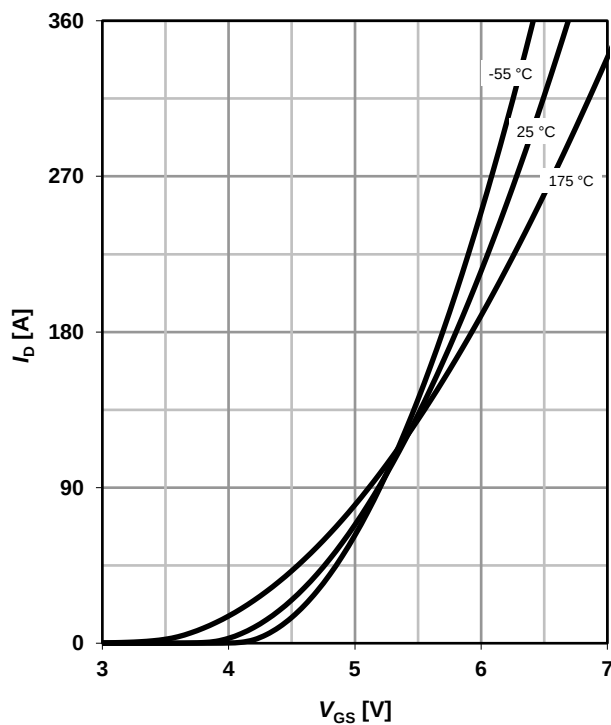
6 Typ. drain-source on-state resistance

 $R_{DS(on)} = f(I_D); T_j = 25^\circ\text{C}$

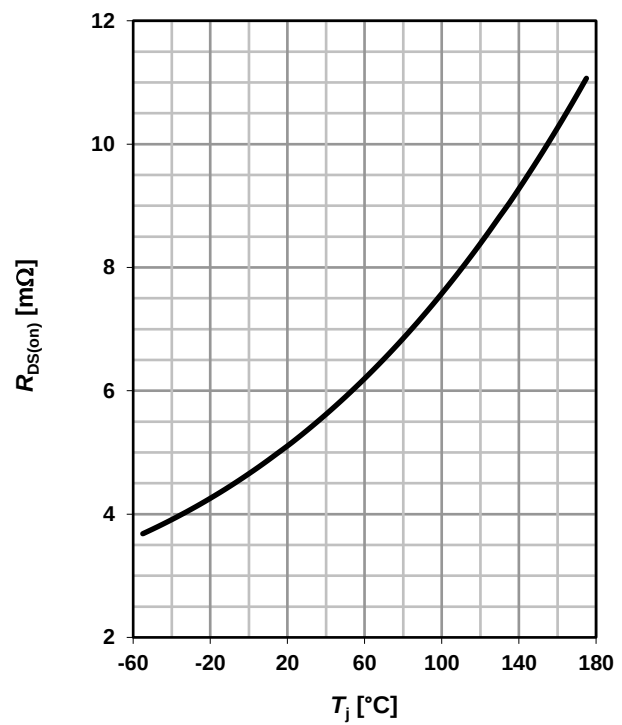
parameter: V_{GS}


7 Typ. transfer characteristics

 $I_D = f(V_{GS}); V_{DS} = 6\text{ V}$

parameter: T_j


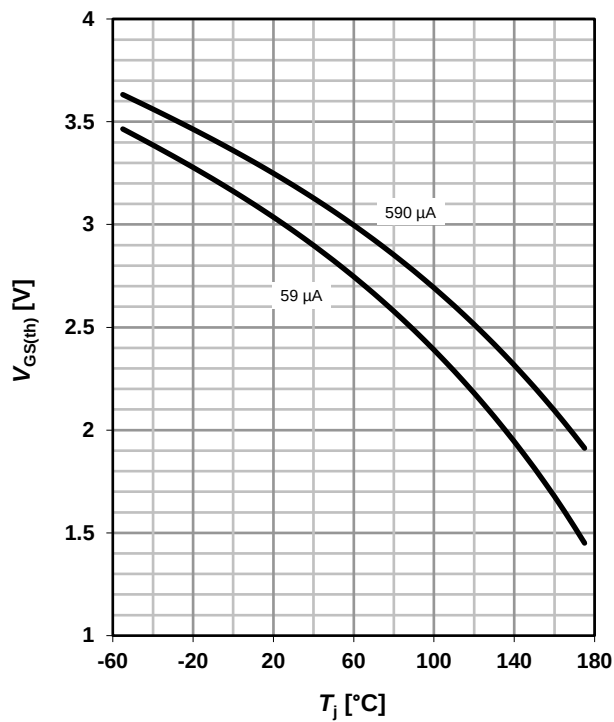
8 Typ. drain-source on-state resistance

 $R_{DS(on)} = f(T_j); I_D = 45\text{ A}; V_{GS} = 10\text{ V}$


9 Typ. gate threshold voltage

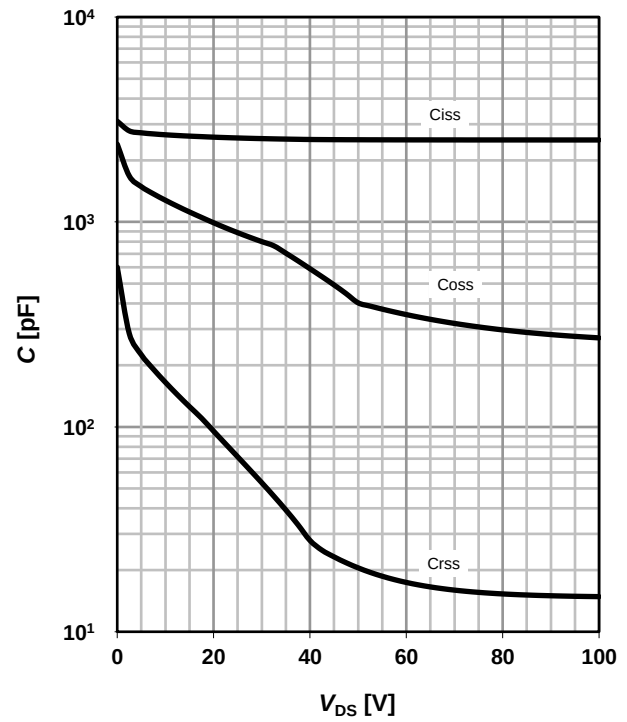
$$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$$

parameter: I_D



10 Typ. capacitances

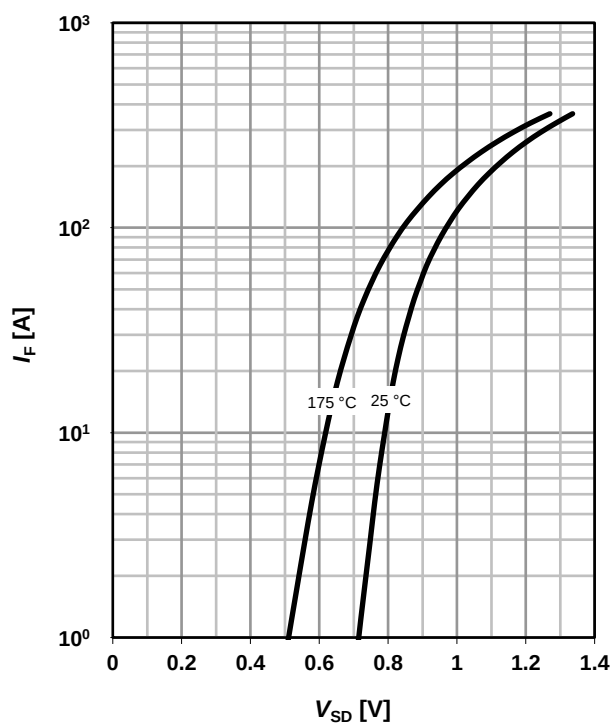
$$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$$



11 Typical forward diode characteristics

$$I_F = f(V_{SD})$$

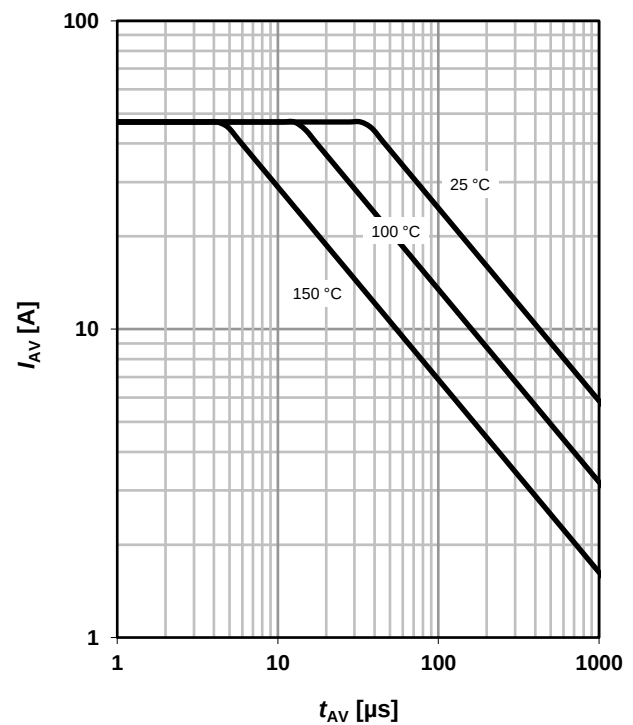
parameter: T_j



12 Typ. avalanche characteristics

$$I_{AS} = f(t_{AV})$$

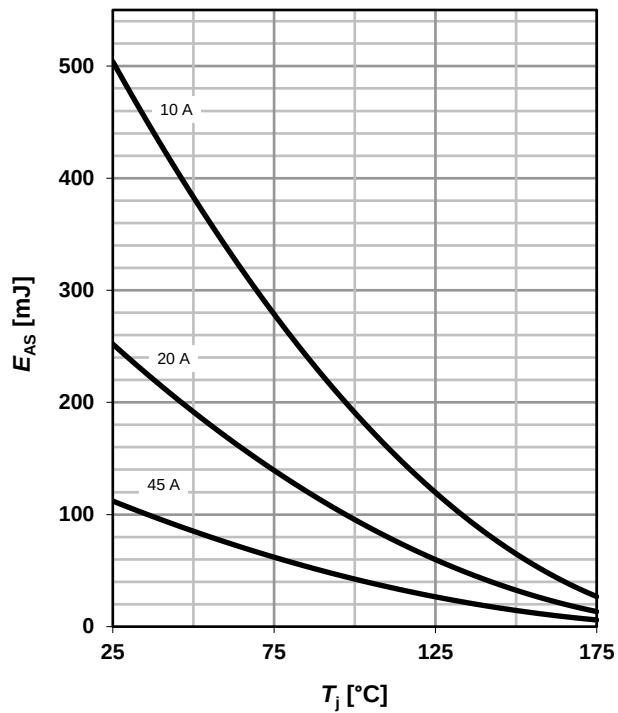
parameter: $T_{j(start)}$



13 Typical avalanche energy

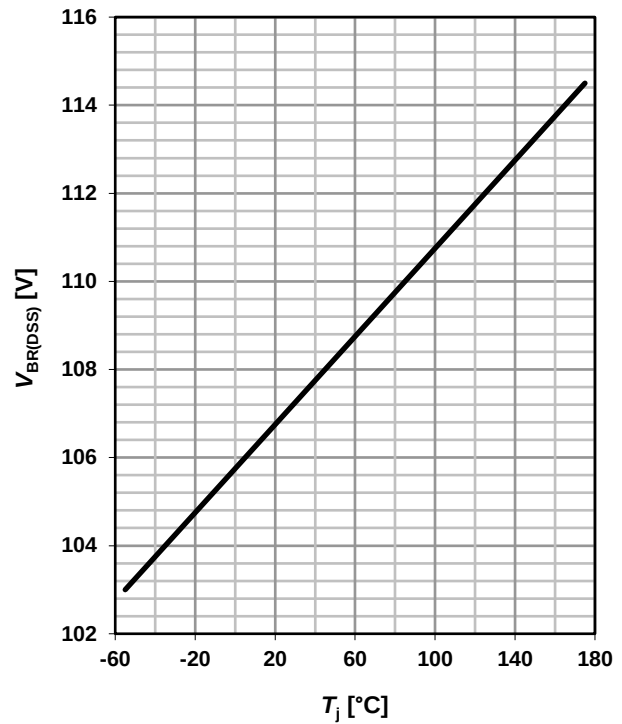
$$E_{AS} = f(T_j)$$

parameter: I_D



14 Drain-source breakdown voltage

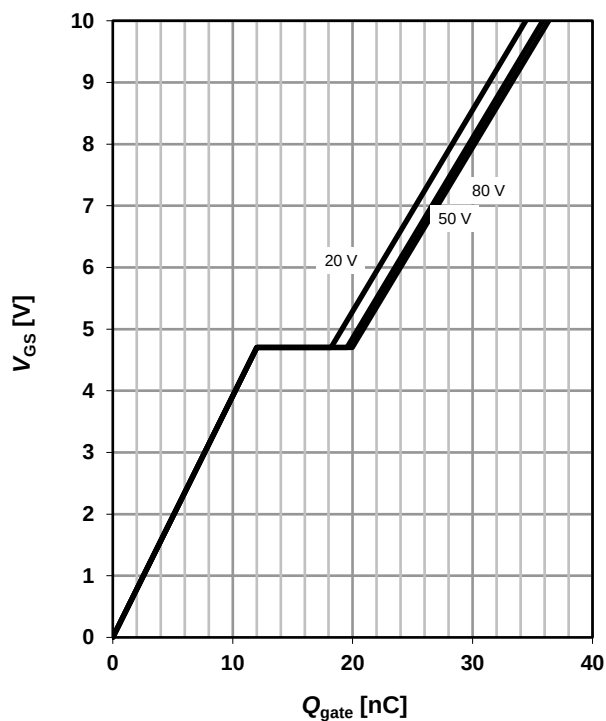
$$V_{BR(DSS)} = f(T_j); I_D = 1 \text{ mA}$$



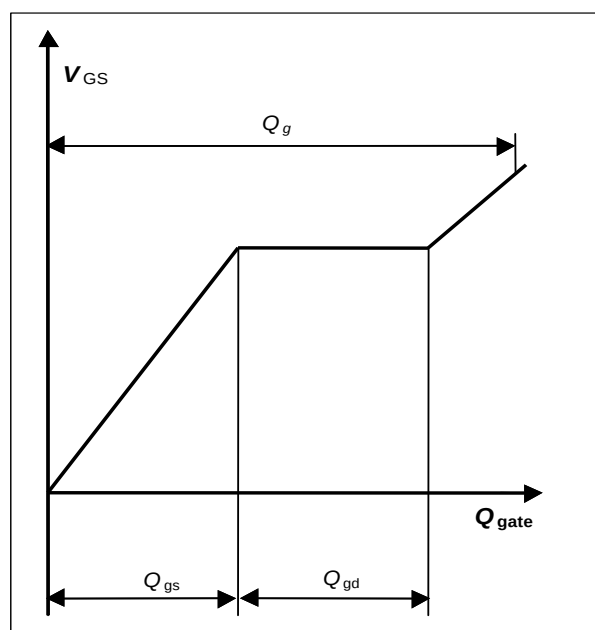
15 Typ. gate charge

$$V_{GS} = f(Q_{gate}); I_D = 45 \text{ A pulsed}$$

parameter: V_{DD}



16 Gate charge waveforms



Technical drawing of a 10-pin D-sub connector housing, showing front, side, and top views with dimensions and feature callouts.

Front View (Left):

- Overall width: 5.15 ± 0.1
- Overall height: 6.44 ± 0.1
- Pin 1 location: 0.44 ± 0.1 from bottom left corner.
- Pin 5 location: 0.13 ± 0.1 from right edge.
- Pin 8 location: 0.48 ± 0.1 from top edge.
- Pin 4 location: 0.44 ± 0.1 from bottom edge.
- Pin 127 location: 1.27 from bottom edge.
- Feature A: 0.25 ± 0.1 from bottom edge.
- Feature B: 0.03 from bottom edge.
- Feature C: 0.03 from bottom edge.
- Feature D: 0.03 from bottom edge.
- Feature E: 0.03 from bottom edge.
- Feature F: 0.03 from bottom edge.
- Feature G: 0.03 from bottom edge.
- Feature H: 0.03 from bottom edge.
- Feature I: 0.03 from bottom edge.
- Feature J: 0.03 from bottom edge.
- Feature K: 0.03 from bottom edge.
- Feature L: 0.03 from bottom edge.
- Feature M: 0.03 from bottom edge.
- Feature N: 0.03 from bottom edge.
- Feature O: 0.03 from bottom edge.
- Feature P: 0.03 from bottom edge.
- Feature Q: 0.03 from bottom edge.
- Feature R: 0.03 from bottom edge.
- Feature S: 0.03 from bottom edge.
- Feature T: 0.03 from bottom edge.
- Feature U: 0.03 from bottom edge.
- Feature V: 0.03 from bottom edge.
- Feature W: 0.03 from bottom edge.
- Feature X: 0.03 from bottom edge.
- Feature Y: 0.03 from bottom edge.
- Feature Z: 0.03 from bottom edge.

Side View (Middle):

- Overall width: 1 ± 0.1
- Overall height: 5.48 ± 0.1
- Feature A: 0.13 ± 0.1 from right edge.
- Feature B: 0.03 from right edge.
- Feature C: 0.03 from right edge.
- Feature D: 0.03 from right edge.
- Feature E: 0.03 from right edge.
- Feature F: 0.03 from right edge.
- Feature G: 0.03 from right edge.
- Feature H: 0.03 from right edge.
- Feature I: 0.03 from right edge.
- Feature J: 0.03 from right edge.
- Feature K: 0.03 from right edge.
- Feature L: 0.03 from right edge.
- Feature M: 0.03 from right edge.
- Feature N: 0.03 from right edge.
- Feature O: 0.03 from right edge.
- Feature P: 0.03 from right edge.
- Feature Q: 0.03 from right edge.
- Feature R: 0.03 from right edge.
- Feature S: 0.03 from right edge.
- Feature T: 0.03 from right edge.
- Feature U: 0.03 from right edge.
- Feature V: 0.03 from right edge.
- Feature W: 0.03 from right edge.
- Feature X: 0.03 from right edge.
- Feature Y: 0.03 from right edge.
- Feature Z: 0.03 from right edge.

Top View (Right):

- Overall width: 4.3 ± 0.1
- Overall height: 3.8 ± 0.1
- Pin 1 location: 0.4 ± 0.1 from bottom left corner.
- Pin 5 location: 0.4 ± 0.1 from bottom edge.
- Pin 8 location: 0.4 ± 0.1 from bottom edge.
- Pin 4 location: 0.4 ± 0.1 from bottom edge.
- Pin 127 location: 1.27 from bottom edge.
- Feature A: 0.25 ± 0.1 from bottom edge.
- Feature B: 0.03 from bottom edge.
- Feature C: 0.03 from bottom edge.
- Feature D: 0.03 from bottom edge.
- Feature E: 0.03 from bottom edge.
- Feature F: 0.03 from bottom edge.
- Feature G: 0.03 from bottom edge.
- Feature H: 0.03 from bottom edge.
- Feature I: 0.03 from bottom edge.
- Feature J: 0.03 from bottom edge.
- Feature K: 0.03 from bottom edge.
- Feature L: 0.03 from bottom edge.
- Feature M: 0.03 from bottom edge.
- Feature N: 0.03 from bottom edge.
- Feature O: 0.03 from bottom edge.
- Feature P: 0.03 from bottom edge.
- Feature Q: 0.03 from bottom edge.
- Feature R: 0.03 from bottom edge.
- Feature S: 0.03 from bottom edge.
- Feature T: 0.03 from bottom edge.
- Feature U: 0.03 from bottom edge.
- Feature V: 0.03 from bottom edge.
- Feature W: 0.03 from bottom edge.
- Feature X: 0.03 from bottom edge.
- Feature Y: 0.03 from bottom edge.
- Feature Z: 0.03 from bottom edge.

-
- Figure 1 shows the dimensions of the PCB layout. The top view (a) includes dimensions for the copper, solder mask, and stencil apertures. The bottom view (b) includes dimensions for the solder mask and stencil apertures. The legend indicates: copper (solid grey), solder mask (white with diagonal lines), and stencil apertures (hatched).

PIN 1 INDEX MARKING

8

4

6.9

12

5.5

0.3

1.3

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Revision History

Version	Date	Changes
Revision 1.0	23.07.2019	Final Data Sheet