



PMCA14UN

12 V, N-channel Trench MOSFET

6 August 2020

Product data sheet

1. General description

N-channel enhancement mode Field-Effect Transistor (FET) in a leadless ultra small DSN1010-3 (SOT8007) Surface-Mounted Device (SMD) package using Trench MOSFET technology.

2. Features and benefits

- Low threshold voltage
- Very fast switching
- Ultra small package: $0.96 \times 0.96 \times 0.24$ mm
- Trench MOSFET technology

3. Applications

- Relay driver
- Battery management
- Low-side load switch
- Switching circuits

4. Quick reference data

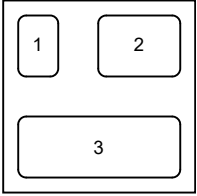
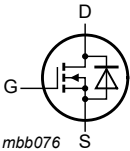
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j = 25\text{ }^{\circ}\text{C}$	-	-	12	V
V_{GS}	gate-source voltage		-8	-	8	V
I_D	drain current	$V_{GS} = 4.5\text{ V}; T_{amb} = 25\text{ }^{\circ}\text{C}; t \leq 5\text{ s}$	[1]	-	14	A
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5\text{ V}; I_D = 5\text{ A}; T_j = 25\text{ }^{\circ}\text{C}$	-	13.2	16	m Ω

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), 4 layer copper, tin-plated and mounting pad for drain 6 cm^2 .

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 Transparent top view DSN1010-3 (SOT8007)	 <i>mbb076</i>
2	D	drain		
3	S	source		

6. Ordering information

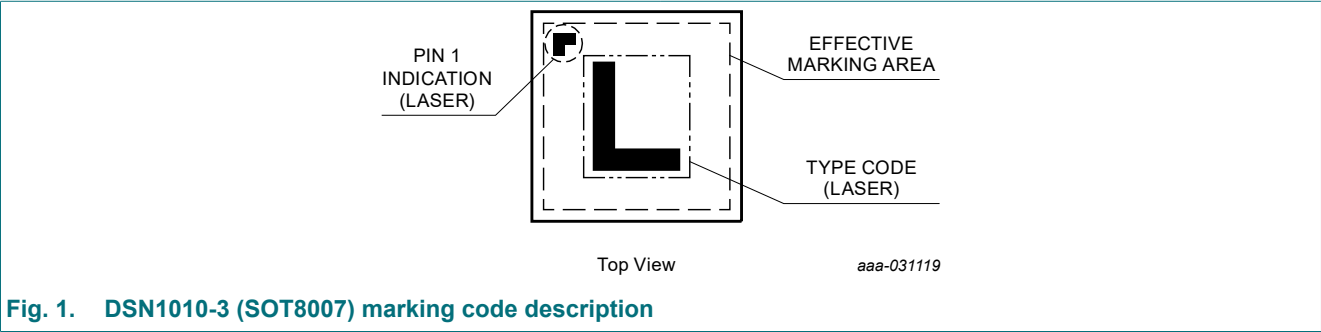
Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMCA14UN	DSN1010-3	chip-scale package; 3 terminals; body 0.96 x 0.96 x 0.24 mm	SOT8007

7. Marking

Table 4. Marking codes

Type number	Marking code
PMCA14UN	L



8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{DS}	drain-source voltage	T _j = 25 °C		-	12	V
V _{GS}	gate-source voltage			-8	8	V
I _D	drain current	V _{GS} = 4.5 V; T _{amb} = 25 °C; t ≤ 5 s	[1]	-	14	A
		V _{GS} = 4.5 V; T _{amb} = 25 °C	[1]	-	11	A
		V _{GS} = 4.5 V; T _{amb} = 100 °C	[1]	-	7	A
I _{DM}	peak drain current	T _{amb} = 25 °C; single pulse; t _p ≤ 10 μs		-	44	A
P _{tot}	total power dissipation	T _{amb} = 25 °C	[2]	-	1.2	W
			[1]	-	2.5	W
		T _{amb} = 25 °C; t ≤ 5 s	[1]	-	3.9	W
		T _{sp} = 25 °C		-	31	W
T _j	junction temperature			-55	150	°C
T _{amb}	ambient temperature			-55	150	°C
T _{stg}	storage temperature			-65	150	°C
Source-drain diode						
I _S	source current	T _{amb} = 25 °C	[1]	-	1.2	A

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), 4 layer copper, tin-plated and mounting pad for drain 6 cm².

[2] Device mounted on an FR4 Printed-Circuit Board (PCB), 4 layer copper, tin-plated and standard footprint.

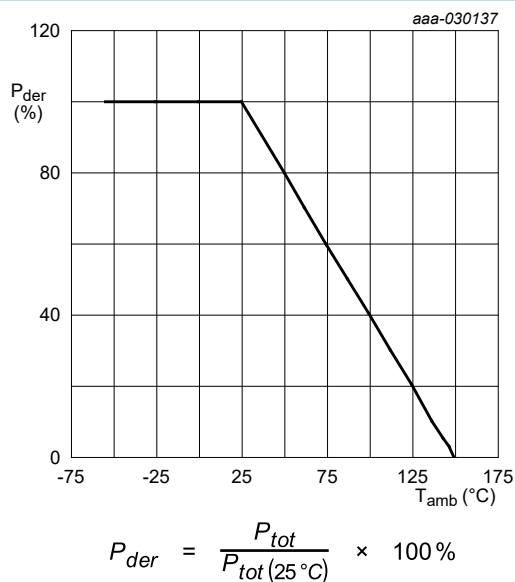


Fig. 2. Normalized total power dissipation as a function of ambient temperature

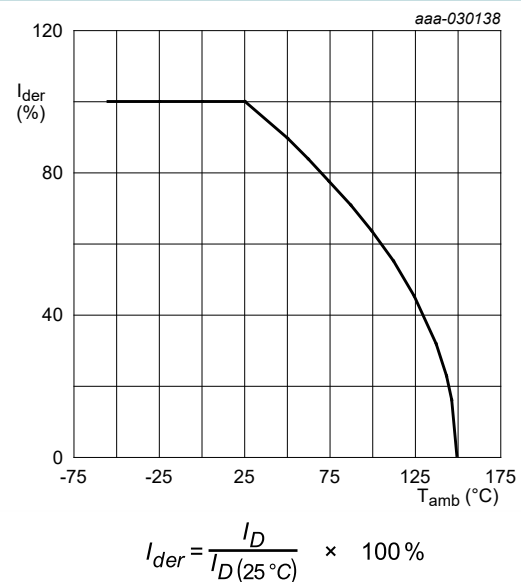
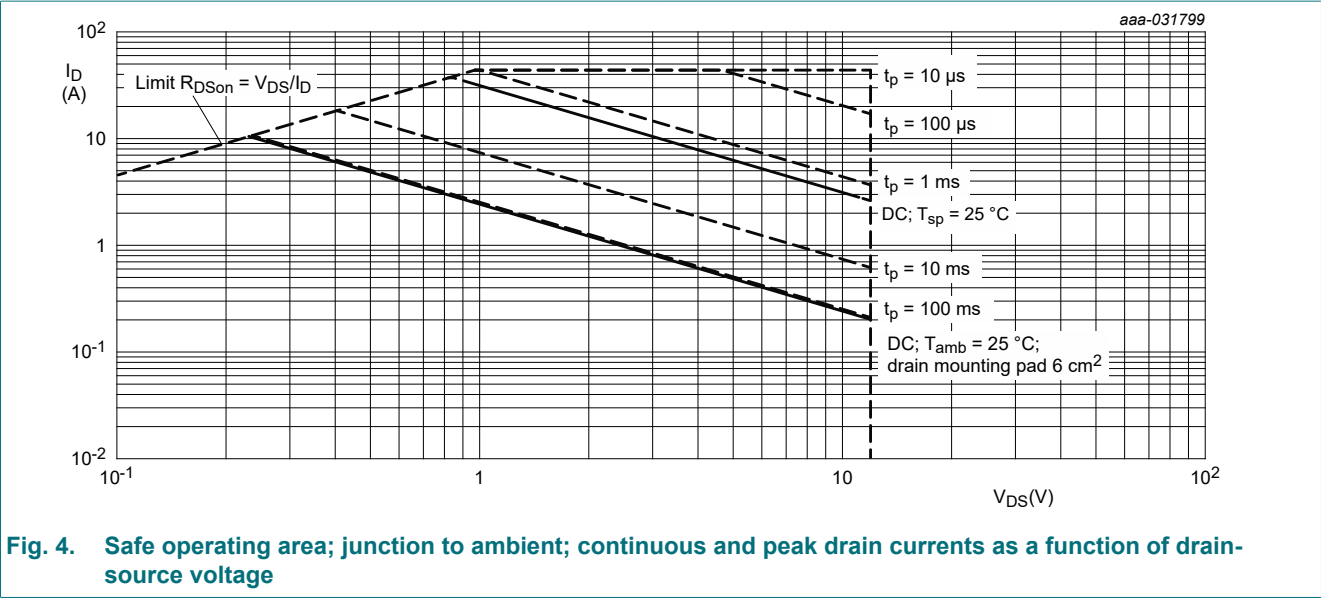


Fig. 3. Normalized continuous drain current as a function of ambient temperature



9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	92	106	K/W
			[2]	-	43	50	K/W
		in free air; $t \leq 5$ s	[2]	-	28	32	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	2	4	K/W

- [1] Device mounted on an FR4 Printed-Circuit Board (PCB), 4 layer copper, tin-plated and standard footprint.
[2] Device mounted on an FR4 Printed-Circuit Board (PCB), 4 layer copper, tin-plated and mounting pad for drain 6 cm².

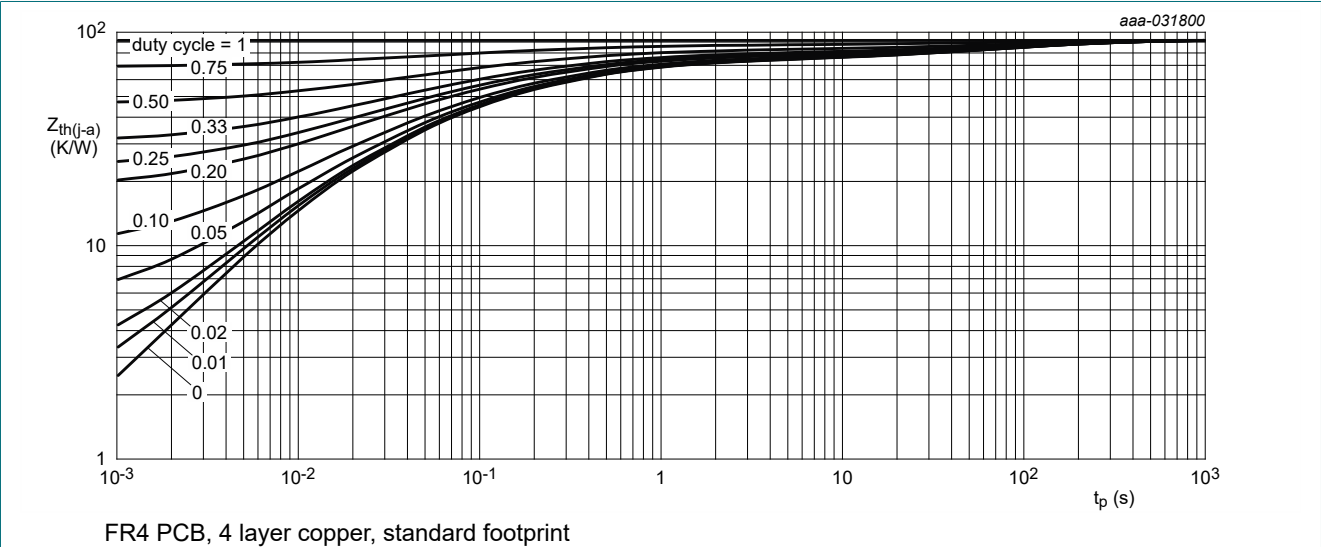


Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

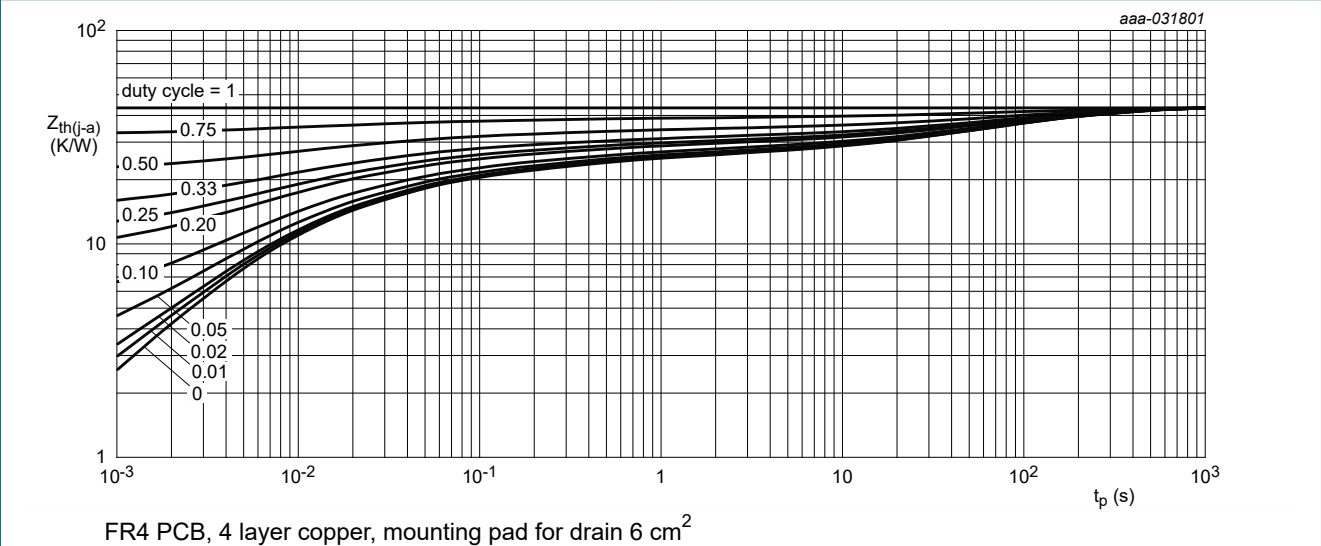


Fig. 6. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 250 μA; V _{GS} = 0 V; T _j = 25 °C		12	-	-	V
V _{GSth}	gate-source threshold voltage	I _D = 250 μA; V _{DS} =V _{GS} ; T _j = 25 °C		0.4	0.6	0.9	V
I _{DSS}	drain leakage current	V _{DS} = 9.6 V; V _{GS} = 0 V; T _j = 25 °C		-	-	1	μA
I _{GSS}	gate leakage current	V _{GS} = 8 V; V _{DS} = 0 V; T _j = 25 °C		-	-	100	nA
		V _{GS} = -8 V; V _{DS} = 0 V; T _j = 25 °C		-	-	-100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 4.5 V; I _D = 5 A; T _j = 25 °C		-	13.2	16	mΩ
		V _{GS} = 4.5 V; I _D = 5 A; T _j = 150 °C		-	17	21	mΩ
		V _{GS} = 3.3 V; I _D = 5 A; T _j = 25 °C		-	14.2	17	mΩ
		V _{GS} = 2.5 V; I _D = 5 A; T _j = 25 °C		-	16	21	mΩ
		V _{GS} = 1.8 V; I _D = 1 A; T _j = 25 °C		-	22	35	mΩ
g _{fs}	forward transconductance	V _{DS} = 6 V; I _D = 1 A; T _j = 25 °C		-	5.6	-	S
R _G	gate resistance	f = 1 MHz		-	1.5	-	Ω
Dynamic characteristics							
Q _{G(tot)}	total gate charge	V _{DS} = 6 V; I _D = 5 A; V _{GS} = 3.3 V; T _j = 25 °C		-	8	12	nC
Q _{GS}	gate-source charge			-	1.3	-	nC
Q _{GD}	gate-drain charge			-	3.2	-	nC
C _{iss}	input capacitance	V _{DS} = 6 V; f = 1 MHz; V _{GS} = 0 V; T _j = 25 °C		-	855	-	pF
C _{oss}	output capacitance			-	257	-	pF
C _{rss}	reverse transfer capacitance			-	237	-	pF
t _{d(on)}	turn-on delay time	V _{DS} = 6 V; I _D = 5 A; V _{GS} = 3.3 V; R _{G(ext)} = 6 Ω; T _j = 25 °C		-	3	-	ns
t _r	rise time			-	6	-	ns
t _{d(off)}	turn-off delay time			-	16	-	ns
t _f	fall time			-	11	-	ns
Source-drain diode							
V _{SD}	source-drain voltage	I _S = 1.2 A; V _{GS} = 0 V; T _j = 25 °C		-	0.7	1.2	V

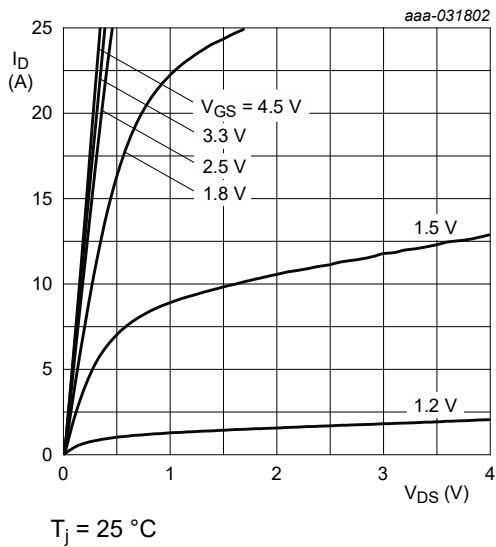


Fig. 7. Output characteristics: drain current as a function of drain-source voltage; typical values

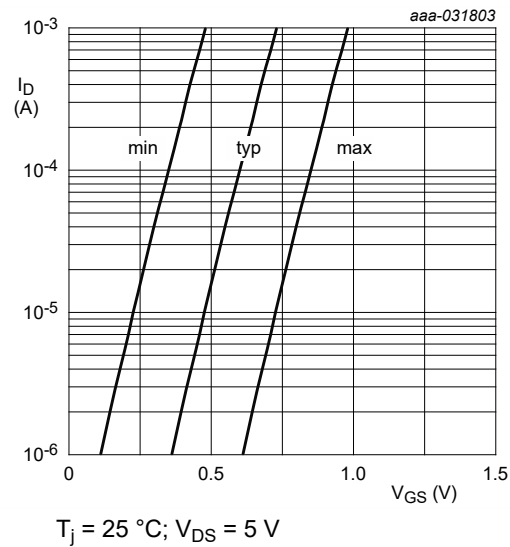


Fig. 8. Subthreshold drain current as a function of gate-source voltage

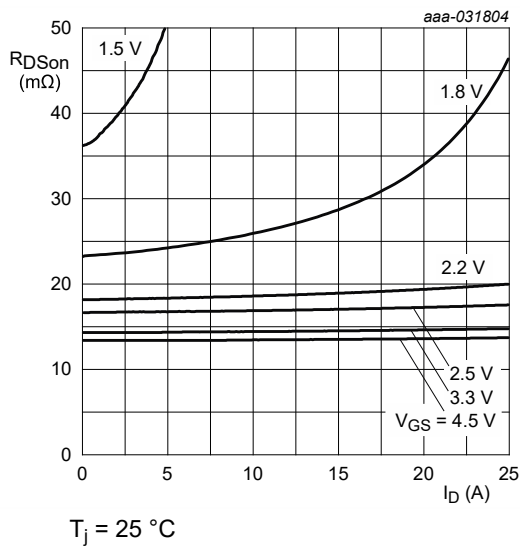


Fig. 9. Drain-source on-state resistance as a function of drain current; typical values

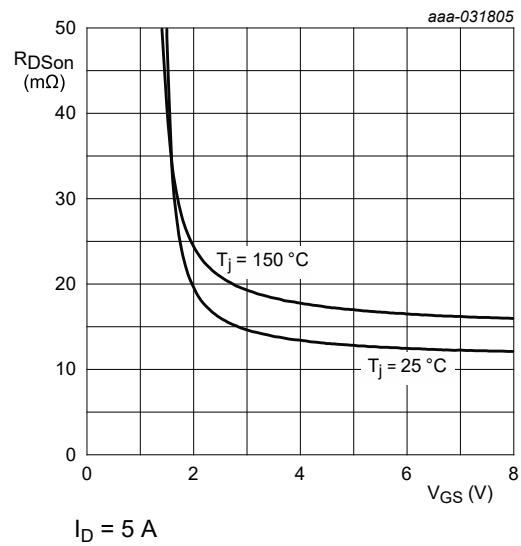


Fig. 10. Drain-source on-state resistance as a function of gate-source voltage; typical values

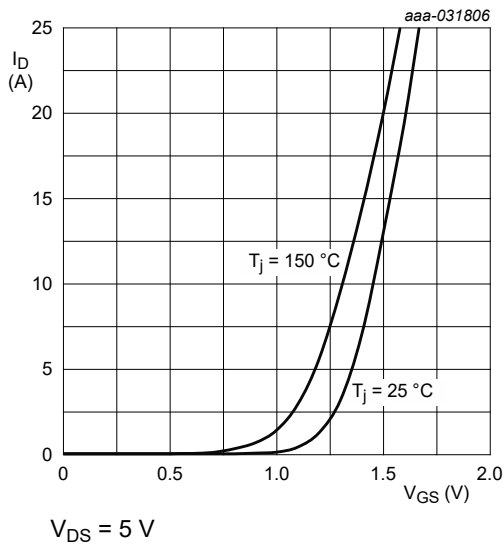


Fig. 11. Transfer characteristics: drain current as a function of gate-source voltage; typical values

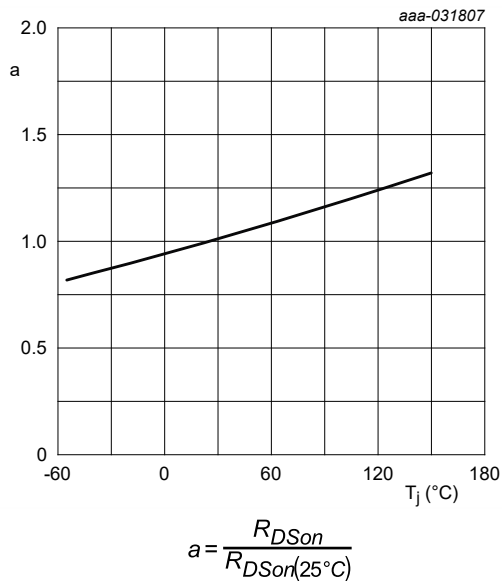


Fig. 12. Normalized drain-source on-state resistance as a function of junction temperature; typical values

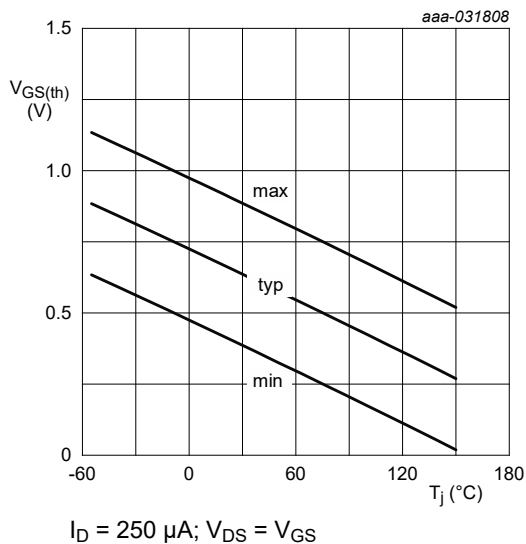


Fig. 13. Gate-source threshold voltage as a function of junction temperature

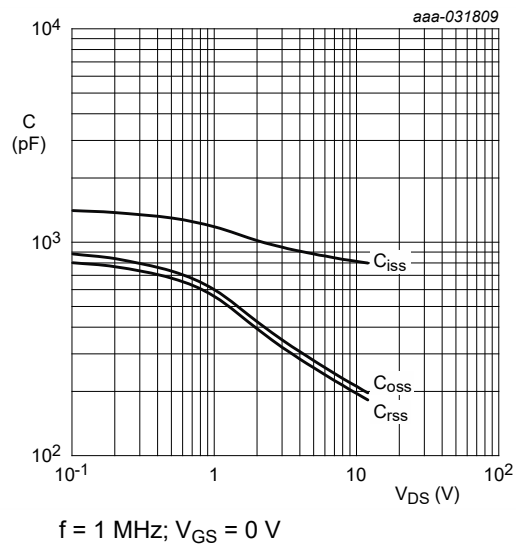


Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

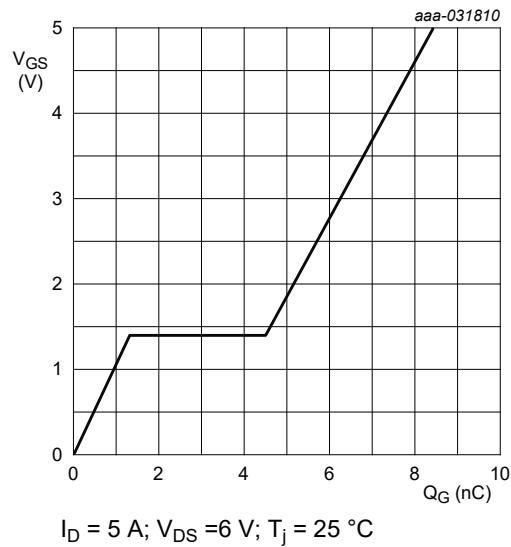


Fig. 15. Gate-source voltage as a function of gate charge; typical values

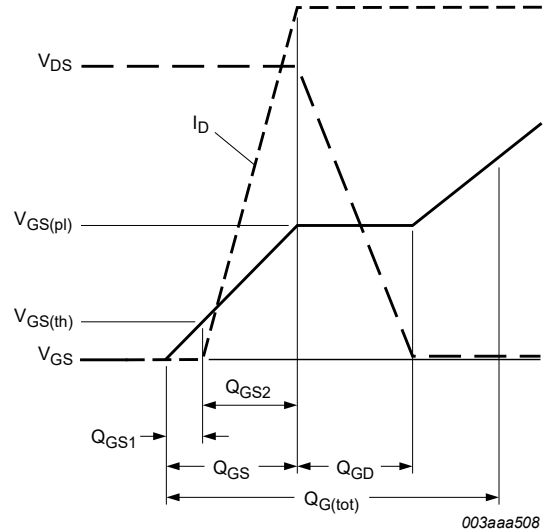


Fig. 16. Gate charge waveform definitions

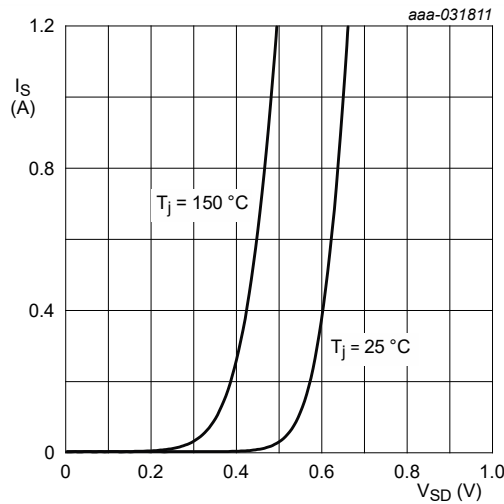


Fig. 17. Source current as a function of source-drain voltage; typical values

11. Test information

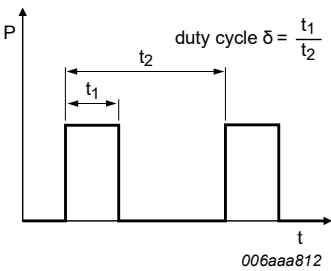


Fig. 18. Duty cycle definition

12. Package outline

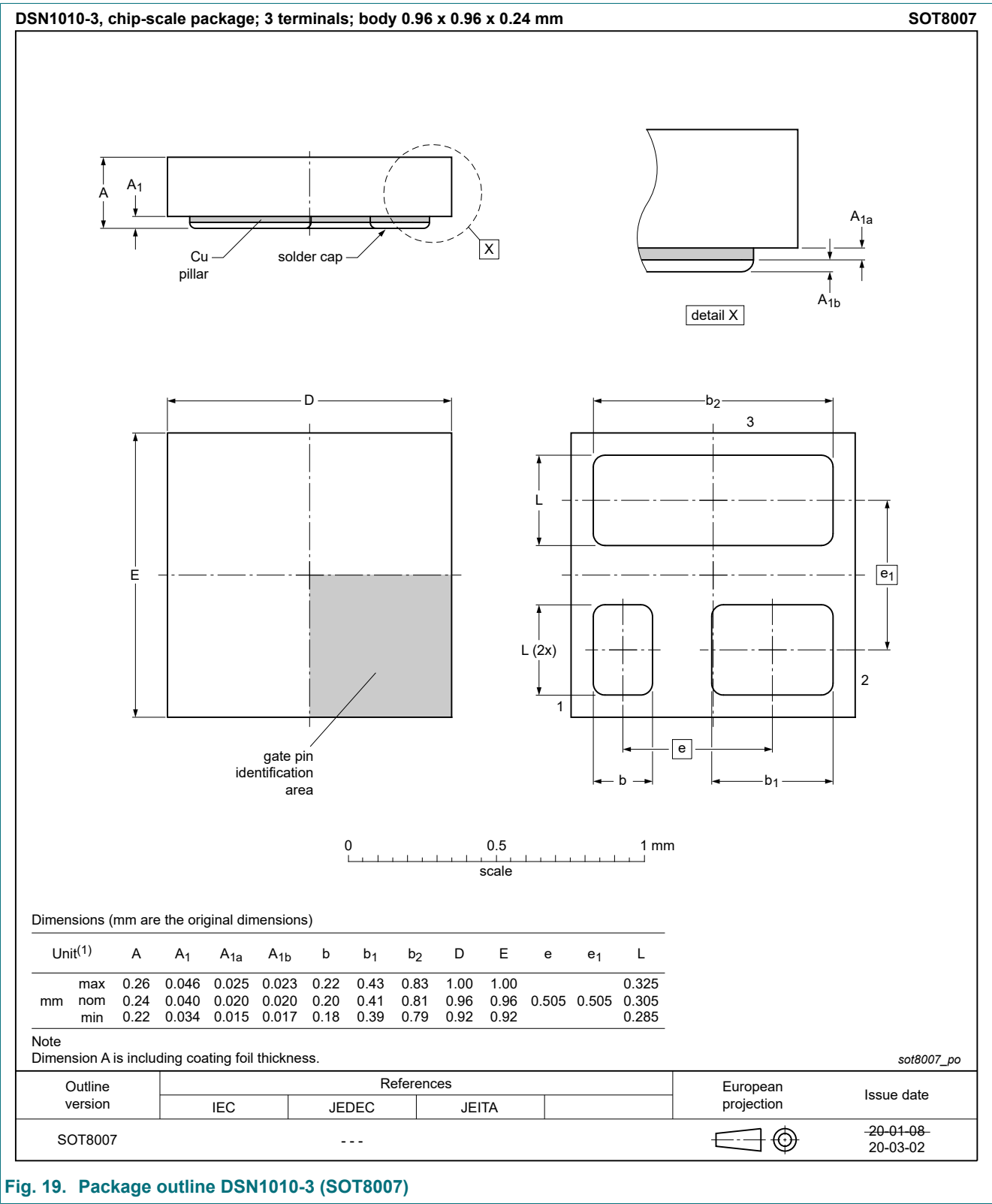


Fig. 19. Package outline DSN1010-3 (SOT8007)

13. Soldering

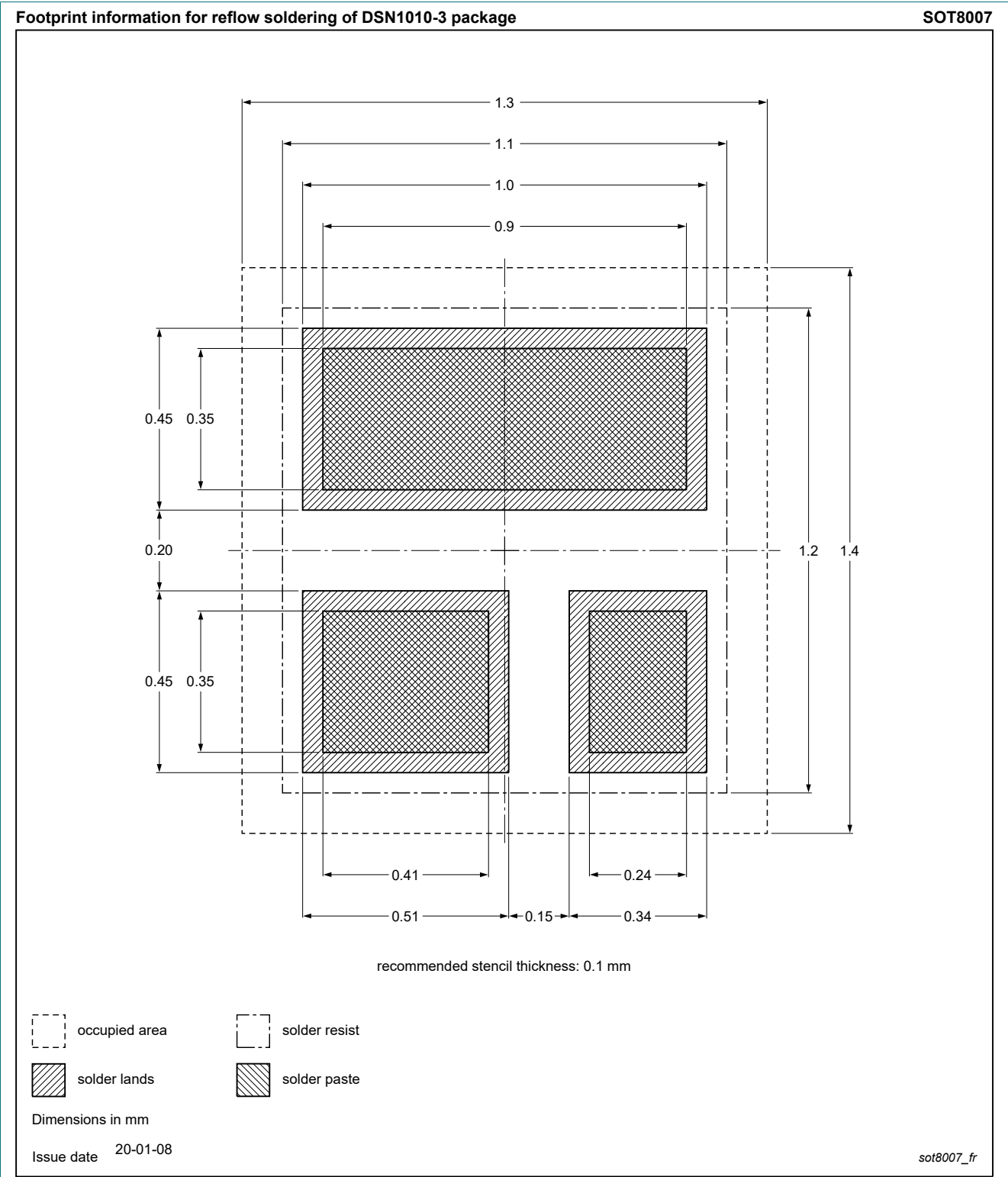


Fig. 20. Reflow soldering footprint for DSN1010-3 (SOT8007)

14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMCA14UN v.1	20200806	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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