

PHB47NQ10T

N-channel TrenchMOS standard level FET

Rev. 02 — 25 February 2010

Product data sheet

1. Product profile

1.1 General description

Standard level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

1.2 Features and benefits

- Low conduction losses due to low on-state resistance
- Suitable for high frequency applications due to fast switching characteristics

1.3 Applications

- DC-to-DC convertors
- Switched-mode power supplies

1.4 Quick reference data

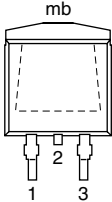
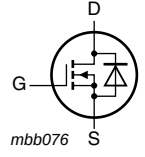
Table 1. Quick reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$	-	-	100	V
I_D	drain current	$T_{mb} = 25\text{ °C}$; $V_{GS} = 10\text{ V}$; see Figure 1 and 2	-	-	47	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; see Figure 3	-	-	166	W
Dynamic characteristics						
Q_{GD}	gate-drain charge	$V_{GS} = 10\text{ V}$; $I_D = 40\text{ A}$; $V_{DS} = 80\text{ V}$; $T_j = 25\text{ °C}$; see Figure 13	-	21	-	nC
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; $T_j = 25\text{ °C}$; see Figure 11 and 12	-	20	28	mΩ



2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 SOT404 (D2PAK)	
2	D	drain ^[1]		
3	S	source		
mb	D	mounting base; connected to drain		

[1] It is not possible to make a connection to pin 2.

3. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
PHB47NQ10T	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

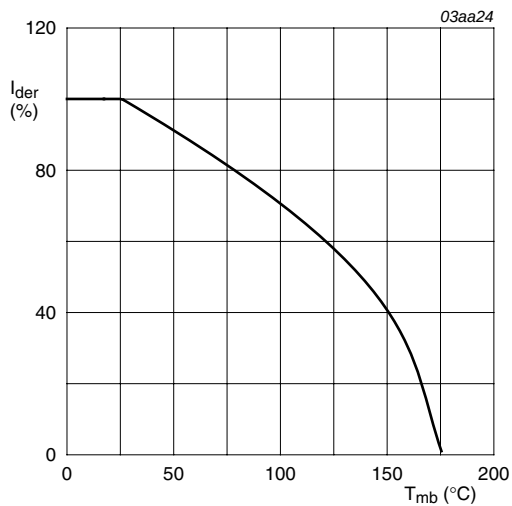
Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ }^{\circ}\text{C}$; $T_j \leq 175\text{ }^{\circ}\text{C}$	-	100	V
V_{DGR}	drain-gate voltage	$T_j \geq 25\text{ }^{\circ}\text{C}$; $T_j \leq 175\text{ }^{\circ}\text{C}$; $R_{GS} = 20\text{ k}\Omega$	-	100	V
V_{GS}	gate-source voltage		-20	20	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 100\text{ }^{\circ}\text{C}$; see Figure 1	-	33	A
		$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ }^{\circ}\text{C}$; see Figure 1 and 2	-	47	A
I_{DM}	peak drain current	$t_p \leq 10\text{ }\mu\text{s}$; pulsed; $T_{mb} = 25\text{ }^{\circ}\text{C}$; see Figure 2	-	187	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ }^{\circ}\text{C}$; see Figure 3	-	166	W
T_{stg}	storage temperature		-55	175	$^{\circ}\text{C}$
T_j	junction temperature		-55	175	$^{\circ}\text{C}$

Source-drain diode

I_S	source current	$T_{mb} = 25\text{ }^{\circ}\text{C}$	-	47	A
I_{SM}	peak source current	$t_p \leq 10\text{ }\mu\text{s}$; pulsed; $T_{mb} = 25\text{ }^{\circ}\text{C}$	-	187	A

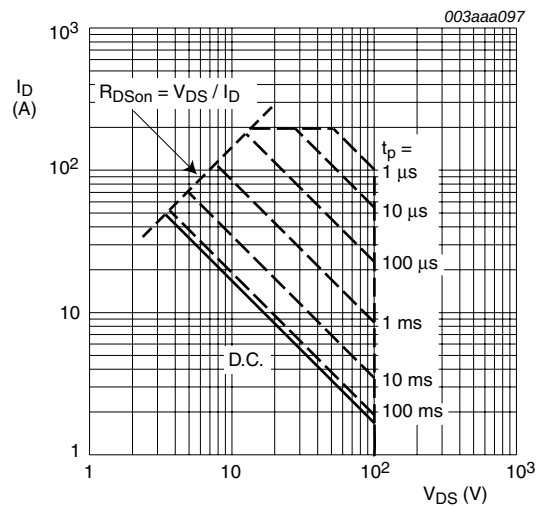
Avalanche ruggedness

$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 5\text{ V}$; $T_{j(\text{init})} = 25\text{ }^{\circ}\text{C}$; $I_D = 30\text{ A}$; $V_{sup} \leq 25\text{ V}$; unclamped; $t_p = 0.1\text{ ms}$; $R_{GS} = 50\text{ }\Omega$; see Figure 4	-	45	mJ
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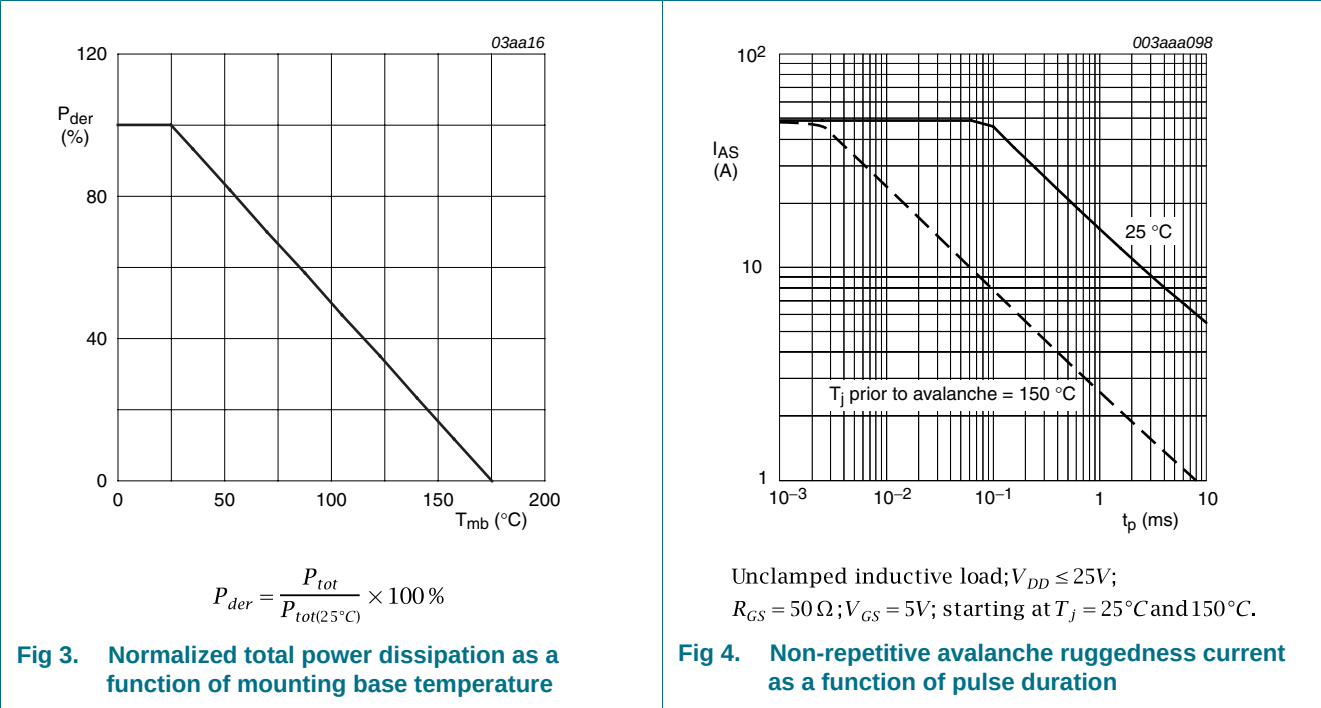
$$I_{der} = \frac{I_D}{I_{D(25^{\circ}\text{C})}} \times 100\%$$

Fig 1. Normalized continuous drain current as a function of mounting base temperature



$T_{mb} = 25^{\circ}\text{C}$; I_{DM} is single pulse

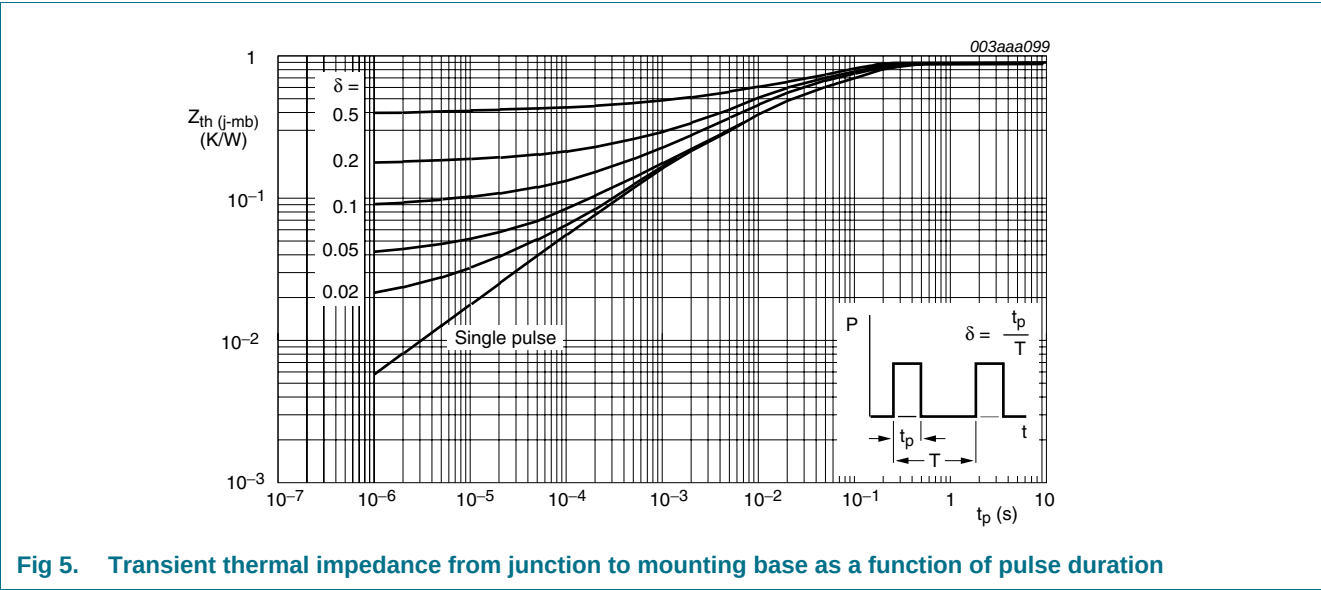
Fig 2. Safe operating area; continuous and peak drain currents as a function of drain-source voltage



5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R _{th(j-mb)}	thermal resistance from junction to mounting base	see Figure 5	-	-	0.9	K/W
R _{th(j-a)}	thermal resistance from junction to ambient	mounted on printed-circuit board; minimum footprint	-	50	-	K/W



6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 250 μA; V _{GS} = 0 V; T _j = 25 °C	100	-	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} = V _{GS} ; T _j = 175 °C; see Figure 10	1	-	-	V
		I _D = 1 mA; V _{DS} = V _{GS} ; T _j = 25 °C; see Figure 10	2	3	4	V
I _{DSS}	drain leakage current	V _{DS} = 100 V; V _{GS} = 0 V; T _j = 25 °C	-	0.05	10	μA
		V _{DS} = 100 V; V _{GS} = 0 V; T _j = 175 °C	-	-	500	μA
I _{GSS}	gate leakage current	V _{GS} = 20 V; V _{DS} = 0 V; T _j = 25 °C	-	2	100	nA
		V _{GS} = -20 V; V _{DS} = 0 V; T _j = 25 °C	-	2	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 25 A; T _j = 175 °C; see Figure 11 and 12	-	-	76	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _j = 25 °C; see Figure 11 and 12	-	20	28	mΩ
Dynamic characteristics						
Q _{G(tot)}	total gate charge	I _D = 40 A; V _{DS} = 80 V; V _{GS} = 10 V; T _j = 25 °C; see Figure 13	-	66	-	nC
Q _{GS}	gate-source charge		-	12	-	nC
Q _{GD}	gate-drain charge		-	21	-	nC
C _{iss}	input capacitance	V _{DS} = 25 V; V _{GS} = 0 V; f = 1 MHz; T _j = 25 °C; see Figure 14	-	2320	3100	pF
C _{oss}	output capacitance		-	315	378	pF
C _{rss}	reverse transfer capacitance		-	187	256	pF
t _{d(on)}	turn-on delay time	V _{DS} = 30 V; R _L = 1.2 Ω; V _{GS} = 10 V; R _{G(ext)} = 10 Ω; T _j = 25 °C	-	15	23	ns
t _r	rise time		-	70	105	ns
t _{d(off)}	turn-off delay time		-	83	116	ns
t _f	fall time		-	45	63	ns
Source-drain diode						
V _{SD}	source-drain voltage	I _S = 25 A; V _{GS} = 0 V; T _j = 25 °C; see Figure 15	-	0.85	1.2	V
t _{rr}	reverse recovery time	I _S = 47 A; dI _S /dt = -100 A/μs; V _{GS} = -10 V; V _{DS} = 30 V; T _j = 25 °C	-	66	-	ns
Q _r	recovered charge		-	0.24	-	μC

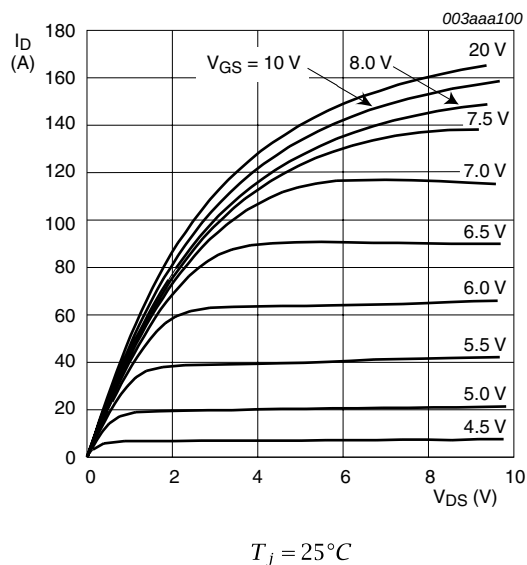


Fig 6. Output characteristics: drain current as a function of drain-source voltage; typical values

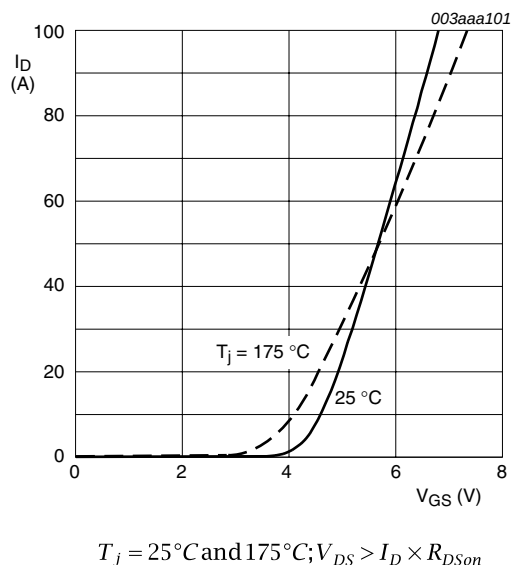


Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values

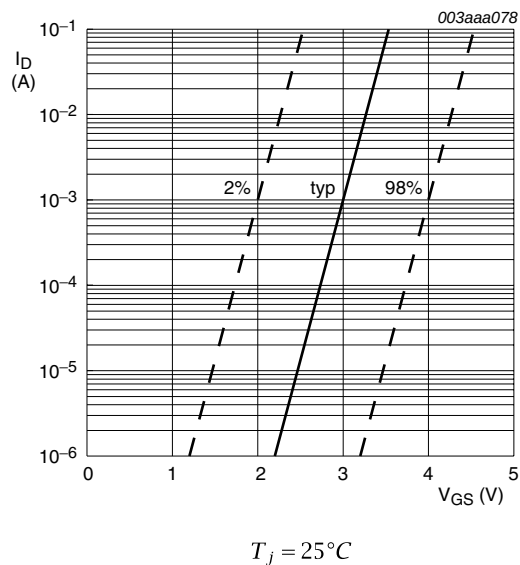


Fig 8. Sub-threshold drain current as a function of gate-source voltage

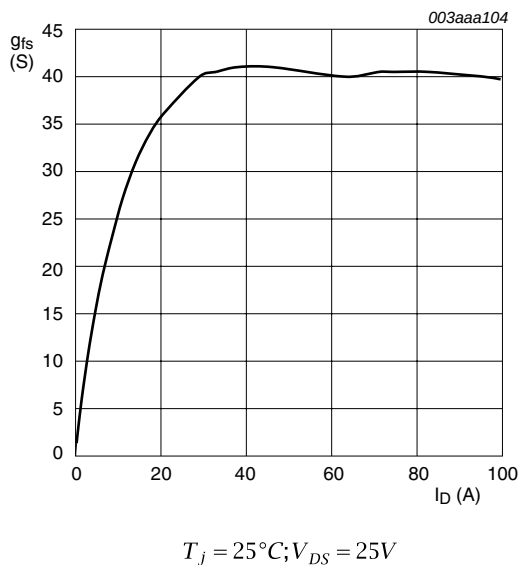


Fig 9. Forward transconductance as a function of drain current; typical values

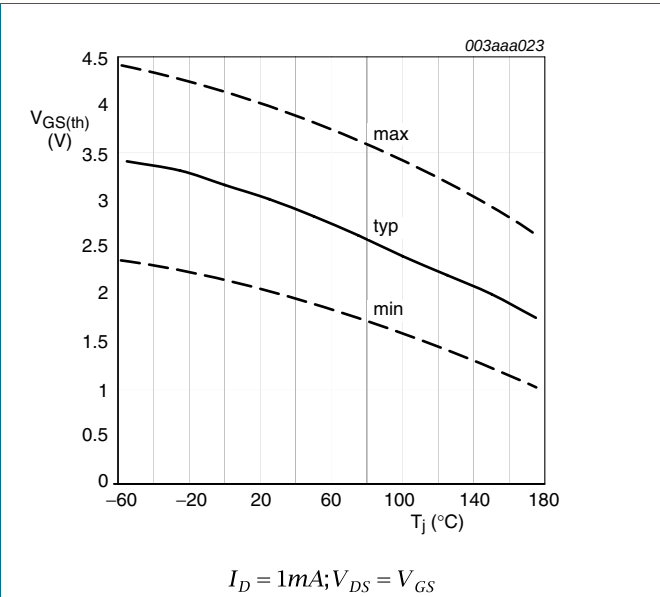


Fig 10. Gate-source threshold voltage as a function of junction temperature

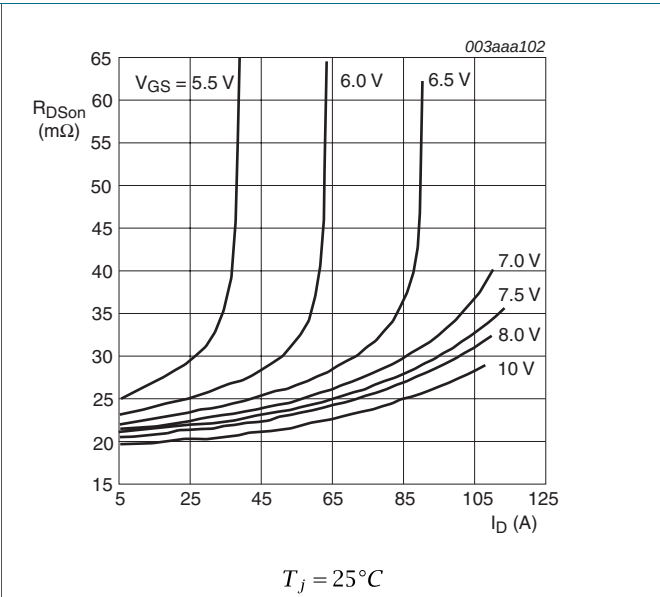


Fig 11. Drain-source on-state resistance as a function of drain current; typical values

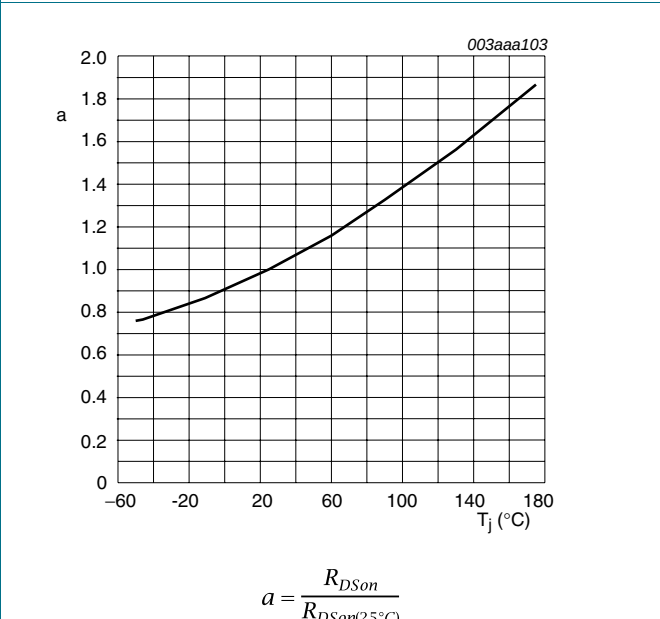


Fig 12. Normalized drain-source on-state resistance factor as a function of junction temperature

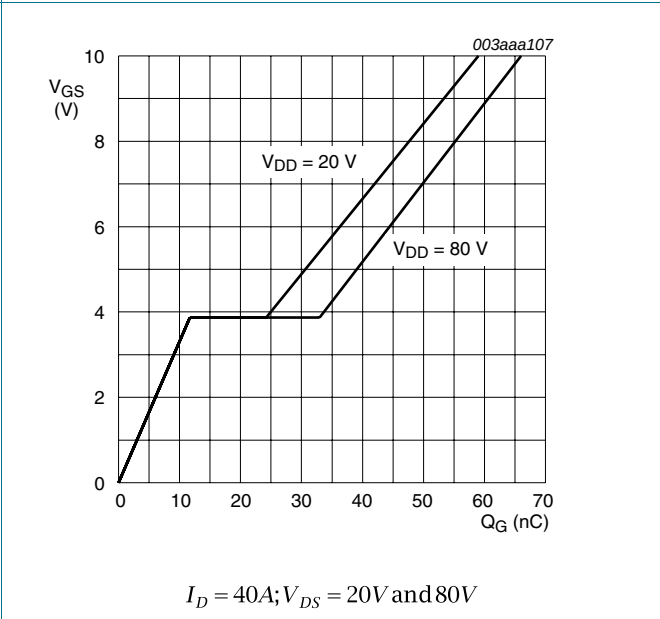
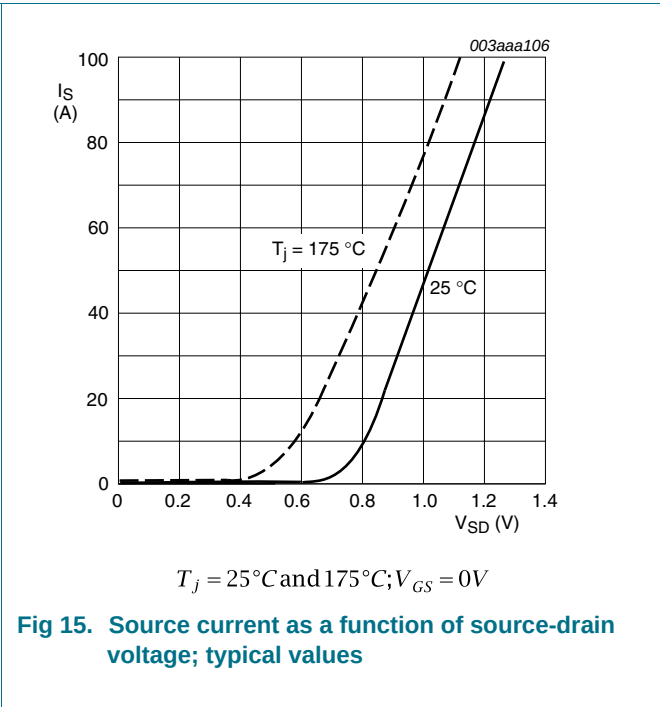
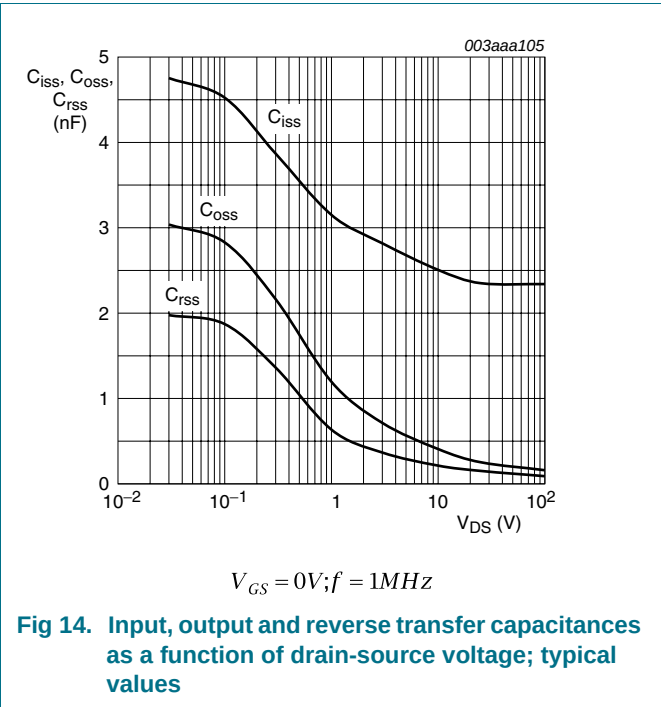


Fig 13. Gate-source voltage as a function of gate charge; typical values



7. Package outline

Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped) SOT404

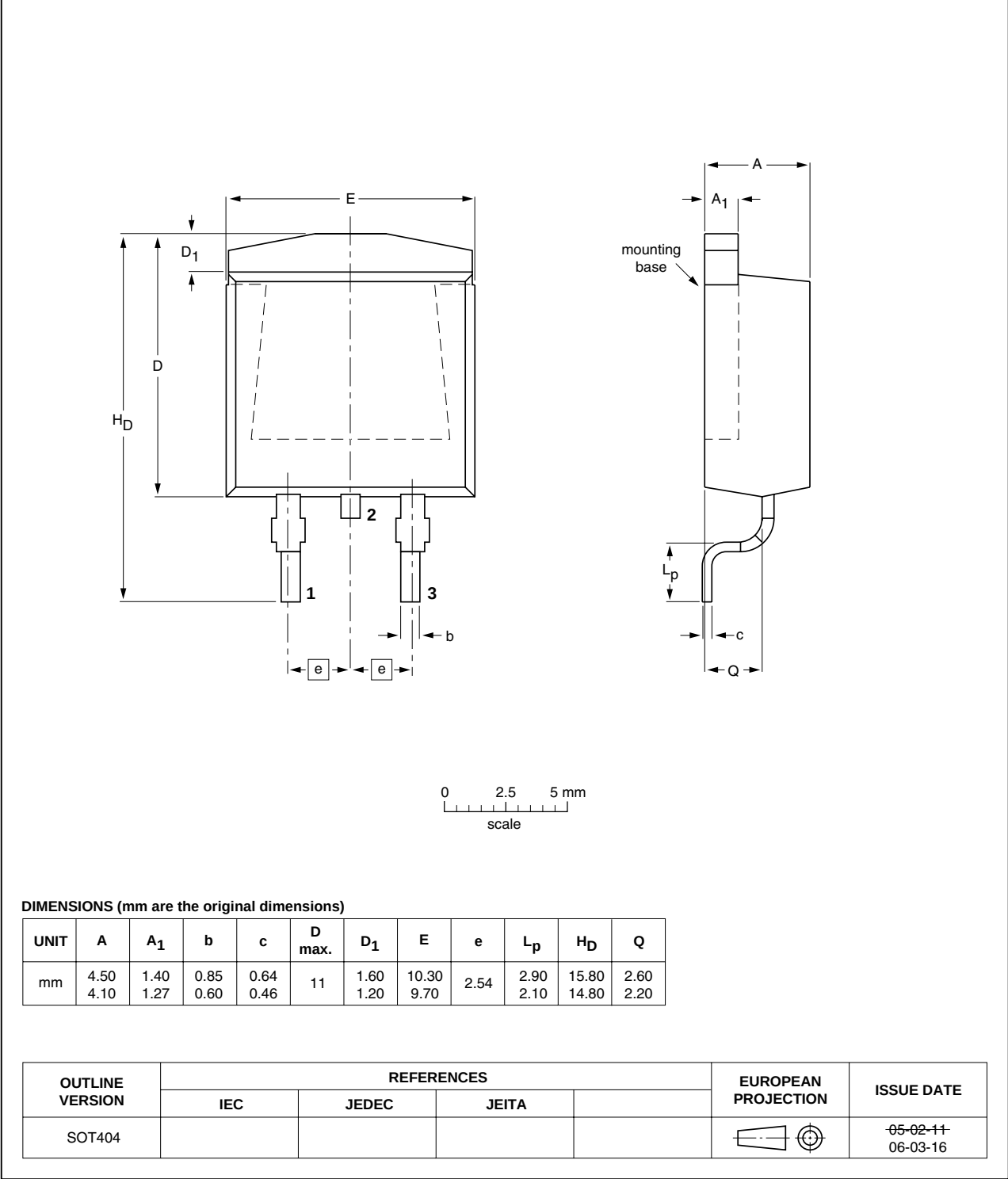


Fig 16. Package outline SOT404 (D2PAK)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PHB47NQ10T_2	20100225	Product data sheet	-	PHP_PHB_47NQ10T-01
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate.			
PHP_PHB_47NQ10T-01 (9397 750 08243)	20010516	Product data	-	-

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9.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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