



BUK9624-55A

N-channel TrenchMOS logic level FET

Rev. 02 — 31 January 2011

Product data sheet

1. Product profile

1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in automotive critical applications.

1.2 Features and benefits

- AEC Q101 compliant
- Low conduction losses due to low on-state resistance
- Suitable for logic level gate drive sources
- Suitable for thermally demanding environments due to 175 °C rating

1.3 Applications

- 12 V and 24 V loads
- Automotive and general purpose power switching
- Motors, lamps and solenoids

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 175\text{ °C}$	-	-	55	V
I_D	drain current	$V_{GS} = 5\text{ V}$; $T_{mb} = 25\text{ °C}$; see Figure 1 ; see Figure 3	-	-	46	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; see Figure 2	-	-	105	W

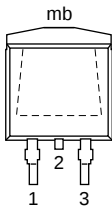
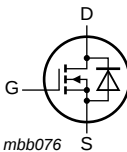


Table 1. Quick reference data ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
R _{DSon}	drain-source on-state resistance	V _{GS} = 4.5 V; I _D = 25 A; T _j = 25 °C	-	-	26	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _j = 25 °C	-	19	21.7	mΩ
		V _{GS} = 5 V; I _D = 25 A; T _j = 25 °C; see Figure 12 ; see Figure 13	-	20	24	mΩ
Avalanche ruggedness						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I _D = 46 A; V _{sup} ≤ 25 V; R _{GS} = 50 Ω; V _{GS} = 5 V; T _{j(init)} = 25 °C; unclamped	-	-	76	mJ

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	D	drain		
3	S	source		
mb	D	mounting base; connected to drain		

SOT404 (D2PAK)

3. Ordering information

Table 3. Ordering information

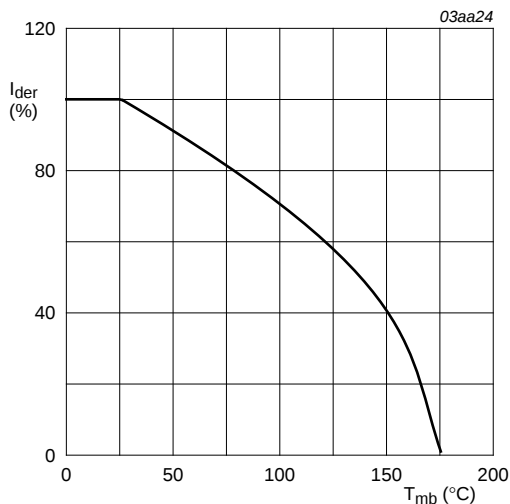
Type number	Package		
	Name	Description	Version
BUK9624-55A	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

4. Limiting values

Table 4. Limiting values

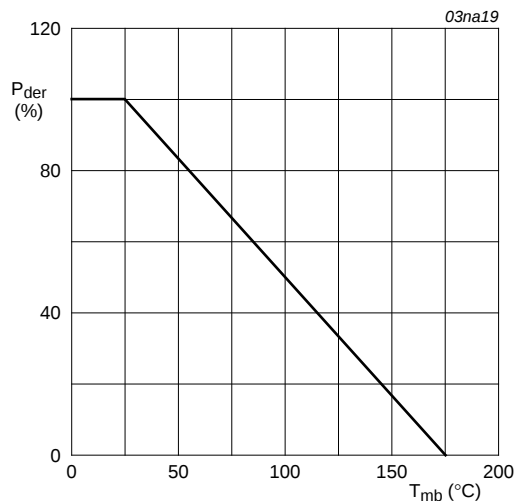
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ }^{\circ}\text{C}$; $T_j \leq 175\text{ }^{\circ}\text{C}$	-	55	V
V_{DGR}	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$	-	55	V
V_{GS}	gate-source voltage		-10	10	V
I_D	drain current	$T_{mb} = 25\text{ }^{\circ}\text{C}$; $V_{GS} = 5\text{ V}$; see Figure 1 ; see Figure 3	-	46	A
		$T_{mb} = 100\text{ }^{\circ}\text{C}$; $V_{GS} = 5\text{ V}$; see Figure 1	-	33	A
I_{DM}	peak drain current	$T_{mb} = 25\text{ }^{\circ}\text{C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$; see Figure 3	-	188	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ }^{\circ}\text{C}$; see Figure 2	-	105	W
T_{stg}	storage temperature		-55	175	$^{\circ}\text{C}$
T_j	junction temperature		-55	175	$^{\circ}\text{C}$
V_{GSM}	peak gate-source voltage	pulsed; $t_p \leq 50\text{ }\mu\text{s}$	-15	15	V
Source-drain diode					
I_S	source current	$T_{mb} = 25\text{ }^{\circ}\text{C}$	-	46	A
I_{SM}	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ }^{\circ}\text{C}$	-	188	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 46\text{ A}$; $V_{sup} \leq 25\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 5\text{ V}$; $T_{j(\text{init})} = 25\text{ }^{\circ}\text{C}$; unclamped	-	76	mJ



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}\text{C})}} \times 100\%$$

Fig 1. Normalized continuous drain current as a function of mounting base temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}\text{C})}} \times 100\%$$

Fig 2. Normalized total power dissipation as a function of mounting base temperature

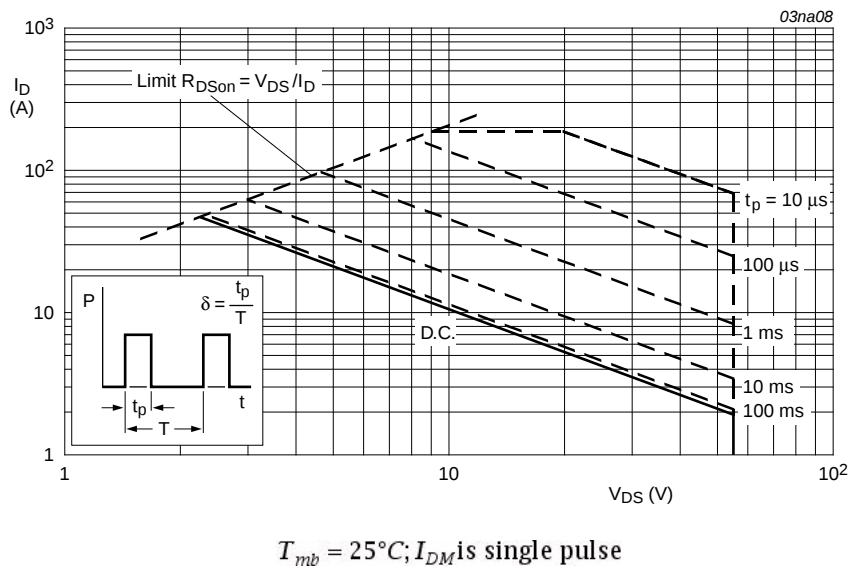


Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base		-	-	1.4	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	vertical in still air; lead length ≤ 5 mm; see Figure 4	-	50	-	K/W

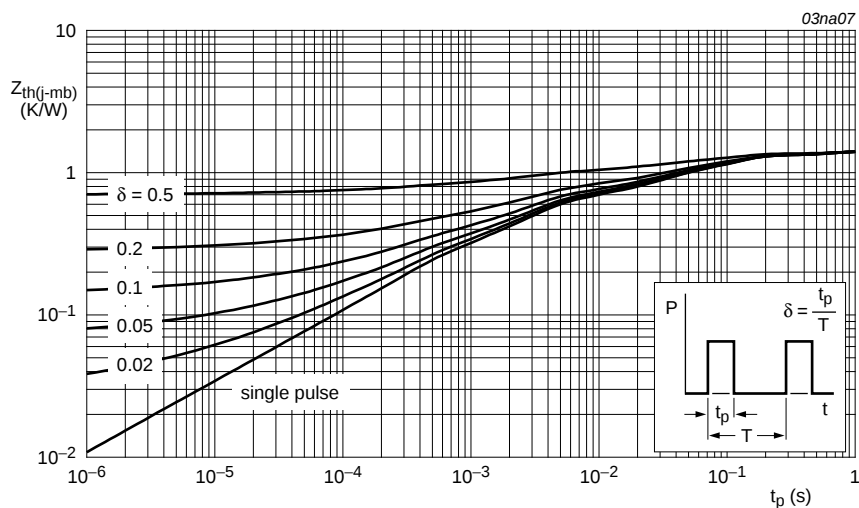


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 0.25 mA; V _{GS} = 0 V; T _j = -55 °C	50	-	-	V
		I _D = 0.25 mA; V _{GS} = 0 V; T _j = 25 °C	55	-	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} = V _{GS} ; T _j = 25 °C; see Figure 11	1	1.5	2	V
		I _D = 1 mA; V _{DS} = V _{GS} ; T _j = 175 °C; see Figure 11	0.5	-	-	V
		I _D = 1 mA; V _{DS} = V _{GS} ; T _j = -55 °C; see Figure 11	-	-	2.3	V
I _{DSS}	drain leakage current	V _{DS} = 55 V; V _{GS} = 0 V; T _j = 25 °C	-	0.05	10	μA
		V _{DS} = 55 V; V _{GS} = 0 V; T _j = 175 °C	-	-	500	μA
I _{GSS}	gate leakage current	V _{GS} = 10 V; V _{DS} = 0 V; T _j = 25 °C	-	2	100	nA
		V _{GS} = -10 V; V _{DS} = 0 V; T _j = 25 °C	-	2	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 5 V; I _D = 25 A; T _j = 175 °C; see Figure 12 ; see Figure 13	-	-	50	mΩ
		V _{GS} = 4.5 V; I _D = 25 A; T _j = 25 °C	-	-	26	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _j = 25 °C	-	19	21.7	mΩ
		V _{GS} = 5 V; I _D = 25 A; T _j = 25 °C; see Figure 12 ; see Figure 13	-	20	24	mΩ
Dynamic characteristics						
C _{iss}	input capacitance	V _{GS} = 0 V; V _{DS} = 25 V; f = 1 MHz;	-	1361	1815	pF
C _{oss}	output capacitance	T _j = 25 °C; see Figure 8	-	239	287	pF
C _{rss}	reverse transfer capacitance		-	162	222	pF
t _{d(on)}	turn-on delay time	V _{DS} = 30 V; R _L = 1.2 Ω; V _{GS} = 5 V;	-	17.5	-	ns
t _r	rise time	R _{G(ext)} = 10 Ω; T _j = 25 °C	-	104	-	ns
t _{d(off)}	turn-off delay time		-	82.5	-	ns
t _f	fall time		-	80	-	ns
L _D	internal drain inductance	from upper edge of drain mounting base to centre of die ; T _j = 25 °C	-	2.5	-	nH
		from drain lead 6 mm from package to centre of die ; T _j = 25 °C	-	4.5	-	nH
L _S	internal source inductance	from source lead to source bond pad ; T _j = 25 °C	-	7.5	-	nH
Source-drain diode						
V _{SD}	source-drain voltage	I _S = 25 A; V _{GS} = 0 V; T _j = 25 °C; see Figure 14	-	0.85	1.2	V
t _{rr}	reverse recovery time	I _S = 46 A; dI _S /dt = -100 A/μs;	-	50	-	ns
Q _r	recovered charge	V _{GS} = -10 V; V _{DS} = 30 V; T _j = 25 °C	-	85	-	nC

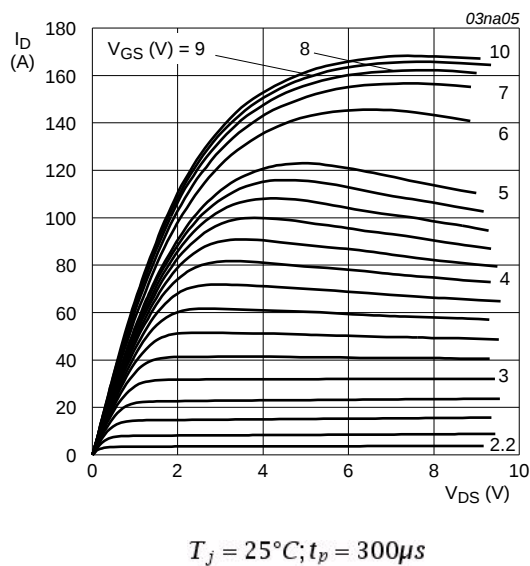


Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values

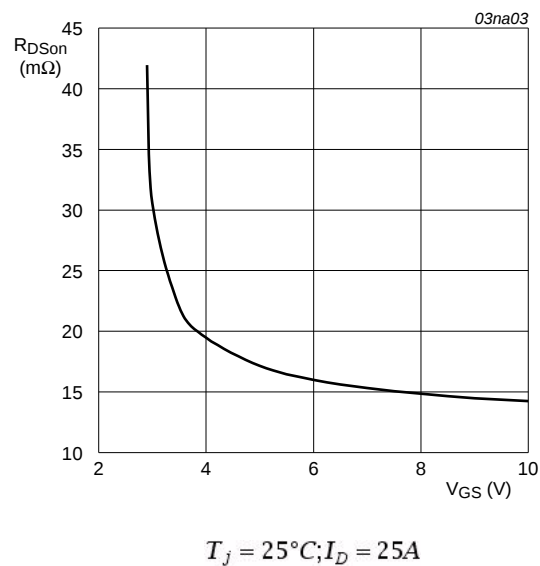


Fig 6. Drain-source on-state resistance as a function of gate-source voltage; typical values

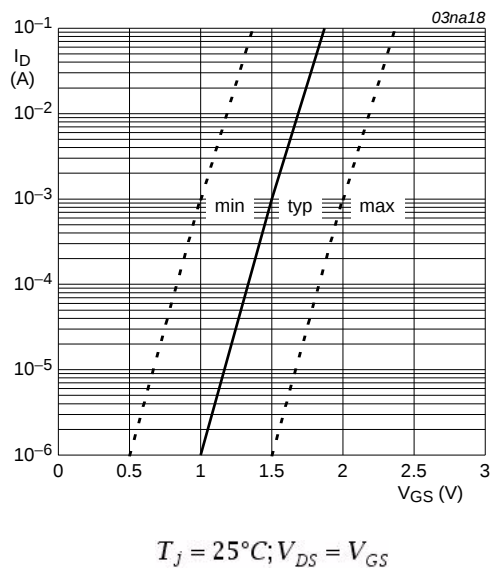


Fig 7. Sub-threshold drain current as a function of gate-source voltage

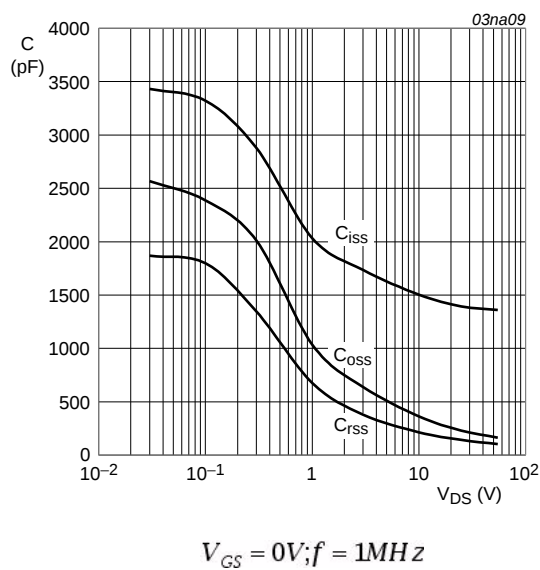


Fig 8. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

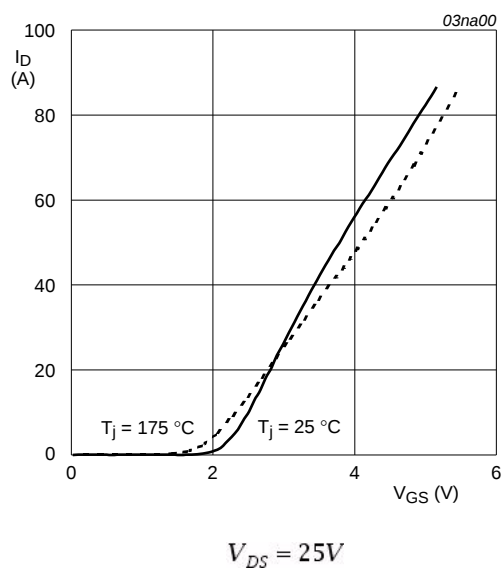


Fig 9. Transfer characteristics: drain current as a function of gate-source voltage; typical values

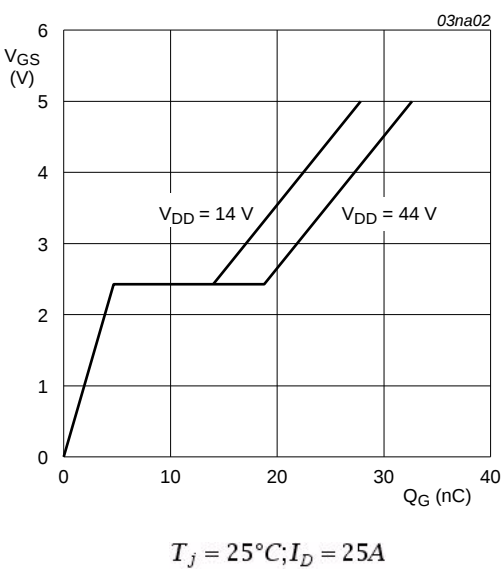


Fig 10. Gate-source voltage as a function of gate charge; typical values

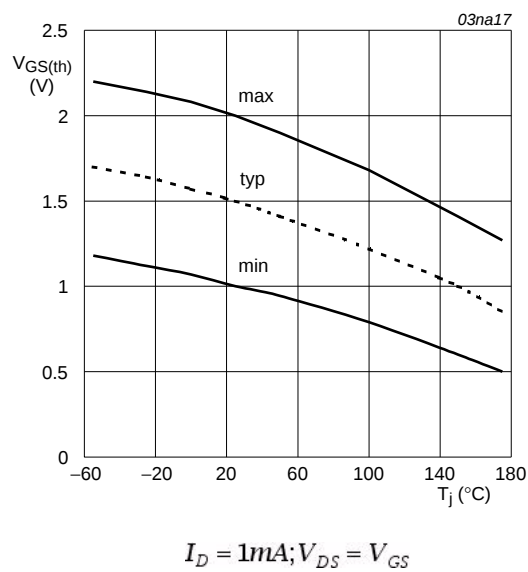


Fig 11. Gate-source threshold voltage as a function of junction temperature

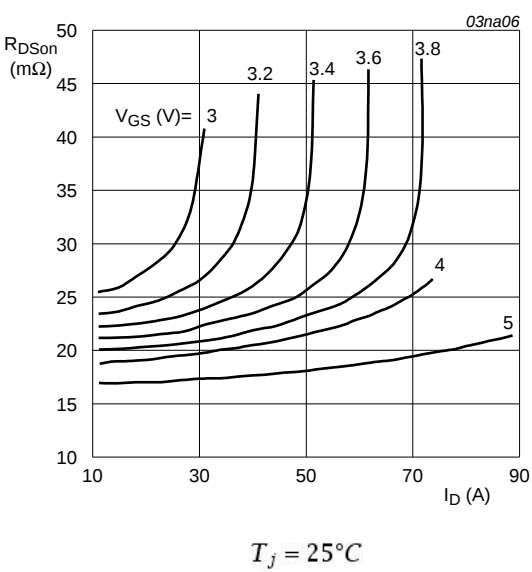


Fig 12. Drain-source on-state resistance as a function of drain current; typical values

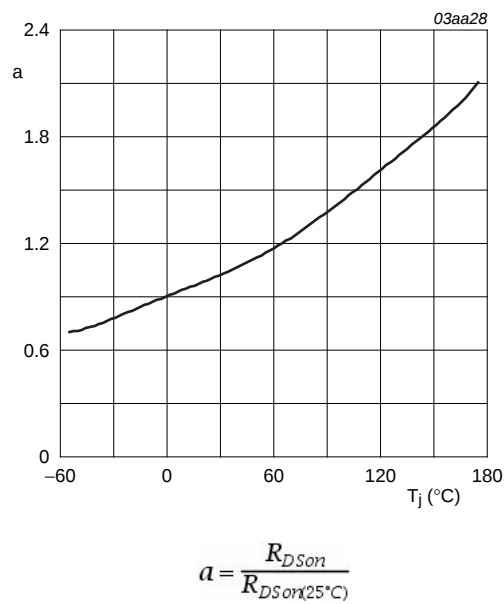


Fig 13. Normalized drain-source on-state resistance factor as a function of junction temperature

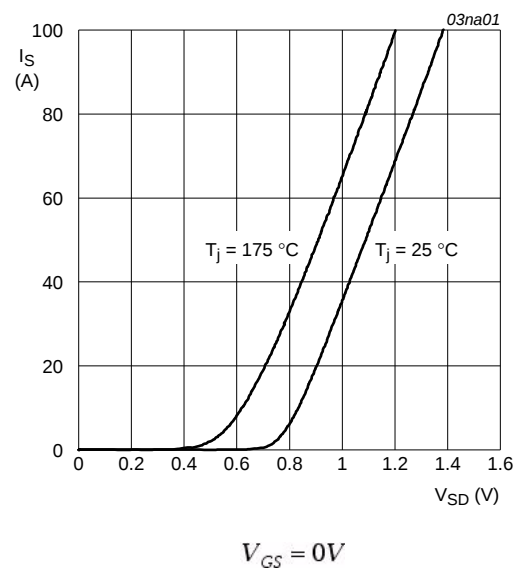
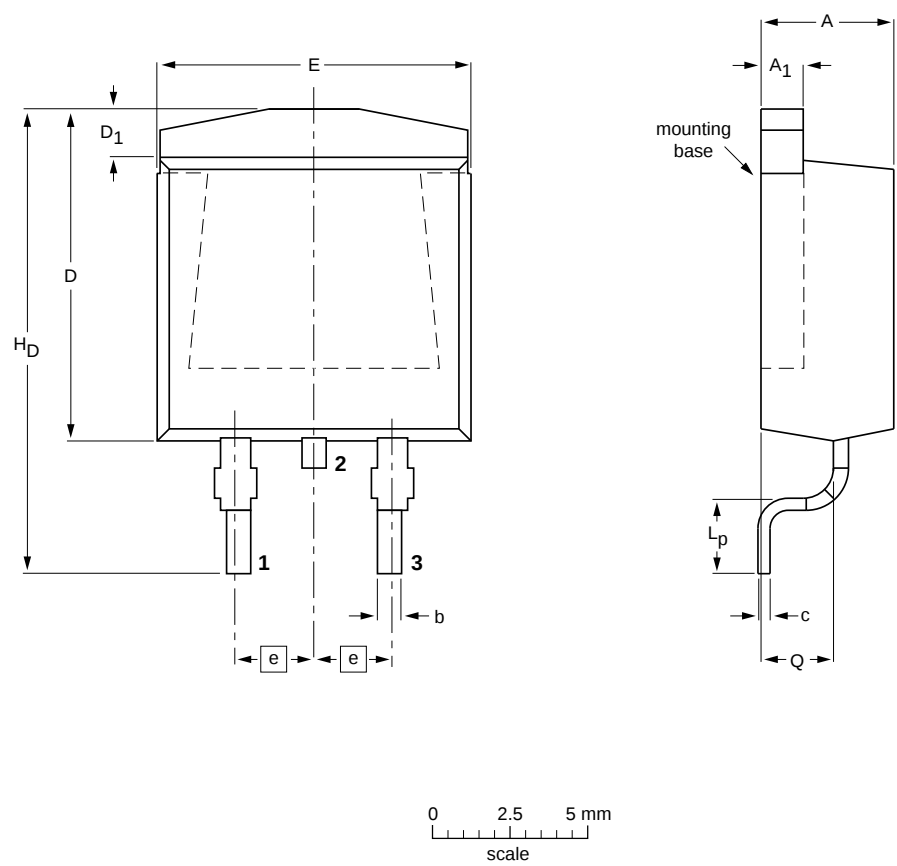


Fig 14. Reverse diode current as a function of reverse diode voltage; typical values

7. Package outline

Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)

SOT404



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁	b	c	D _{max.}	D ₁	E	e	L _p	H _D	Q
mm	4.50 4.10	1.40 1.27	0.85 0.60	0.64 0.46	11	1.60 1.20	10.30 9.70	2.54	2.90 2.10	15.80 14.80	2.60 2.20

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT404						05-02-11 06-03-16

Fig 15. Package outline SOT404 (D2PAK)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK9624-55A v.2	20110131	Product data sheet	-	BUK9524_9624_55A v.1
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Type number BUK9624-55A separated from data sheet BUK9524_9624_55A v.1. • Various changes to content.			
BUK9524_9624_55A v.1	20000929	Product specification	-	-

9. Legal information

9.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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