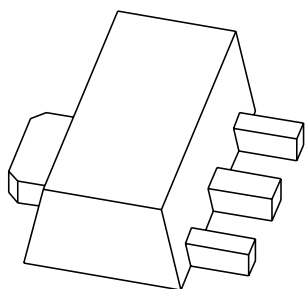


DATA SHEET



BF621; BF623 PNP high-voltage transistors

Product specification
Supersedes data of 1999 Apr 21

2004 Dec 14

PNP high-voltage transistors

BF621; BF623

FEATURES

- Low current (max. 50 mA)
- High voltage (max. 300 V).

APPLICATIONS

- Video output stages.

DESCRIPTION

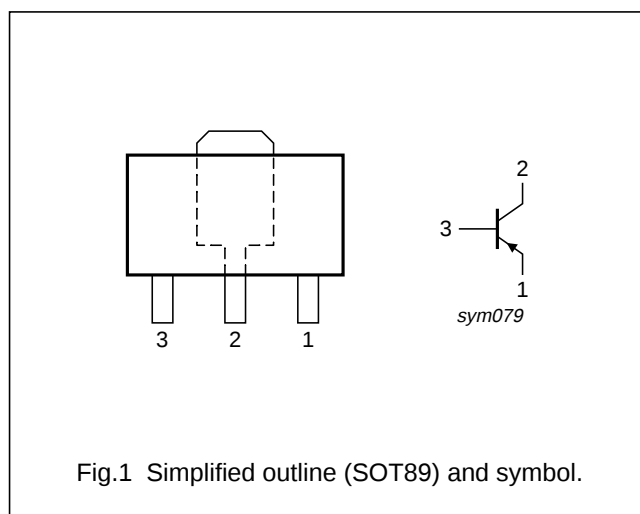
PNP high-voltage transistor in a SOT89 plastic package.
NPN complements: BF620 and BF622.

MARKING

TYPE NUMBER	MARKING CODE
BF621	DF
BF623	DB

PINNING

PIN	DESCRIPTION
1	emitter
2	collector
3	base



ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
BF621	SC-62	plastic surface mounted package; collector pad for good heat transfer; 3 leads	SOT89
BF623			

PNP high-voltage transistors

BF621; BF623

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

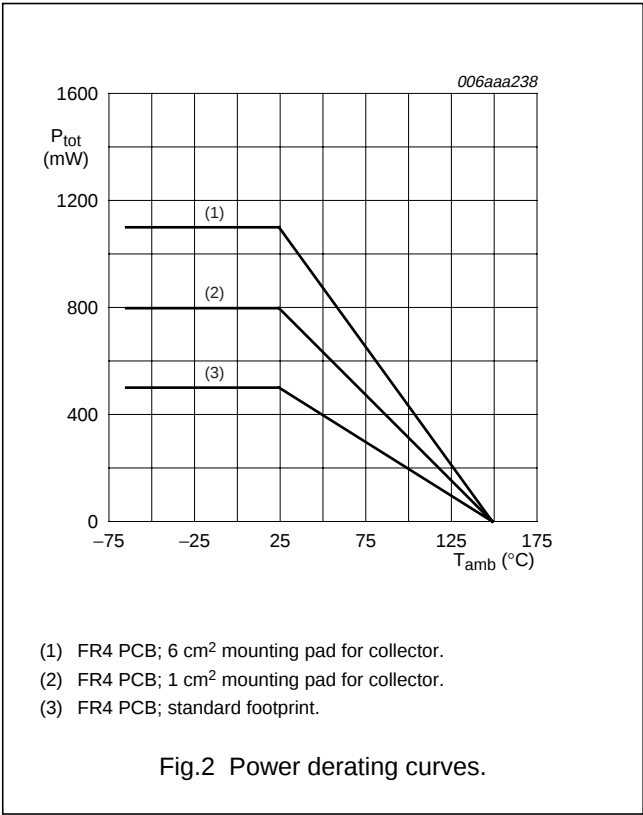
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter			
	BF621		–	–300	V
	BF623		–	–250	V
V_{CEO}	collector-emitter voltage	open base			
	BF621		–	–300	V
	BF623		–	–250	V
V_{EBO}	emitter-base voltage	open collector	–	–5	V
I_C	collector current (DC)		–	–50	mA
I_{CM}	peak collector current		–	–100	mA
I_{BM}	peak base current		–	–50	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25\text{ °C}$			
		note 1	–	0.5	W
		note 2	–	0.8	W
		note 3	–	1.1	W
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	150	°C
T_{amb}	ambient temperature		–65	+150	°C

Notes

1. Device mounted on a printed-circuit board, single-sided copper, tin-plated and standard footprint.
2. Device mounted on a printed-circuit board, single-sided copper, tin-plated and mounting pad for collector 1 cm².
3. Device mounted on a printed-circuit board, single-sided copper, tin-plated and mounting pad for collector 6 cm².

PNP high-voltage transistors

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PNP high-voltage transistors

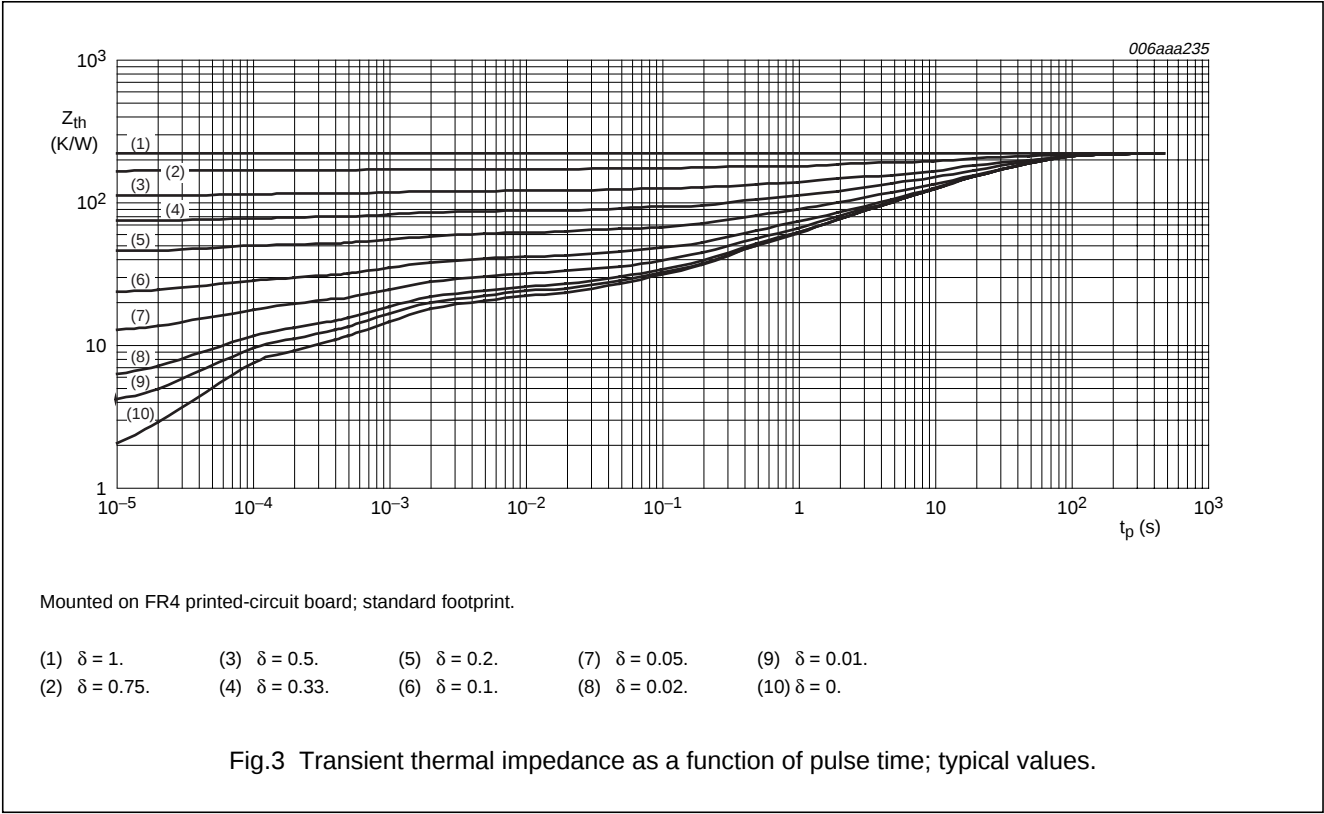
BF621; BF623

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air		
		note 1	250	K/W
		note 2	156	K/W
		note 3	113	K/W
$R_{th(j-s)}$	thermal resistance from junction to soldering point		30	K/W

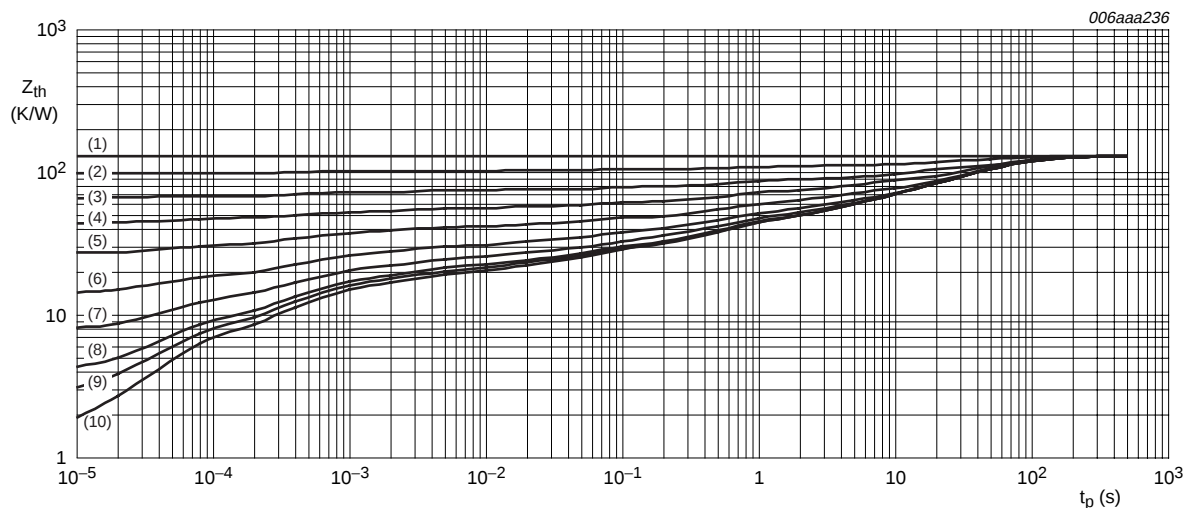
Notes

- 1. Device mounted on a printed-circuit board, single-sided copper, tin-plated and standard footprint.
- 2. Device mounted on a printed-circuit board, single-sided copper, tin-plated and mounting pad for collector 1 cm².
- 3. Device mounted on a printed-circuit board, single-sided copper, tin-plated and mounting pad for collector 6 cm².



PNP high-voltage transistors

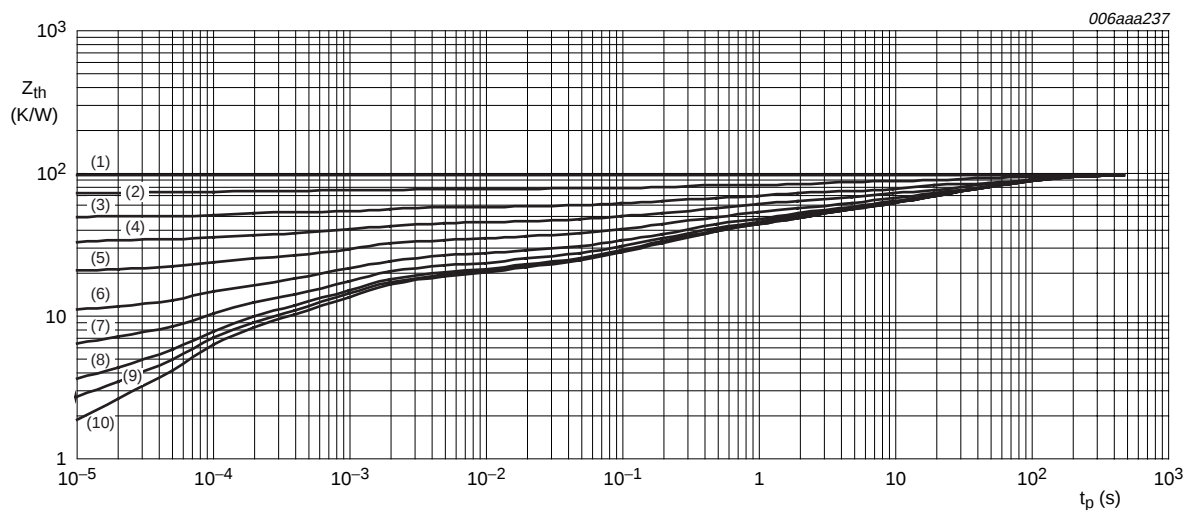
BF621; BF623



Mounted on FR4 printed-circuit board; mounting pad for collector 1 cm².

- | | | | | |
|----------------------|----------------------|---------------------|----------------------|----------------------|
| (1) $\delta = 1.$ | (3) $\delta = 0.5.$ | (5) $\delta = 0.2.$ | (7) $\delta = 0.05.$ | (9) $\delta = 0.01.$ |
| (2) $\delta = 0.75.$ | (4) $\delta = 0.33.$ | (6) $\delta = 0.1.$ | (8) $\delta = 0.02.$ | (10) $\delta = 0.$ |

Fig.4 Transient thermal impedance as a function of pulse time; typical values.



Mounted on FR4 printed-circuit board; mounting pad for collector 6 cm².

- | | | | | |
|----------------------|----------------------|---------------------|----------------------|----------------------|
| (1) $\delta = 1.$ | (3) $\delta = 0.5.$ | (5) $\delta = 0.2.$ | (7) $\delta = 0.05.$ | (9) $\delta = 0.01.$ |
| (2) $\delta = 0.75.$ | (4) $\delta = 0.33.$ | (6) $\delta = 0.1.$ | (8) $\delta = 0.02.$ | (10) $\delta = 0.$ |

Fig.5 Transient thermal impedance as a function of pulse time; typical values.

PNP high-voltage transistors

BF621; BF623

CHARACTERISTICS $T_{\text{amb}} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
I_{CBO}	collector-base cut-off current	$I_{\text{E}} = 0\text{ A}; V_{\text{CB}} = -200\text{ V}$	–	–10	nA
		$I_{\text{E}} = 0\text{ A}; V_{\text{CB}} = -200\text{ V}; T_{\text{j}} = 150\text{ }^{\circ}\text{C}$	–	–10	μA
I_{EBO}	emitter-base cut-off current	$I_{\text{C}} = 0\text{ A}; V_{\text{EB}} = -5\text{ V}$	–	–50	nA
h_{FE}	DC current gain	$I_{\text{C}} = -25\text{ mA}; V_{\text{CE}} = -20\text{ V}$	50	–	
V_{CEsat}	collector-emitter saturation voltage	$I_{\text{C}} = -30\text{ mA}; I_{\text{B}} = -5\text{ mA}$	–	–800	mV
C_{re}	feedback capacitance	$I_{\text{C}} = i_{\text{c}} = 0\text{ A}; V_{\text{CE}} = -30\text{ V}; f = 1\text{ MHz}$	–	1.6	pF
f_{T}	transition frequency	$I_{\text{C}} = -10\text{ mA}; V_{\text{CE}} = -10\text{ V}; f = 100\text{ MHz}$	60	–	MHz

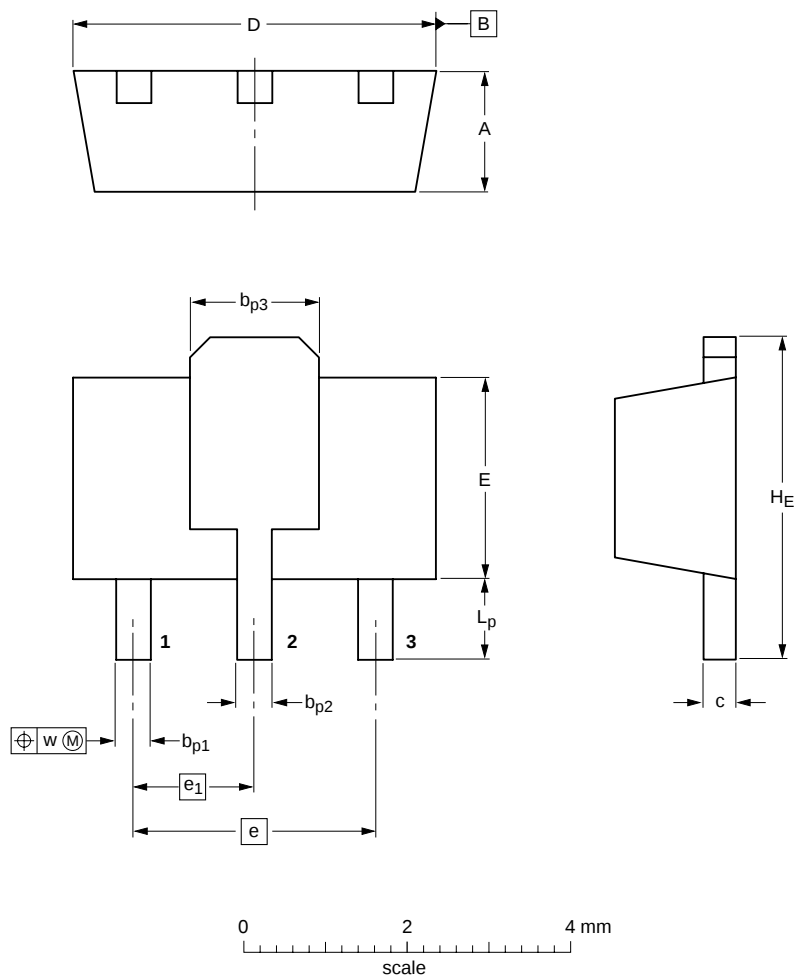
PNP high-voltage transistors

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PACKAGE OUTLINE

Plastic surface mounted package; collector pad for good heat transfer; 3 leads

SOT89



DIMENSIONS (mm are the original dimensions)

UNIT	A	b _{p1}	b _{p2}	b _{p3}	c	D	E	e	e ₁	H _E	L _p	w
mm	1.6 1.4	0.48 0.35	0.53 0.40	1.8 1.4	0.44 0.23	4.6 4.4	2.6 2.4	3.0	1.5	4.25 3.75	1.2 0.8	0.13

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT89		TO-243	SC-62			99-09-13 04-08-03

PNP high-voltage transistors

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DATA SHEET STATUS

LEVEL	DATA SHEET STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾⁽³⁾	DEFINITION
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