Sauls Wharf House
Crittens Road
Great Yarmouth
Norfolk
NR31 0AG

Telephone +44 (0)1493 602602
Email:sales@midasdisplays.com
Email:tech@midasdisplays.com
www.midasdisplays.com

| MDOT136160AY-WS | 136 x 160 | OLED Module |
|---|---|---|
| **Specification** | | |
| Version: 1 | | Date: 16/02/2015 |
| **Revision** | | |
| 1 | 13/02/2015 | First Issue |

| Display Features | |
|---|---|
| Resolution | 136 x 160 |
| Appearance | White on Black |
| Logic Voltage | 2.8V |
| Interface | SPI |
| Module Size | 32.70 x 54.85 x 1.00mm |
| Operating Temperature | -40°C ~ +80°C |
| Construction | COT |

RoHS compliant

| Box Quantity | Weight / Display |
|---|---|
| --- | --- |

* - For full design functionality, please use this specification in conjunction with the SH1108 specification. (Provided Separately)

| Display Accessories | |
|---|---|
| **Part Number** | **Description** |
| | |
| | |
| | |

| Optional Variants | |
|---|---|
| **Appearance** | **Voltage** |
| | |

## *Basic Specifications*

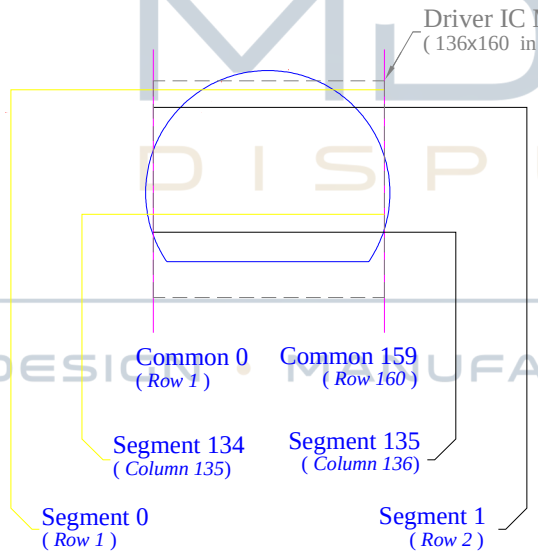
### Display Specifications

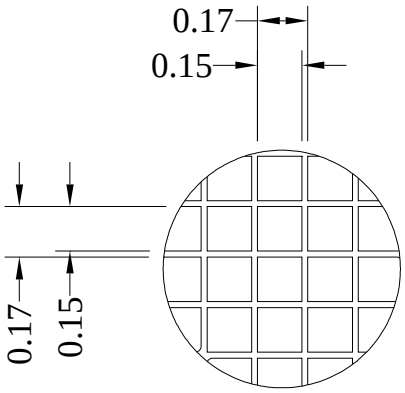
1) Display Mode : Passive Matrix
2) Display Color : Monochrome (White)
3) Drive Duty : 1/160 Duty

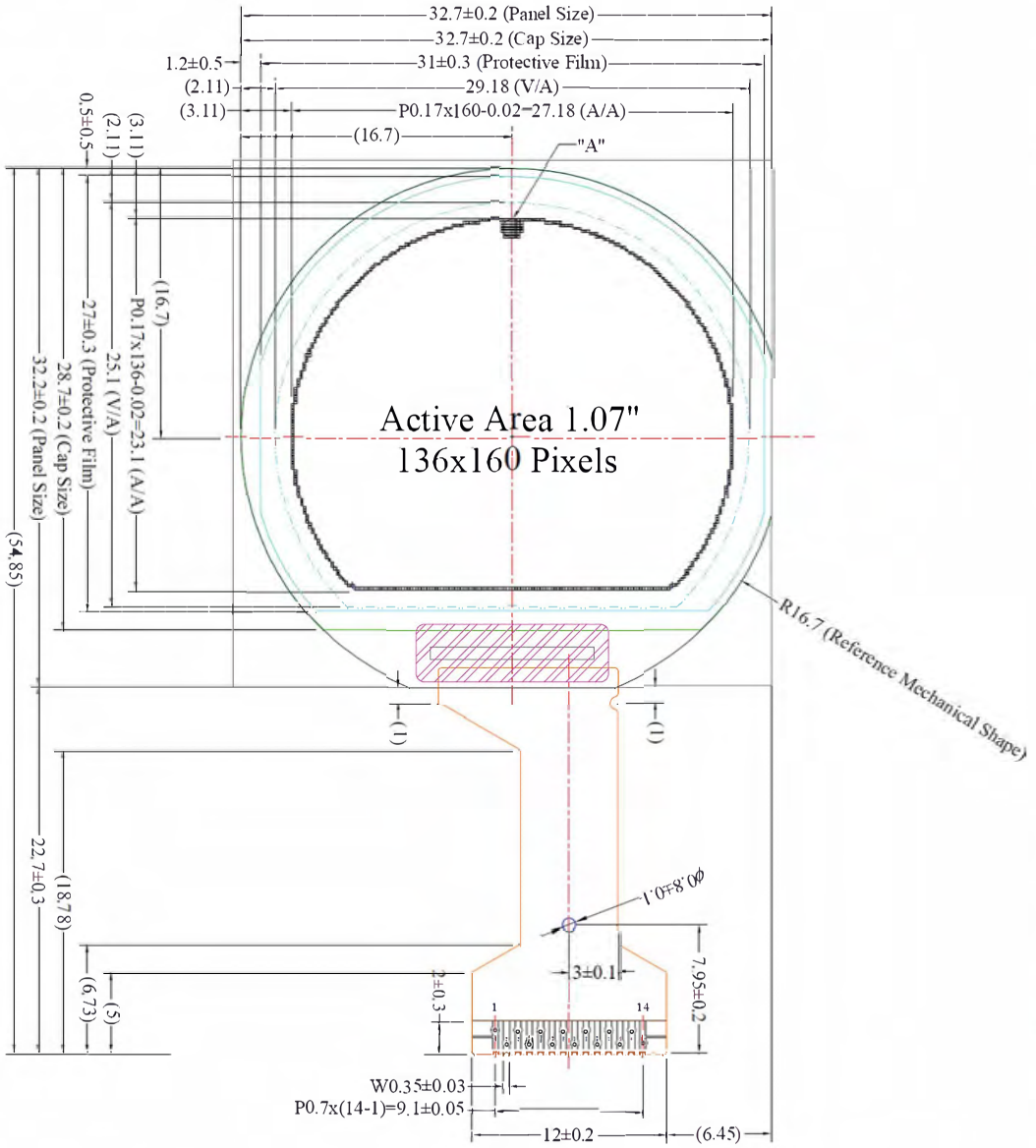
### Mechanical Specifications

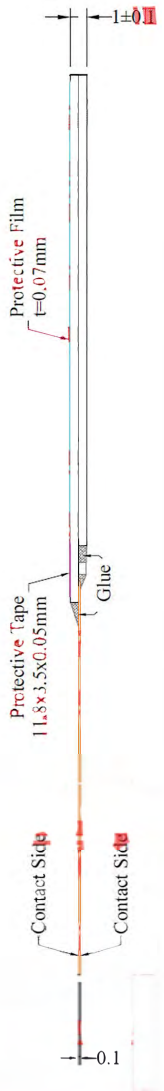
1) Outline Drawing : According to the annexed outline drawing
2) Number of Pixels : 136 × 160
3) Module Size : 32.70 × 54.85 × 1.00 (mm)
4) Panel Size : 32.70 × 32.20 × 1.00 (mm) as "Polarizer Free"
5) Active Area : 27.18 × 23.1 (mm)
6) Pixel Pitch : 0.17 × 0.17 (mm)
7) Pixel Size : 0.15 × 0.15 (mm)
8) Weight : TBD (g) ± 10%

### Memory Mapping & Pixel Construction

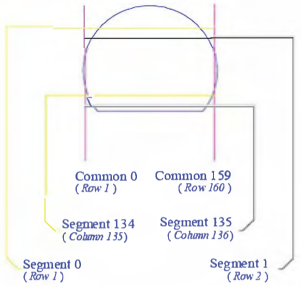


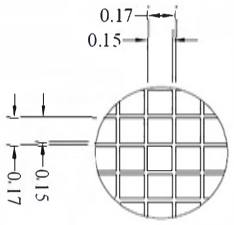






| Pin | Symbol |
|---|---|
| 1 | GND |
| 2 | VPP |
| 3 | VSL |
| 4 | VSEGM |
| 5 | VCOMH |
| 6 | GND |
| 7 | VDD |
| 8 | IREF |
| 9 | CSB |
| 10 | RESB |
| 11 | A0 |
| 12 | SCL |
| 13 | SI |
| 14 | GND |




Detail "A"
Scale (10:1)

Notes:

1. Color: White
2. Driver IC: SH1108
3. Interface: 4-wire SPI
4. General Tolerance: ±0.30
5. The total thickness (1.1 Max) is without Protective Film.
   The actual assembled total thickness with above materials should be 1.2 Max

## Pin Definition

| Pin Number | Symbol | I/O | Function |
|---|---|---|---|
| ***Power Supply*** | | | |
| 7 | VDD | P | **Power Supply for Logic**<br>This is a voltage supply pin. It must be connected to external source. |
| 6 | GND | P | **Ground of OEL System**<br>This is a ground pin. It also acts as a reference for the logic pins, the OEL driving voltages, and the analog circuits. It must be connected to external ground. |
| 2 | VPP | P | **Power Supply for OEL Panel**<br>This is the most positive voltage supply pin of the chip. It must be supplied externally. |
| ***Driver*** | | | |
| 5 | VCOMH | O | **Voltage Output High Level for COM Signal**<br>This pin is for the voltage output high level for COM signals. A capacitor should be connected between this pin and GND. |
| 4 | VSEGM | O | **Voltage Output High Level for Segment Pre-Charge**<br>This pin is for the voltage output high level for SEG pre-charge. A capacitor should be connected between this pin and GND. |
| 3 | VSL | P | **Voltage Reference of Segment**<br>This pin is segment voltage reference pin. A capacitor should be connected between this pin and GND. |
| 8 | IREF | O | **Current Reference for Brightness Adjustment**<br>This pin is segment current reference pin. A resistor should be connected between this pin and GND. Set the current at 15.625μA maximum. |
| ***Interface*** | | | |
| 9 | CSB | | **Chip Select**<br>when CSB is pulled low. |
| 10 | RESB | I | **Power Reset for Controller and Driver**<br>This pin is reset signal input. When the pin is low, initialization of the chip is executed. |
| 11 | A0 | I | **Data/Command Control**<br>When the pin is pulled high and serial interface mode is selected, the data at SI is treated as data. When it is pulled low, the data at SI will be transferred to the command register. |
| 12 | SCL | I | **Serial Clock Input Signal**<br>The transmission of information in the bus is following a clock signal. Each transmission of data bit is taken place during a single clock period of this pin. |
| 13 | SI | I | **Serial Data Input Signal**<br>This pin acts as a communication channel. The input data through SI are latched at the rising edge of SCL in the sequence of MSB first and converted to 8-bit parallel data and handled at the rising edge of last serial clock.<br>SI is identified to display data or command by A0 bit data at the rising of first SCL. |
| ***Reserve*** | | | |
| 1, 14 | GND | - | **Reserved Pin (Supporting Pin)**<br>The supporting pins can reduce the influences from stresses on the function pins. These pins must be connected to external ground as the ESD protection circuit. |

## *Absolute Maximum Ratings*

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Supply Voltage for Logic | $V_{DD}$ | -0.3 | 3.6 | V | 1, 2 |
| Supply Voltage for Display | $V_{PP}$ | 0 | 10 | V | 1, 2 |
| Operating Temperature | $T_{OP}$ | -40 | 70 | °C | |
| Storage Temperature | $T_{STG}$ | -40 | 85 | °C | |
| Life Time (200 cd/m$^2$) | | 20,000 | - | hour | 3 |

Note 1: All the above voltages are on the basis of "$GND$ = 0V".

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to Section 3. "Optics & Electrical Characteristics". If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

Note 3: $V_{PP}$ = 12.0V, $T_a$ = 25°C, 50% Checkerboard. Software configuration follows Section 4.5 Initialization. End of lifetime is specified as 50% of initial brightness reached. The average operating lifetime at room temperature is estimated by the accelerated operation at high temperature conditions.

## *Optics & Electrical Characteristics*

### Optics Characteristics

| Characteristics | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Brightness | $L_{br}$ | Note 4 | 150 | 200 | - | $cd/m^2$ |
| C.I.E. (White) | (x)<br>(y) | C.I.E. 1931 | 0.25<br>0.27 | 0.29<br>0.31 | 0.33<br>0.35 | |
| Dark Room Contrast | CR | | - | >10,000:1 | - | |
| Viewing Angle | | | - | Free | - | degree |

* Optical measurement taken at $V_{DD}$ = 2.8V, $V_{PP}$ = 12.0V.
Software configuration follows Section 4.5 Initialization.

### DC Characteristics

| Characteristics | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Supply Voltage for Logic | $V_{DD}$ | | 1.65 | 2.8 | 3.5 | V |
| Supply Voltage for Display | $V_{PP}$ | Note 4 | 11.5 | 12.0 | 12.5 | V |
| High Level Input | $V_{IHC}$ | | $0.8\times V_{DD}$ | - | $V_{DD}$ | V |
| Low Level Input | $V_{ILC}$ | | 0 | - | $0.2\times V_{DD}$ | V |
| High Level Output | $V_{OHC}$ | $I_{OH}$ = -500µA | $0.8\times V_{DD}$ | - | $V_{DD}$ | V |
| Low Level Output | $V_{OLC}$ | $I_{OL}$ = 500µA | 0 | - | $0.2\times V_{DD}$ | V |
| Operating Current for $V_{DD}$ | $I_{DD}$ | | - | 170 | 250 | µA |
| Operating Current for $V_{PP}$ | $I_{PP}$ | Note 5 | - | 10.7 | 13.4 | mA |
| | | Note 6 | - | 15.8 | 19.8 | mA |
| | | Note 7 | - | 26.6 | 33.3 | mA |
| Sleep Mode Current for $V_{DD}$ | $I_{DD, SLEEP}$ | | - | 2 | 5 | µA |
| Sleep Mode Current for $V_{PP}$ | $I_{PP, SLEEP}$ | | - | 1 | 5 | µA |

Note 4: Brightness ($L_{br}$) and Supply Voltage for Display ($V_{PP}$) are subject to the change of the panel characteristics and the customer's request.
Note 5: $V_{DD}$ = 2.8V, $V_{PP}$ = 12.0V, 30% Display Area Turn on.
Note 6: $V_{DD}$ = 2.8V, $V_{PP}$ = 12.0V, 50% Display Area Turn on.
Note 7: $V_{DD}$ = 2.8V, $V_{PP}$ = 12.0V, 100% Display Area Turn on.

* Software configuration follows Section 4.5 Initialization.

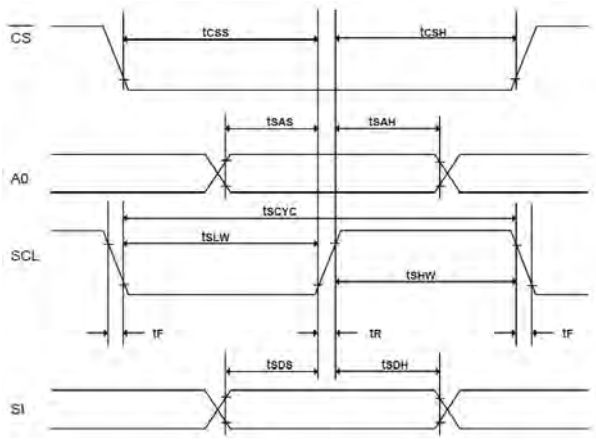
## AC Characteristics

| Symbol | Description | Min | Max | Unit |
|---|---|---|---|---|
| $t_{SCYC}$ | Serial Clock Cycle Time | 250 | - | ns |
| $t_{SAS}$ | Address Setup Time | 150 | - | ns |
| $t_{SAH}$ | Address Hold Time | 150 | - | ns |
| $t_{SDS}$ | Data Setup Time | 100 | - | ns |
| $t_{SDH}$ | Data Hold Time | 100 | - | ns |
| $t_{CSS}$ | Chip Select Setup Time | 120 | - | ns |
| $t_{CSH}$ | Chip Select Hold Time | 60 | - | ns |
| $t_{SLW}$ | Serial Clock L Pulse Width | 100 | - | ns |
| $t_{SHW}$ | Serial Clock H Pulse Width | 100 | - | ns |
| $t_R$ | Rise Time | - | 15 | ns |
| $t_F$ | Fall Time | - | 15 | ns |

* ($V_{DD}$ - GND = 1.65V to 1.8V, $T_a$ = 25°C)

| Symbol | Description | Min | Max | Unit |
|---|---|---|---|---|
| $t_{SCYC}$ | Serial Clock Cycle Time | 200 | - | ns |
| $t_{SAS}$ | Address Setup Time | 120 | - | ns |
| $t_{SAH}$ | Address Hold Time | 120 | - | ns |
| $t_{SDS}$ | Data Setup Time | 80 | - | ns |
| $t_{SDH}$ | Data Hold Time | 80 | - | ns |
| $t_{CSS}$ | Chip Select Setup Time | 96 | - | ns |
| $t_{CSH}$ | Chip Select Hold Time | 48 | - | ns |
| $t_{SLW}$ | Serial Clock L Pulse Width | 80 | - | ns |
| $t_{SHW}$ | Serial Clock H Pulse Width | 80 | - | ns |
| $t_R$ | Rise Time | - | 12 | ns |
| $t_F$ | Fall Time | - | 12 | ns |

* ($V_{DD}$ - GND = 1.8V to 3.5V, $T_a$ = 25°C)



## *Functional Specification*

### Commands

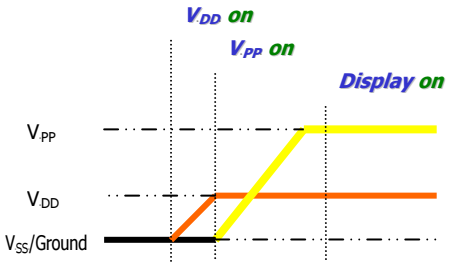
Refer to the Technical Manual for the SH1108

### Power down and Power up Sequence

To protect OEL panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. It gives the OEL panel enough time to complete the action of charge and discharge before/after the operation.

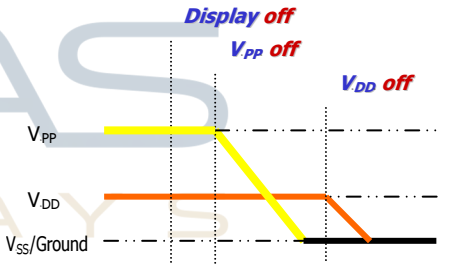
Power up Sequence:

1. Power up $V_{DD}$
2. Send Display off command
3. Initialization
4. Clear Screen
5. Power up $V_{PP}$
6. Delay 100ms
   (When $V_{PP}$ is stable)
7. Send Display on command




Power down Sequence:

1. Send Display off command
2. Power down $V_{PP}$
3. Delay 100ms
   (When $V_{PP}$ is reach 0 and panel is completely discharges)
4. Power down $V_{DD}$




Note 8:

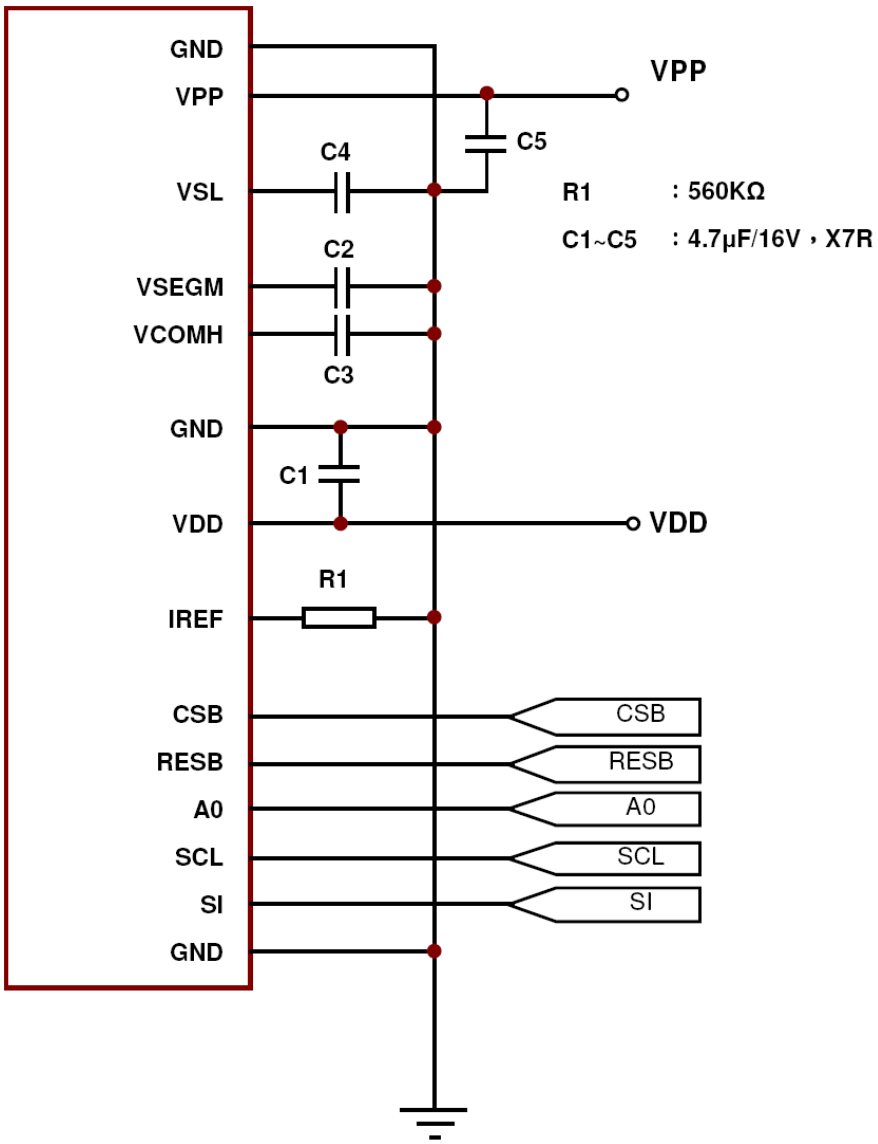
1) Since an ESD protection circuit is connected between $V_{DD}$ and $V_{PP}$ inside the driver IC, $V_{PP}$ becomes lower than $V_{DD}$ whenever $V_{DD}$ is ON and $V_{PP}$ is OFF.
2) $V_{PP}$ should be kept float (disable) when it is OFF.
3) Power Pins ($V_{DD}$, $V_{PP}$) can never be pulled to ground under any circumstance.
4) $V_{DD}$ should not be power down before $V_{PP}$ power down.

### Reset Circuit

When RESB input is low, the chip is initialized with the following status:

1. Display is OFF
2. 160×160 Display Mode
3. Normal segment and display data column and row address mapping (SEG0 mapped to column address 00h and COM0 mapped to row address 00h)
4. Shift register data clear in serial interface
5. Display start line is set at display RAM address 0
6. Column address counter is set at 0
7. Normal scan direction of the COM outputs
8. Contrast control register is set at 80h
9. Internal booster is selected

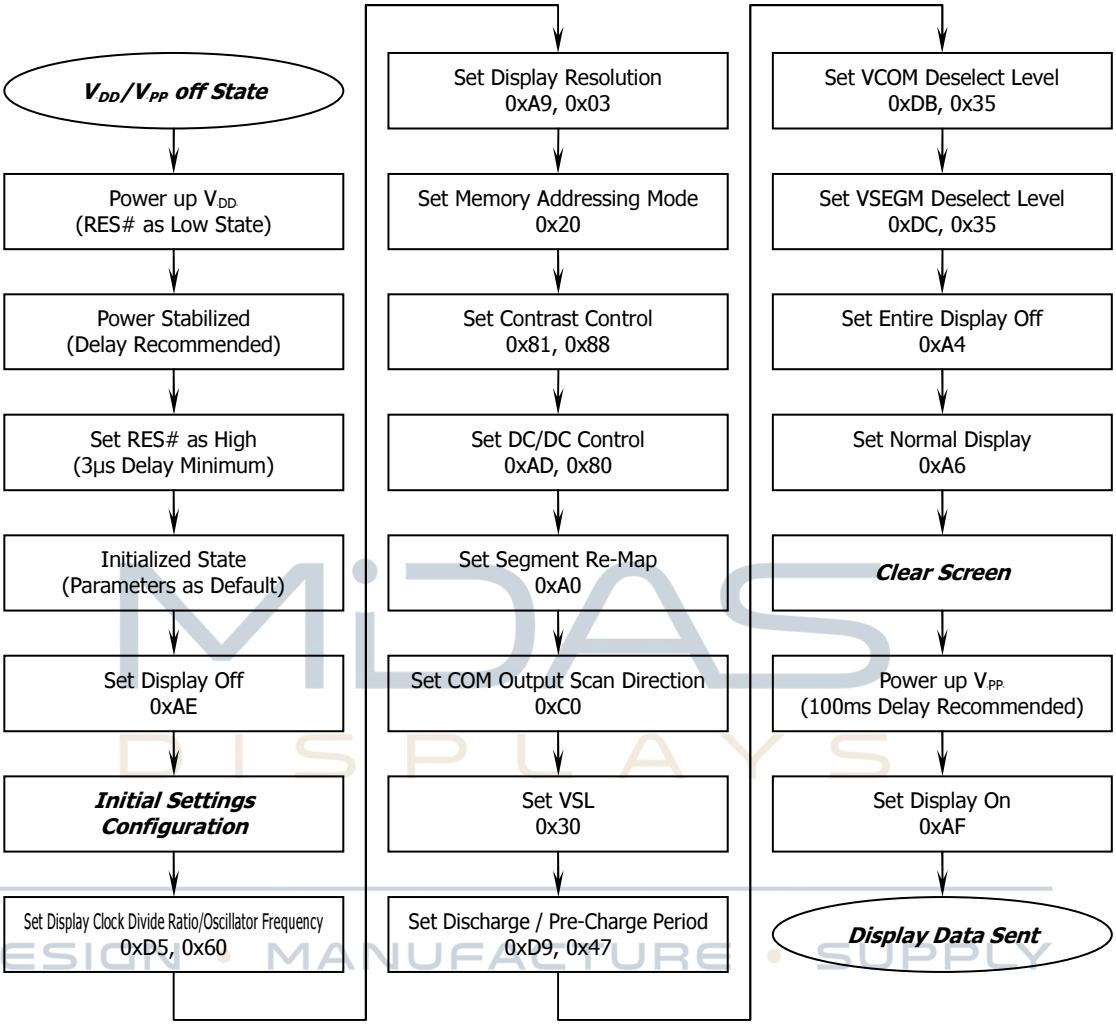
## Peripheral Circuit



**Actual Application Example**

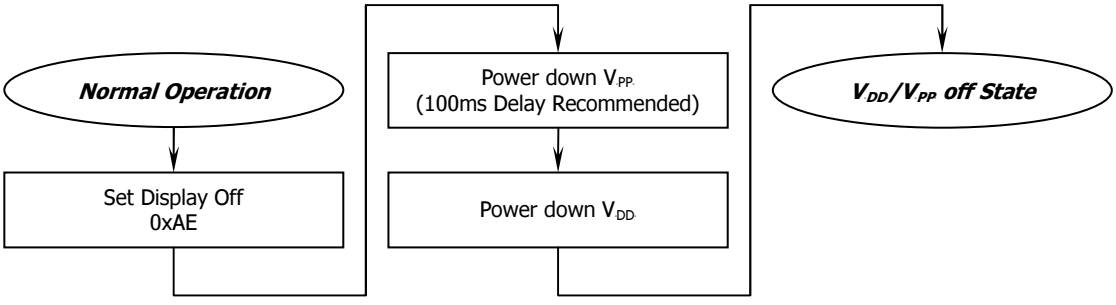
Command usage and explanation of an actual example

<Power up Sequence>

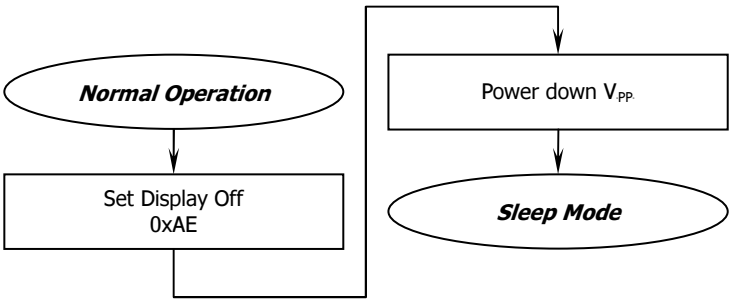



If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

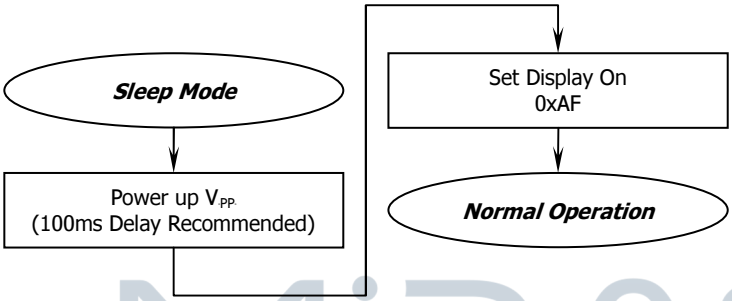
<Power down Sequence>



<Entering Sleep Mode>




<Exiting Sleep Mode>



## *Reliability*

### Contents of Reliability Tests

| Item | Conditions | Criteria |
|---|---|---|
| High Temperature Operation | 70°C, 240 hrs | The operational functions work. |
| Low Temperature Operation | -40°C, 240 hrs | |
| High Temperature Storage | 85°C, 240 hrs | |
| Low Temperature Storage | -40°C, 240 hrs | |
| High Temperature/Humidity Operation | 60°C, 90% RH, 120 hrs | |
| Thermal Shock | -40°C ⇔ 85°C, 24 cycles<br>60 mins dwell | |

* The samples used for the above tests do not include polarizer.
* No moisture condensation is observed during tests.

### Failure Check Standard

After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure test at 23±5°C; 55±15% RH.

## *Outgoing Quality Control Specifications*

### Environment Required

Customer's test & measurement are required to be conducted under the following conditions:

| | |
|---|---|
| Temperature: | 23 ± 5°C |
| Humidity: | 55 ± 15% RH |
| Fluorescent Lamp: | 30W |
| Distance between the Panel & Lamp: | ≥ 50cm |
| Distance between the Panel & Eyes of the Inspector: | ≥ 30cm |

Finger glove (or finger cover) must be worn by the inspector.
Inspection table or jig must be anti-electrostatic.

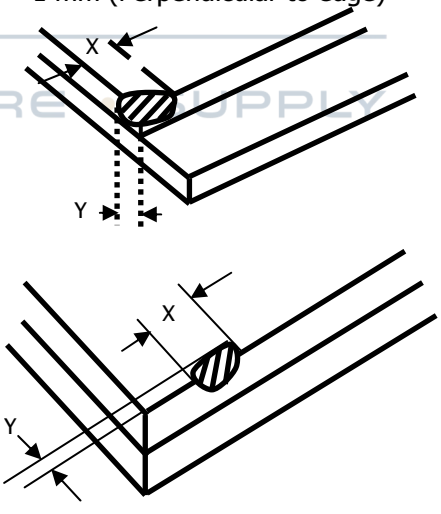
### Sampling Plan

Level II, Normal Inspection, Single Sampling, MIL-STD-105E

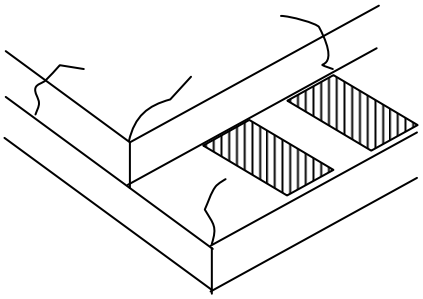
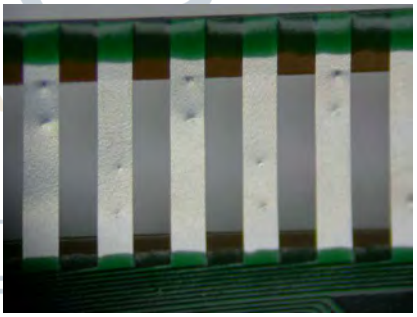
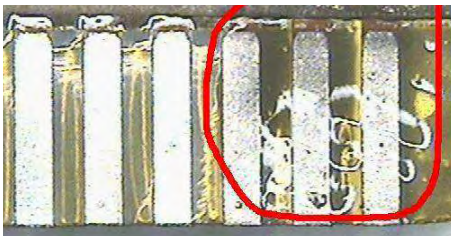
### Criteria & Acceptable Quality Level

| Partition | AQL | Definition |
|---|---|---|
| Major | 0.65 | Defects in Pattern Check (Display On) |
| Minor | 1.0 | Defects in Cosmetic Check (Display Off) |

6.3.1 Cosmetic Check (Display Off) in Non-Active Area

| Check Item | Classification | Criteria |
|---|---|---|
| Panel General Chipping | Minor | X > 6 mm (Along with Edge)<br>Y > 1 mm (Perpendicular to edge)<br>  |

Cosmetic Check (Display Off) in Non-Active Area (Continued)

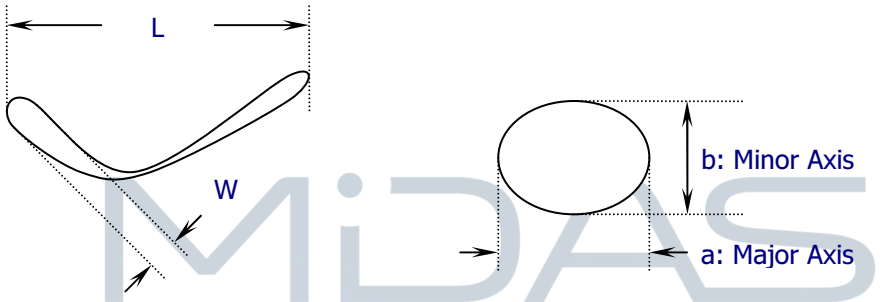
| Check Item | Classification | Criteria |
|---|---|---|
| Panel Crack | Minor | Any crack is not allowable.<br>  |
| Copper Exposed<br>(Even Pin or Film) | Minor | Not Allowable by Naked Eye Inspection |
| Film or Trace Damage | Minor |  |
| Terminal Lead Prober Mark | Acceptable |  |
| Glue or Contamination on Pin<br>(Couldn't Be Removed by Alcohol) | Minor |  |
| Ink Marking on Back Side of panel<br>(Exclude on Film) | Acceptable | Ignore for Any |

Cosmetic Check (Display Off) in Active Area

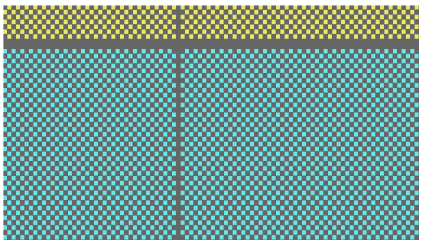
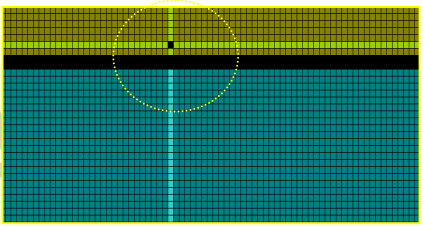
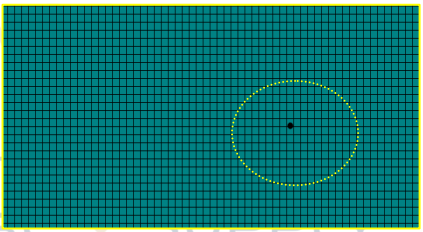
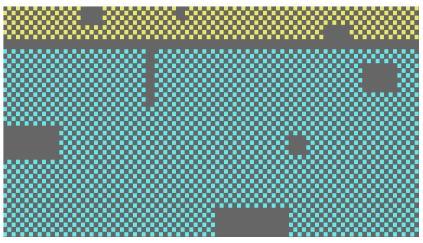
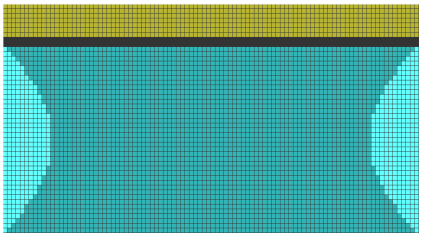
It is recommended to execute in clear room environment (class 10k) if actual in necessary.

| Check Item | Classification | Criteria |
|---|---|---|
| Any Dirt & Scratch on Protective Film | Acceptable | Ignore for Any |
| Scratches, Fiber, Line-Shape Defect (On Glass Display Side) | Minor | W ≤ 0.1 Ignore<br>W > 0.1<br>L ≤ 2 n ≤ 1<br>L > 2 n = 0 |
| Dirt, Spot-Shape Defect (On Glass Display Side) | Minor | Φ ≤ 0.1 Ignore<br>0.1 < Φ ≤ 0.25 n ≤ 1<br>0.25 < Φ n = 0 |
| Fingerprint, Flow Mark (On Glass Display Side) | Minor | Not Allowable |

* Definition of W & L & Φ (Unit: mm): Φ = (a + b) / 2



6.3.3 Pattern Check (Display On) in Active Area

| Check Item | Classification | Criteria |
|---|---|---|
| No Display | Major |  |
| Missing Line | Major |  |
| Pixel Short | Major |  |
| Darker Pixel | Major |  |
| Wrong Display | Major |  |
| Un-uniform | Major |  |

MiDAS
DISPLAYS

DESIGN • MANUFACTURE • SUPPLY