

N-channel 600 V, 0.078 Ω typ., 34 A MDmesh M2
Power MOSFETs in D²PAK, TO-220 and TO-247 packages

Datasheet – production data

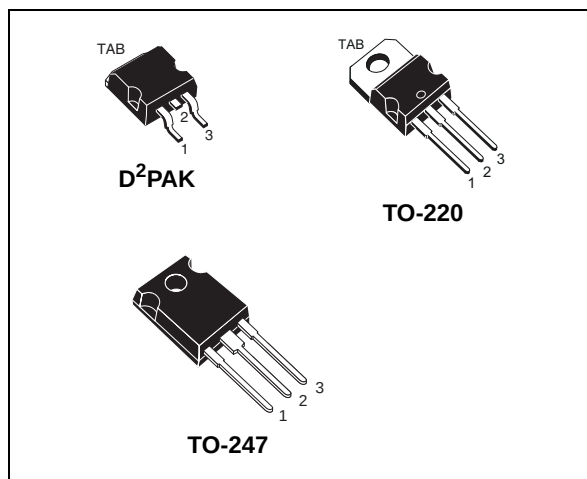
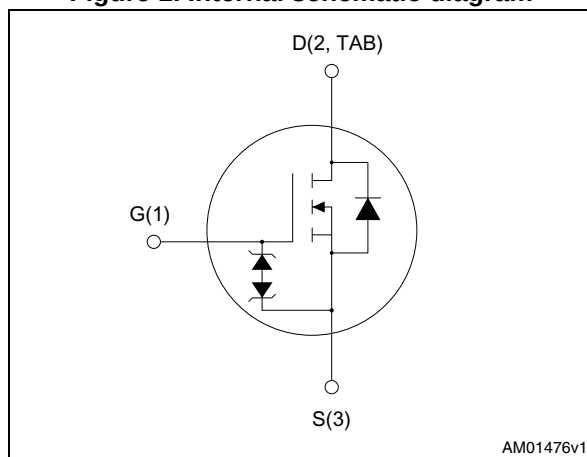


Figure 1. Internal schematic diagram



Features

Order code	$V_{DS} @ T_{Jmax}$	$R_{DS(on)}$ max	I_D
STB40N60M2	650 V	0.088 Ω	34 A
STP40N60M2			
STW40N60M2			

- Extremely low gate charge
- Excellent output capacitance (C_{oss}) profile
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications
- LLC converters, resonant converters

Description

These devices are N-channel Power MOSFETs developed using MDmesh™ M2 technology. Thanks to their strip layout and improved vertical structure, the devices exhibit low on-resistance and optimized switching characteristics, rendering them suitable for the most demanding high efficiency converters.

Table 1. Device summary

Order code	Marking	Packages	Packing
STB40N60M2	40N60M2	D ² PAK	Tape and reel
STP40N60M2		TO-220	Tube
STW40N60M2		TO-247	

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 25	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	34	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	22	A
$I_{DM}^{(1)}$	Drain current (pulsed)	136	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	250	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
$dv/dt^{(3)}$	MOSFET dv/dt ruggedness	50	V/ns
T_{stg}	Storage temperature range	- 55 to 150	$^{\circ}\text{C}$
T_j	Operating junction temperature range		$^{\circ}\text{C}$

1. Pulse width limited by safe operating area.
2. $I_{SD} \leq 34\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$; $V_{DS\text{ peak}} < V_{(BR)DSS}$, $V_{DD} = 400\text{ V}$.
3. $V_{DS} \leq 480\text{ V}$

Table 3. Thermal data

Symbol	Parameter	Value			Unit
		D ² PAK	TO-220	TO-247	
$R_{thj-case}$	Thermal resistance junction-case	0.50			$^{\circ}\text{C}/\text{W}$
$R_{thj-pcb}$	Thermal resistance junction-pcb ⁽¹⁾	30			$^{\circ}\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient		62.5	50	$^{\circ}\text{C}/\text{W}$

1. When mounted on 1 inch² FR-4, 2 Oz copper board

Table 4. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_{jmax})	6	A
E_{AS}	Single pulse avalanche energy (starting $T_j = 25^{\circ}\text{C}$, $I_D = I_{AR}$; $V_{DD} = 50\text{ V}$)	500	mJ

2 Electrical characteristics

($T_C = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Table 5. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0, I_D = 1\text{ mA}$	600			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0, V_{DS} = 600\text{ V}$			1	μA
		$V_{GS} = 0, V_{DS} = 600\text{ V}, T_C = 125\text{ }^{\circ}\text{C}^{(1)}$			100	μA
I_{GSS}	Gate-body leakage current	$V_{DS} = 0, V_{GS} = \pm 25\text{ V}$			± 10	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}, I_D = 17\text{ A}$		0.078	0.088	Ω

1. Defined by design, not subject to production test

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 100\text{ V}, f = 1\text{ MHz}, V_{GS} = 0$	-	2500	-	pF
C_{oss}	Output capacitance		-	117	-	pF
C_{rss}	Reverse transfer capacitance		-	2.4	-	pF
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{DS} = 0\text{ to }480\text{ V}, V_{GS} = 0$	-	342	-	pF
R_G	Intrinsic gate resistance	$f = 1\text{ MHz}, I_D = 0$	-	4.4	-	Ω
Q_g	Total gate charge	$V_{DD} = 480\text{ V}, I_D = 34\text{ A}, V_{GS} = 10\text{ V}$ (see Figure 17)	-	57	-	nC
Q_{gs}	Gate-source charge		-	10	-	nC
Q_{gd}	Gate-drain charge		-	25.5	-	nC

1. $C_{oss\text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$, $I_D = 34\text{ A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (see Figure 16 and Figure 21)	-	20.5	-	ns
t_r	Rise time		-	13.5	-	ns
$t_{d(off)}$	Turn-off-delay time		-	96	-	ns
t_f	Fall time		-	11	-	ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-	34		A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-	136		A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 34\text{ A}$, $V_{GS} = 0$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 34\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$ (see Figure 18)	-	440		ns
Q_{rr}	Reverse recovery charge		-	8.2		μC
I_{RRM}	Reverse recovery current		-	37		A
t_{rr}	Reverse recovery time	$I_{SD} = 34\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$, $T_J = 150\text{ }^\circ\text{C}$ (see Figure 18)	-	568		ns
Q_{rr}	Reverse recovery charge		-	11.5		μC
I_{RRM}	Reverse recovery current		-	40.5		A

1. Pulse width limited by safe operating area.

2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for D²PAK and TO-220

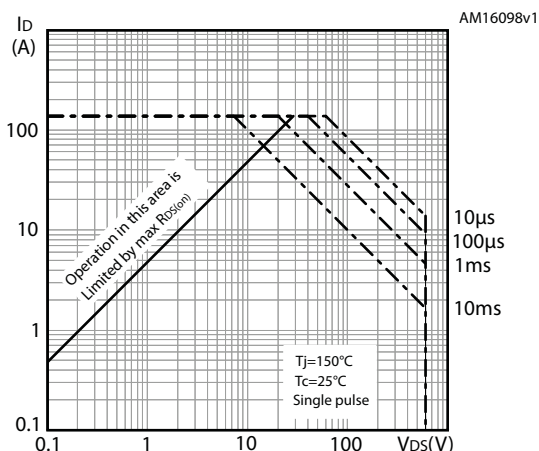


Figure 3. Thermal impedance D²PAK and TO-220

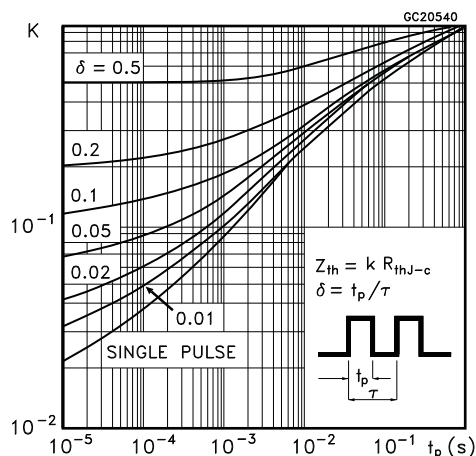


Figure 4. Safe operating area for TO-247

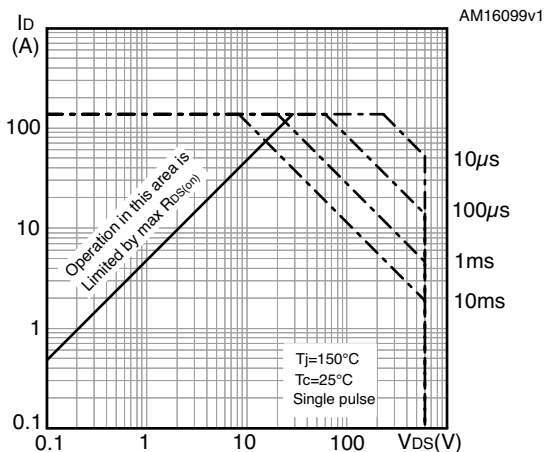


Figure 5. Thermal impedance for TO-247

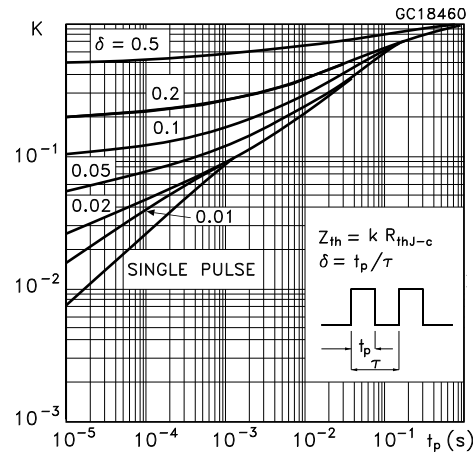


Figure 6. Output characteristics

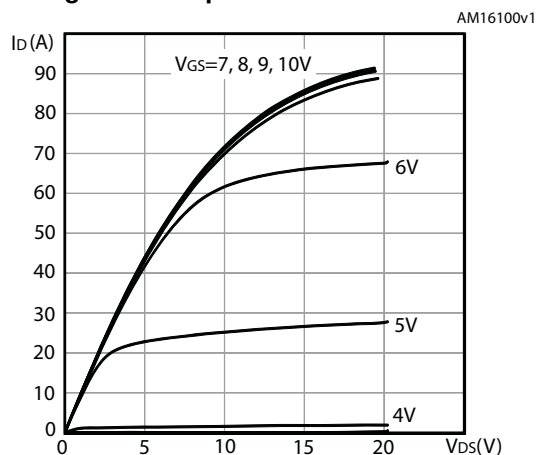


Figure 7. Transfer characteristics

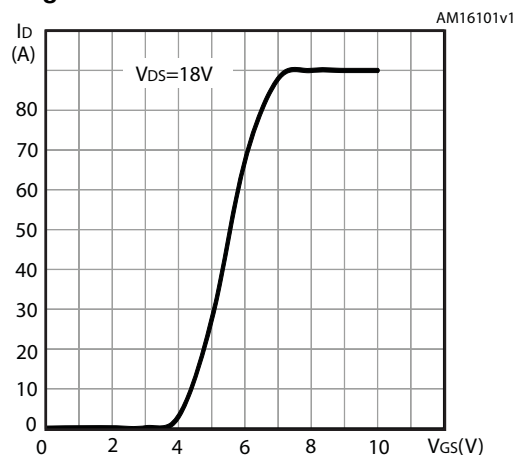


Figure 8. Gate charge vs gate-source voltage

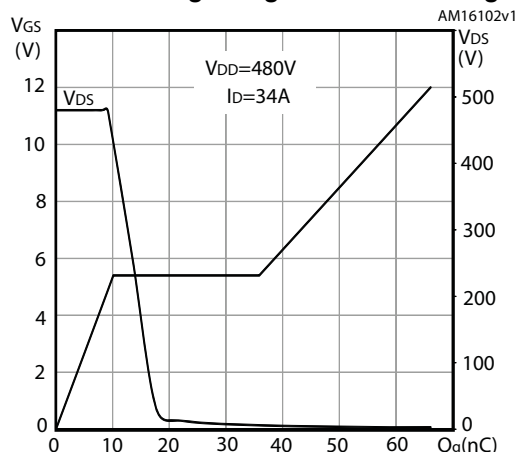


Figure 9. Static drain-source on-resistance

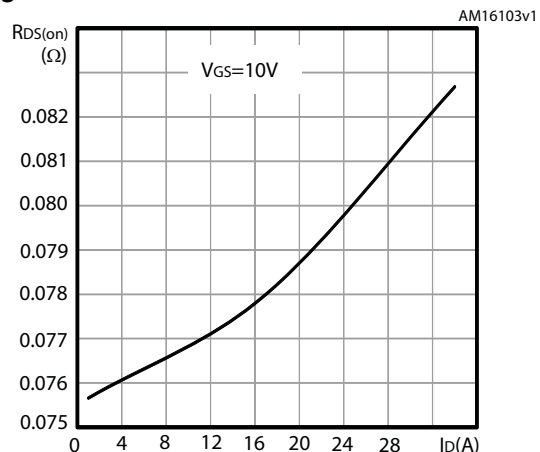


Figure 10. Capacitance variations

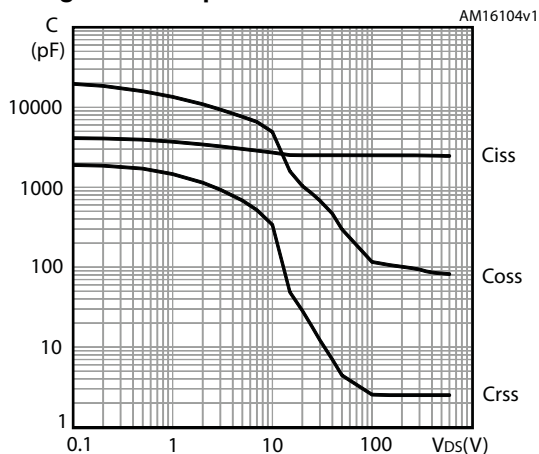


Figure 11. Output capacitance stored energy

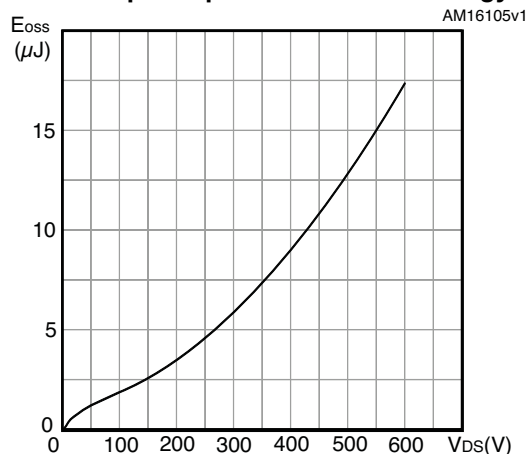


Figure 12. Normalized gate threshold voltage vs temperature

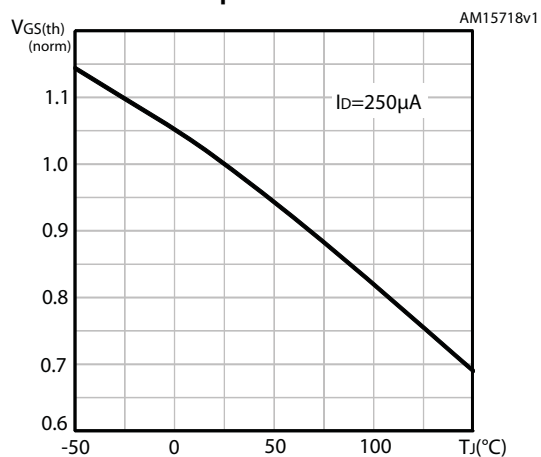


Figure 13. Normalized on-resistance vs temperature

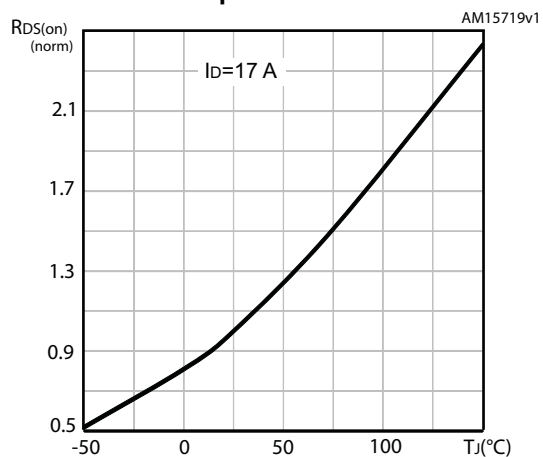


Figure 14. Normalized $V_{(BR)DSS}$ vs temperature

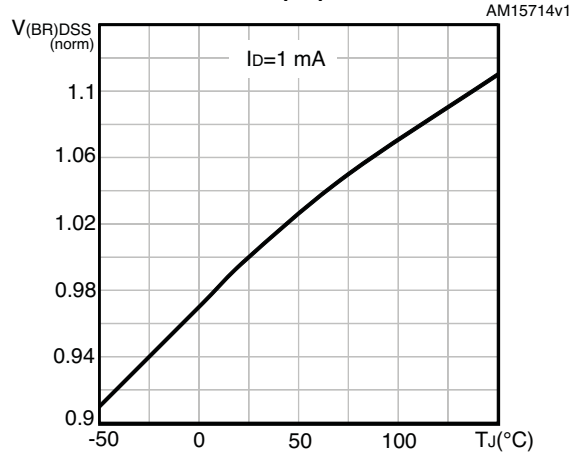
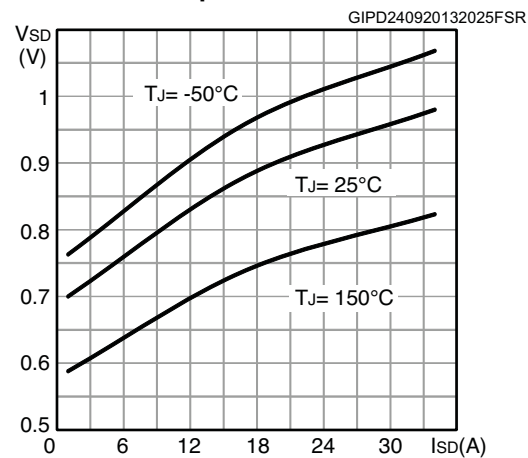
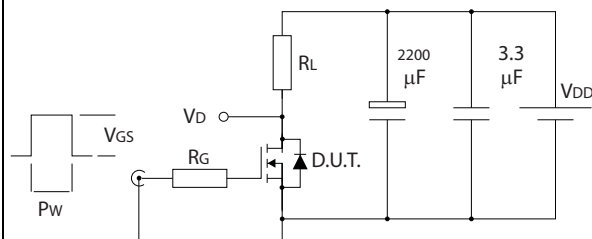


Figure 15. Source-drain diode forward vs temperature



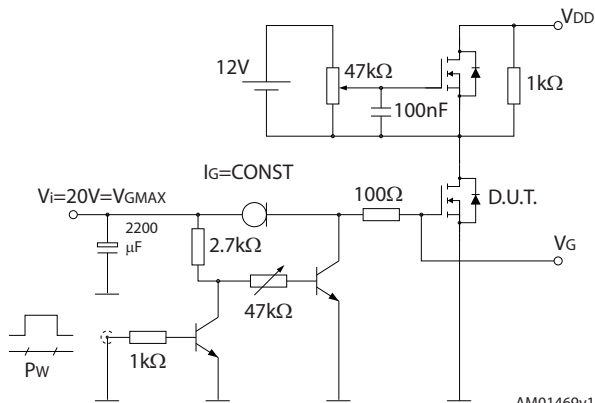
3 Test circuits

Figure 16. Switching times test circuit for resistive load



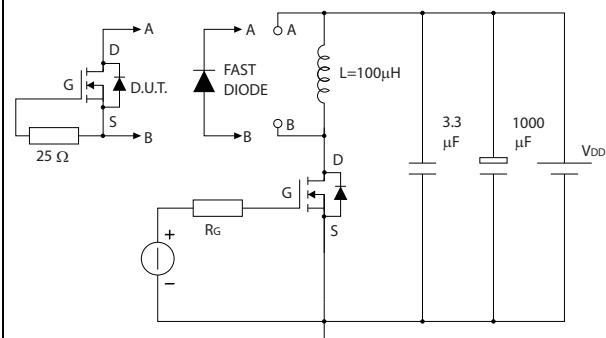
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Figure 17. Gate charge test circuit



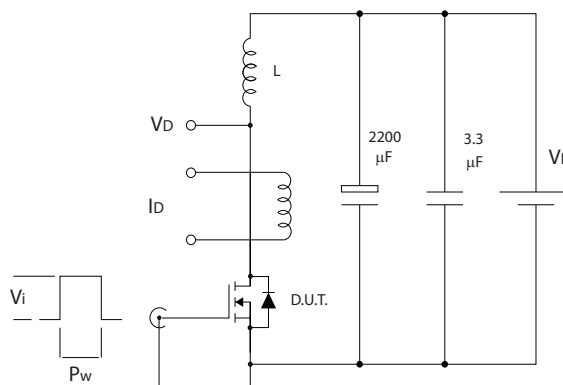
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Figure 18. Test circuit for inductive load switching and diode recovery times



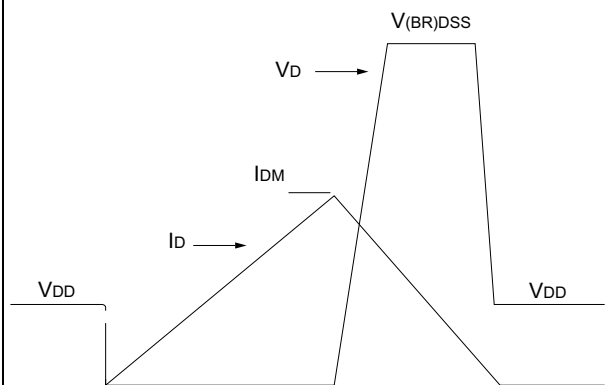
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Figure 19. Unclamped inductive load test circuit



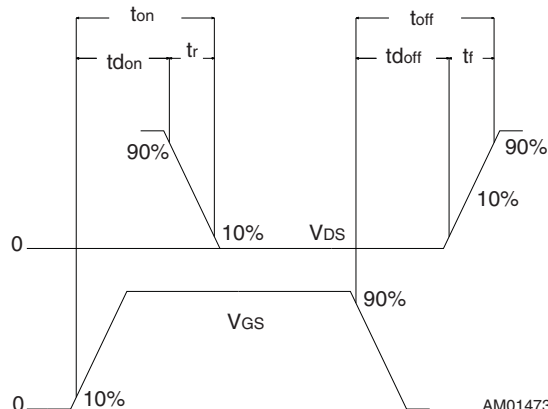
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Figure 20. Unclamped inductive waveform



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Figure 21. Switching time waveform



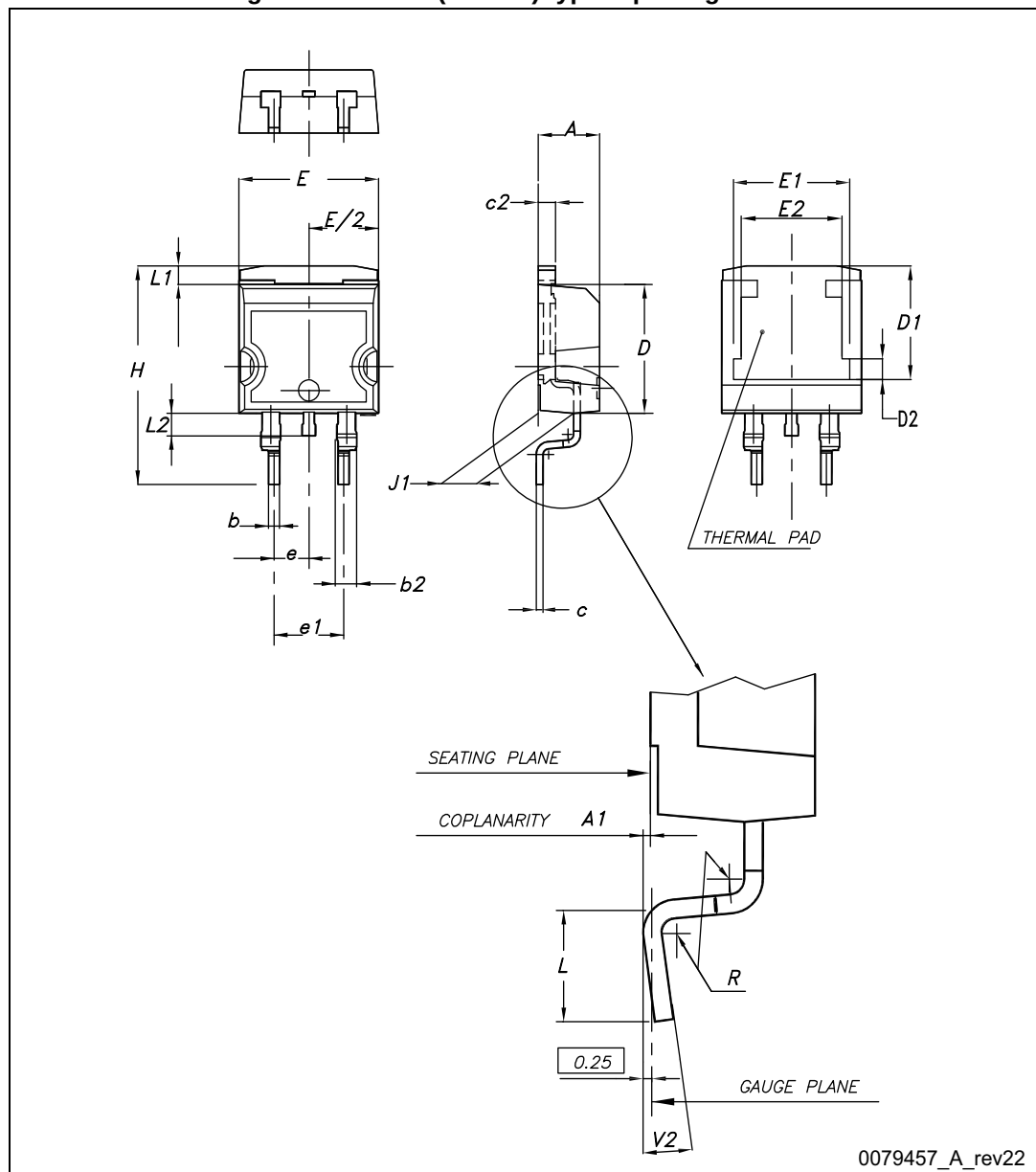
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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

4.1 D²PAK (TO-263) package information

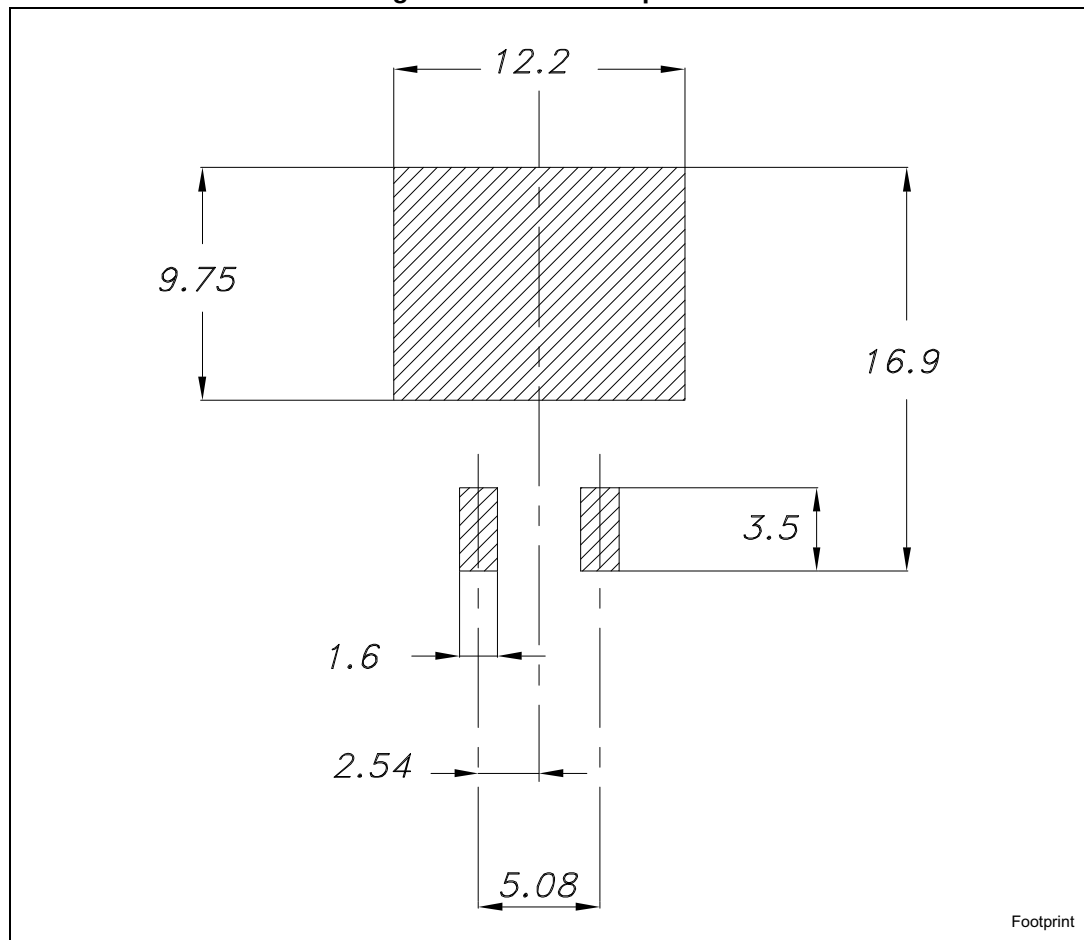
Figure 22. D²PAK (TO-263) type A package outline



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Table 9. D²PAK (TO-263) type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10.00		10.40
E1	8.50	8.70	8.90
E2	6.85	7.05	7.25
e		2.54	
e1	4.88		5.28
H	15.00		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.4	
V2	0°		8°

Figure 23. D²PAK footprint^(a)

a. All dimension are in millimeters

4.2 TO-220 package information

Figure 24. TO-220 type A package outline

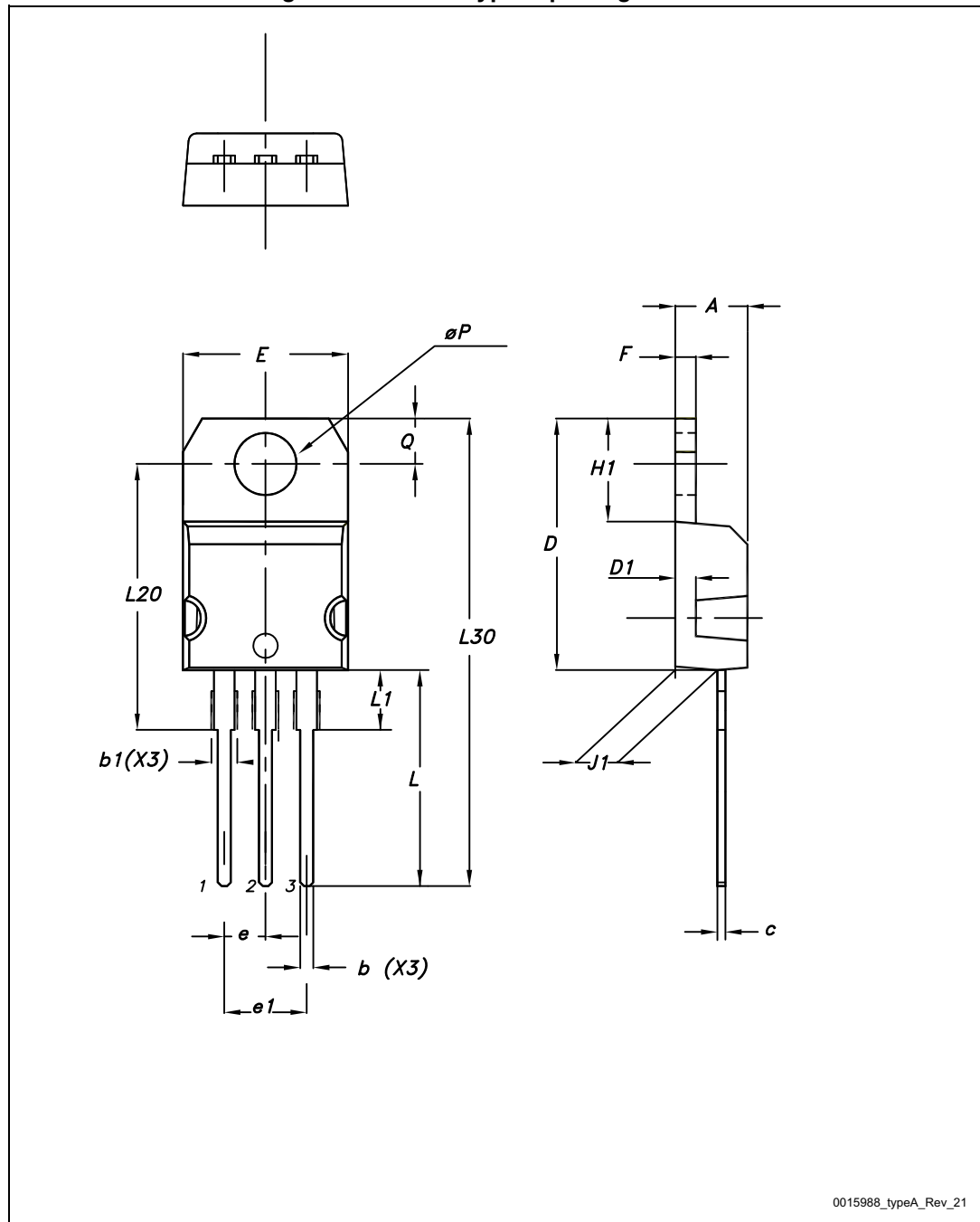


Table 10. TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95

4.3 TO-247 package information

Figure 25. TO-247 package outline

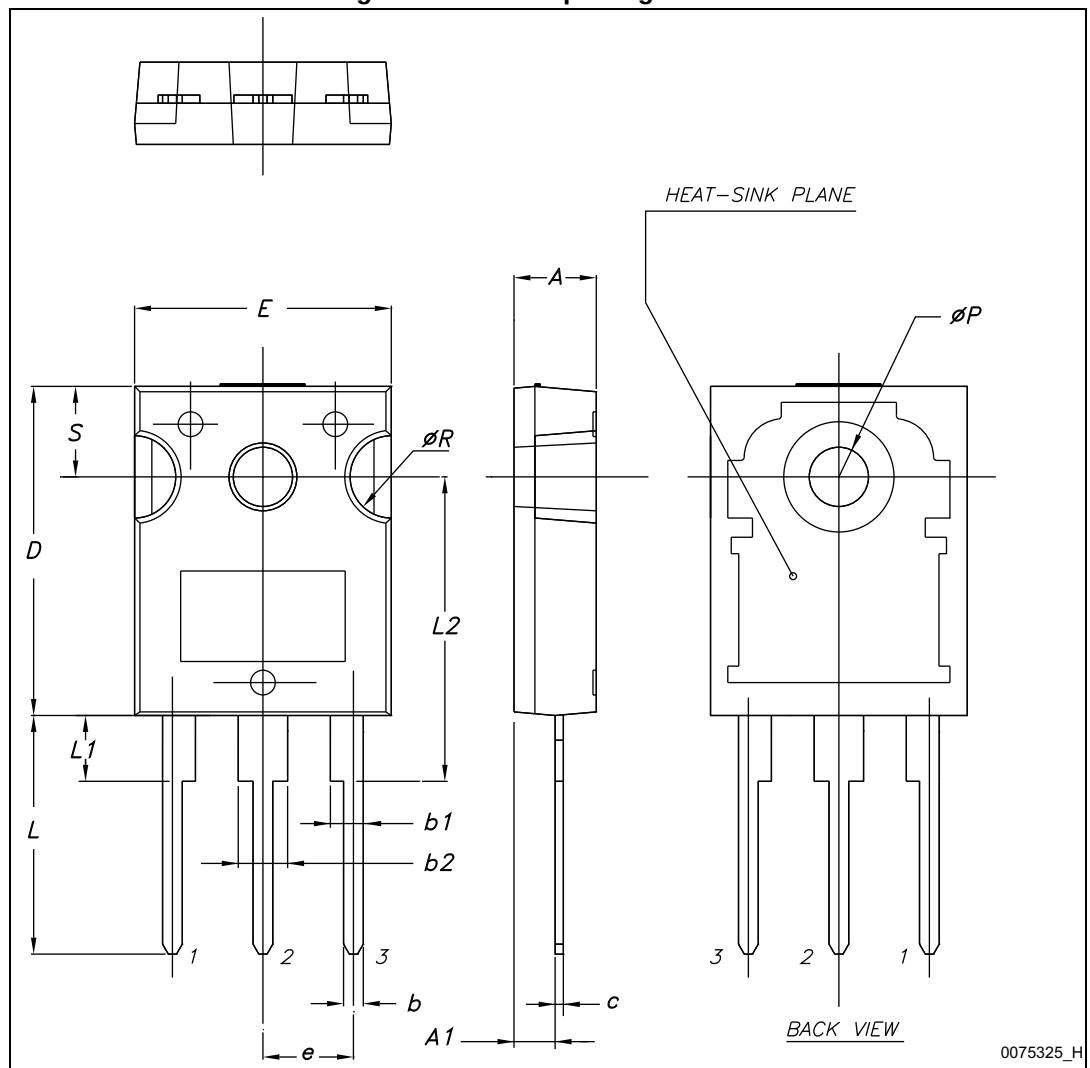


Table 11. TO-247 package mechanical data

Dim.	mm.		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70

5 Packing information

Figure 26. Tape

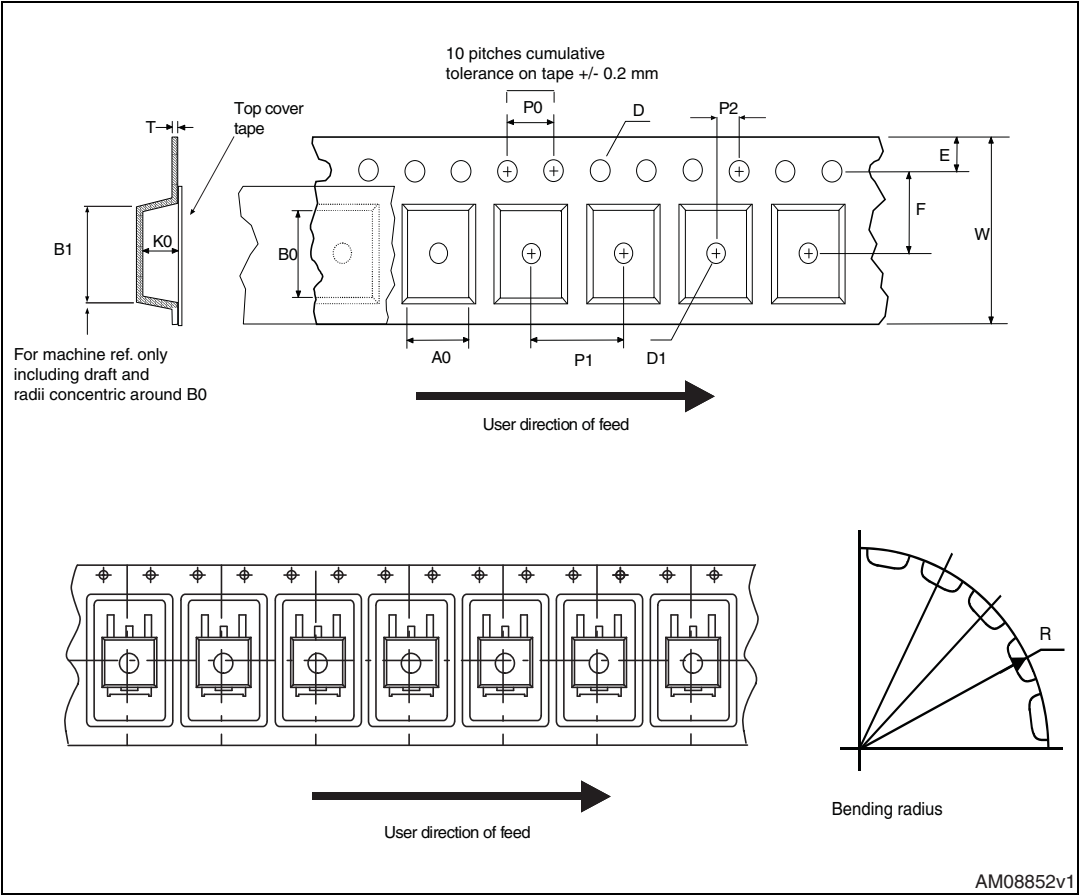
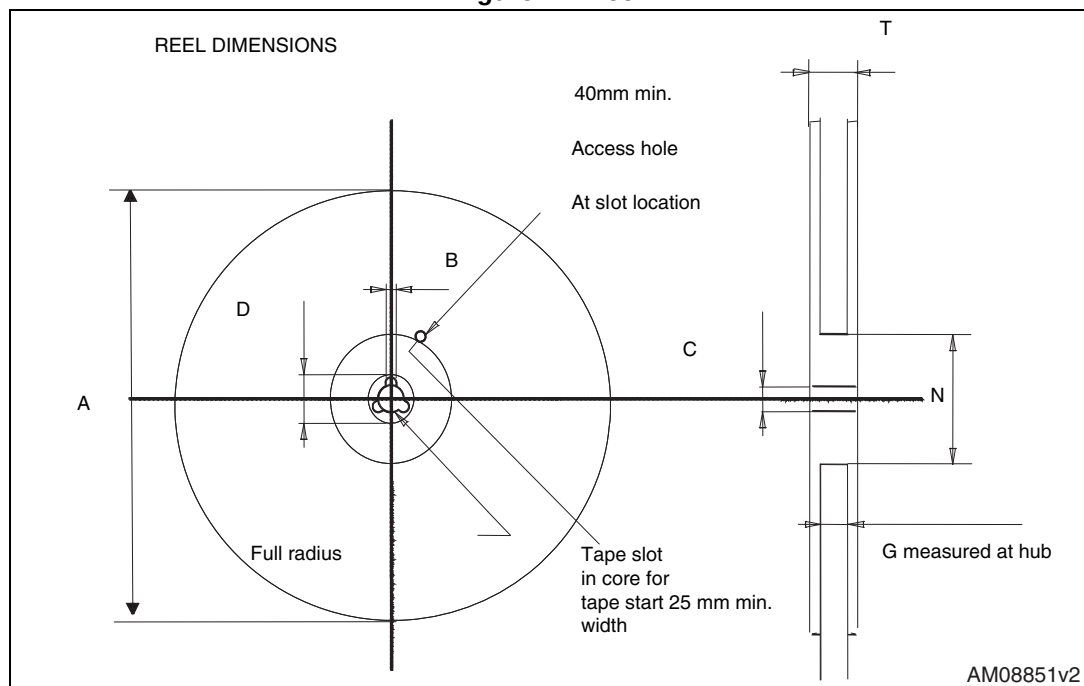


Figure 27. Reel

Table 12. D²PAK (TO-263) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base qty		1000
P2	1.9	2.1	Bulk qty		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

6 Revision history

Table 13. Document revision history

Date	Revision	Changes
01-Jul-2013	1	First release.
23-Sep-2013	2	– Added: TO-220FP and I²PAKFP packages – Inserted: V_{ISO} in <i>Table 2</i> – Modified: values in <i>Table 4</i>, the entire typical values in <i>Table 6</i>, <i>7</i> and <i>8</i> – Updated: <i>Section 4: Package mechanical data</i>. – Minor text changes
13-May-2014	3	– The part numbers STB40N60M2 and STF140N60M2 have been moved to a separate datasheet – Minor text changes
09-Aug-2016	4	Updated title, features and description in cover page. Updated <i>Table 2: Absolute maximum ratings</i>, <i>Table 5: On /off states</i> and <i>Table 8: Source drain diode</i>. Updated <i>Section 4.1: D²PAK (TO-263) package information</i> and <i>Section 4.2: TO-220 package information</i>. Minor text changes.

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