

N-channel 1500 V, 1.6 Ω typ., 7 A MDmesh™ K5

Power MOSFET in a TO-247 package

Datasheet - production data

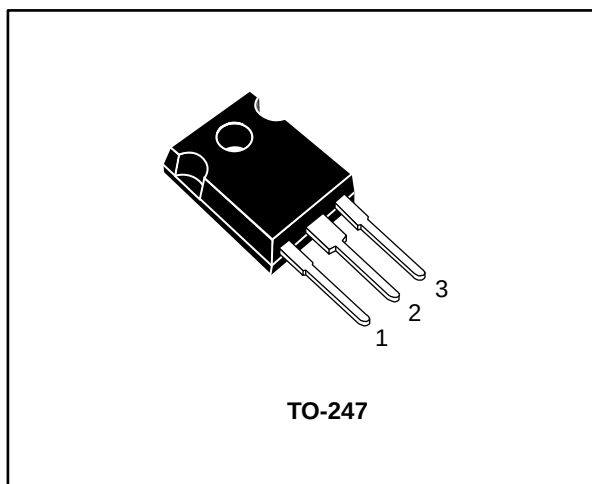
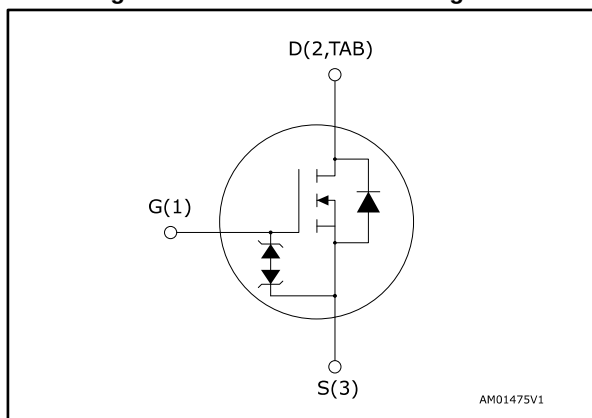


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max.	I _D	P _{TOT}
STW12N150K5	1500 V	1.9 Ω	7 A	250 W

- Industry's lowest R_{DS(on)} * area
- Industry's best figure of merit (FoM)
- Ultra low gate charge
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

This very high voltage N-channel Power MOSFET is designed using MDmesh™ K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

Table 1: Device summary

Order code	Marking	Package	Packing
STW12N150K5	12N150K5	TO-247	Tube

Contents

1	Electrical ratings	3
2	Electrical characteristics	4
	2.1 Electrical characteristics (curves)	6
3	Test circuits	9
4	Package information	10
	4.1 TO-247 package information	10
5	Revision history	12

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 30	V
I_D	Drain current at $T_C = 25\text{ }^{\circ}\text{C}$	7	A
I_D	Drain current at $T_C = 100\text{ }^{\circ}\text{C}$	4	A
$I_{DM}^{(1)}$	Drain current (pulsed)	28	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	250	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	4.5	V/ns
$dv/dt^{(3)}$	MOSFET dv/dt ruggedness	50	V/ns
T_j	Operating junction temperature	- 55 to 150	$^{\circ}\text{C}$
T_{stg}	Storage temperature		

Notes:⁽¹⁾Pulse width limited by safe operating area⁽²⁾ $I_{SD} \leq 7\text{ A}$, $di/dt \leq 100\text{ A}/\mu\text{s}$, $V_{Peak} \leq V_{(BR)DSS}$ ⁽³⁾ $V_{DS} \leq 1200\text{ V}$

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	0.5	$^{\circ}\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-amb	50	$^{\circ}\text{C}/\text{W}$

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Max current during repetitive or single pulse avalanche	2	A
E_{AS}	Single pulse avalanche energy	900	mJ

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 5: On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	V _{GS} = 0 V, I _D = 1 mA	1500			V
I _{DSS}	Zero gate voltage drain current	V _{GS} = 0 V, V _{DS} = 1500 V			1	μA
		V _{GS} = 0 V, V _{DS} = 1500 V, T _C = 125 °C			50	μA
I _{GSS}	Gate body leakage current	V _{DS} = 0, V _{GS} = ± 20 V			±10	μA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 100 μA	3	4	5	V
R _{DS(on)}	Static drain-source on-resistance	V _{GS} = 10 V, I _D = 3.5 A		1.6	1.9	Ω

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iss}	Input capacitance	V _{GS} = 0 V, V _{DS} = 100 V, f = 1 MHz	-	1360	-	pF
C _{oss}	Output capacitance		-	80	-	pF
C _{rss}	Reverse transfer capacitance		-	0.7	-	pF
C _{o(tr)} ⁽¹⁾	Equivalent capacitance time related	V _{DS} = 0 V to 1200 V, V _{GS} = 0 V	-	82	-	pF
C _{o(er)} ⁽²⁾	Equivalent capacitance energy related		-	32	-	pF
R _G	Intrinsic gate resistance	f = 1 MHz, I _D = 0 A	-	3	-	Ω
Q _g	Total gate charge	V _{DD} = 1200V, I _D = 7 A V _{GS} = 10 V (see Figure 16: "Gate charge test circuit")	-	47	-	nC
Q _{gs}	Gate-source charge		-	8	-	nC
Q _{gd}	Gate-drain charge		-	32	-	nC

Notes:

⁽¹⁾ Time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.

⁽²⁾ Energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 750 \text{ V}$, $I_D = 3.5 \text{ A}$, $R_G = 4.7 \text{ } \Omega$ $V_{GS} = 10 \text{ V}$ (see Figure 18: "Unclamped inductive load test circuit")	-	25	-	ns
t_r	Rise time		-	8	-	ns
$t_{d(off)}$	Turn-off delay time		-	90	-	ns
t_f	Fall time		-	37	-	ns

Table 8: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		7	A
I_{SDM}	Source-drain current (pulsed)		-		28	A
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD} = 7 \text{ A}$, $V_{GS} = 0 \text{ V}$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 7 \text{ A}$, $V_{DD} = 60 \text{ V}$ $di/dt = 100 \text{ A}/\mu\text{s}$, (see Figure 17: "Test circuit for inductive load switching and diode recovery times")	-	302		ns
Q_{rr}	Reverse recovery charge		-	3.71		μC
I_{RRM}	Reverse recovery current		-	24.6		A
t_{rr}	Reverse recovery time	$I_{SD} = 7 \text{ A}$, $V_{DD} = 60 \text{ V}$ $di/dt = 100 \text{ A}/\mu\text{s}$, $T_j = 150 \text{ }^\circ\text{C}$ (see Figure 17: "Test circuit for inductive load switching and diode recovery times")	-	432		ns
Q_{rr}	Reverse recovery charge		-	4.71		μC
I_{RRM}	Reverse recovery current		-	21.8		A

Notes:

⁽¹⁾Pulsed: pulse duration = 300 μs , duty cycle 1.5%

Table 9: Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 1 \text{ mA}$, $I_D = 0 \text{ A}$	30	-		V

The built-in back-to-back Zener diodes have been specifically designed to enhance the ESD capability of the device. The Zener voltage is appropriate for efficient and cost-effective intervention to protect the device integrity. These integrated Zener diodes thus eliminate the need for external components.

2.1 Electrical characteristics (curves)

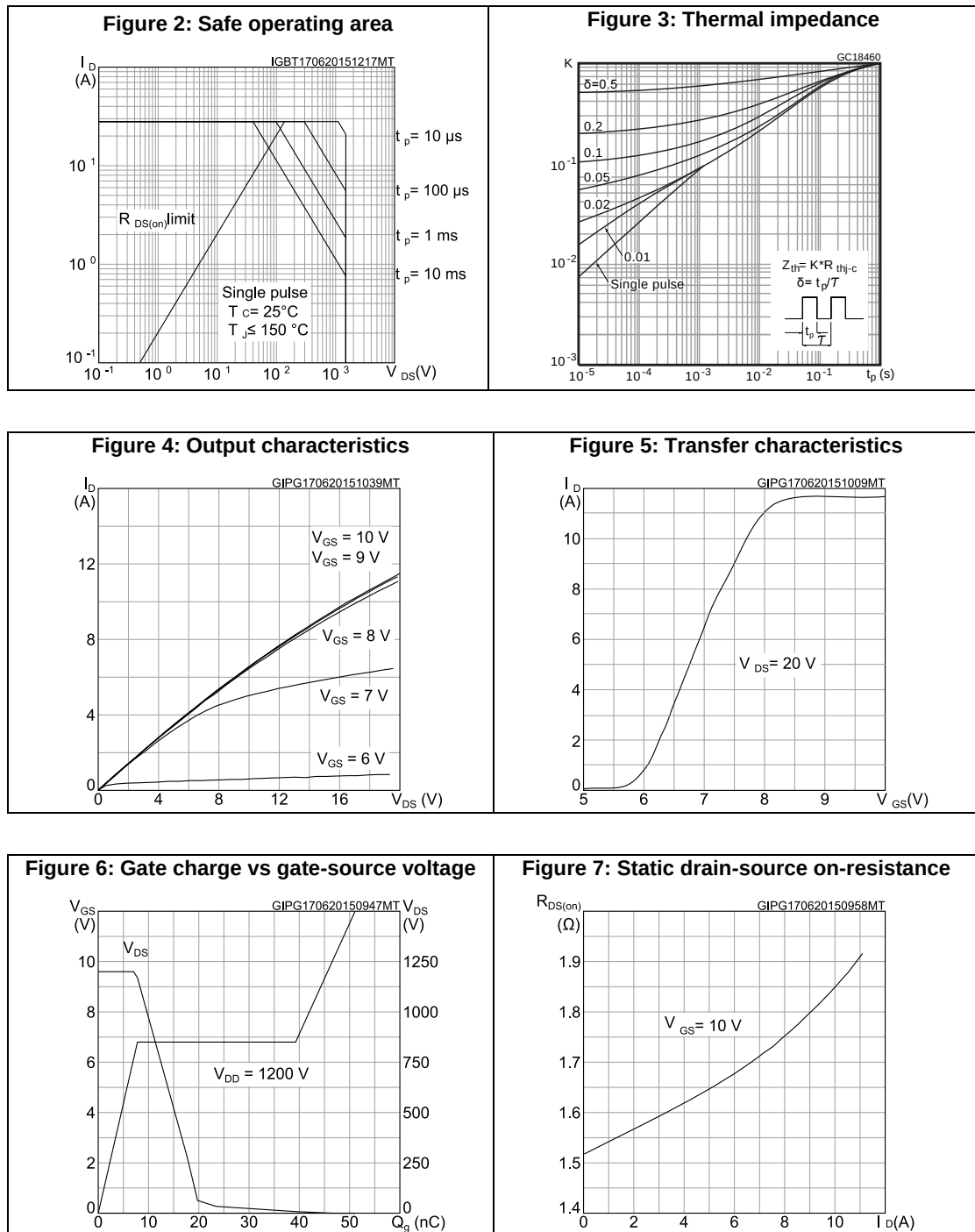


Figure 8: Capacitance variation

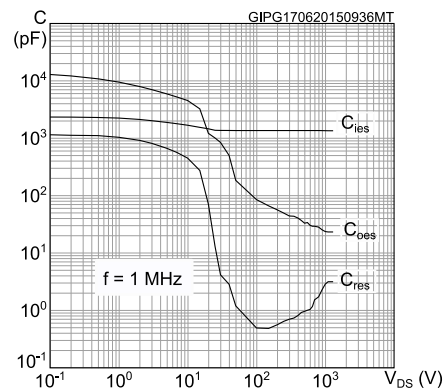


Figure 9: Output capacitance stored energy

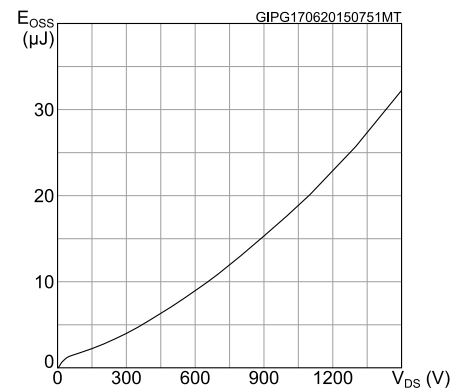


Figure 10: Normalized gate threshold voltage vs temperature

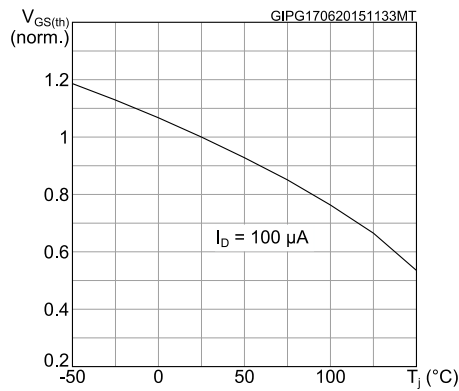


Figure 11: Normalized on-resistance vs temperature

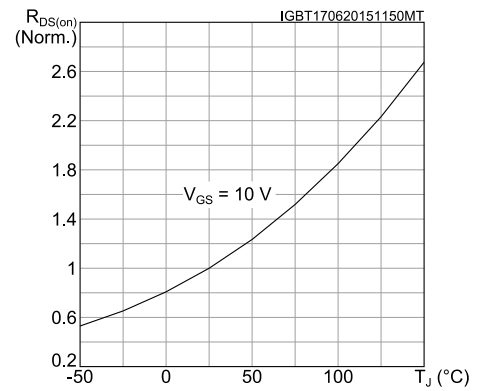
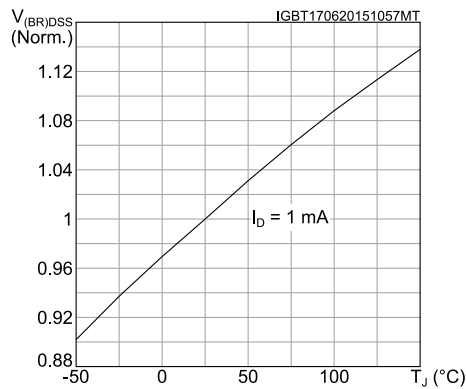
Figure 12: Normalized $V_{(BR)DSS}$ vs temperature

Figure 13: Source-drain diode forward characteristics

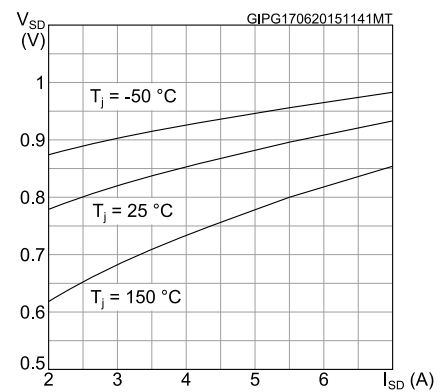
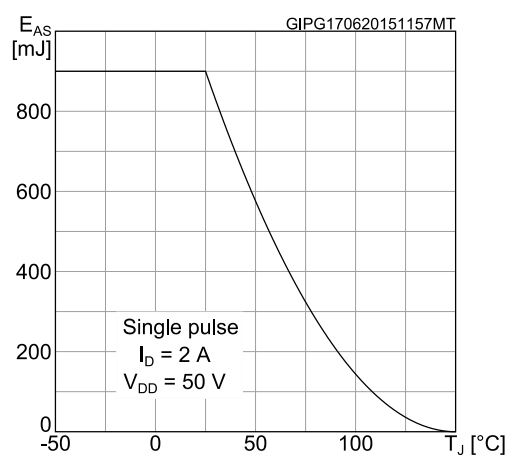
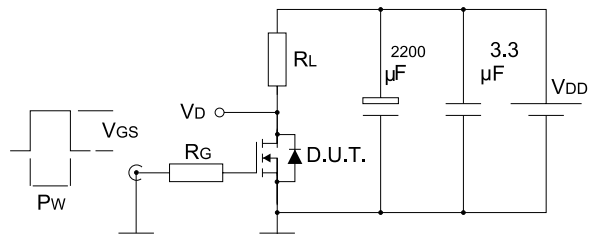


Figure 14: Maximum avalanche energy vs T_J 

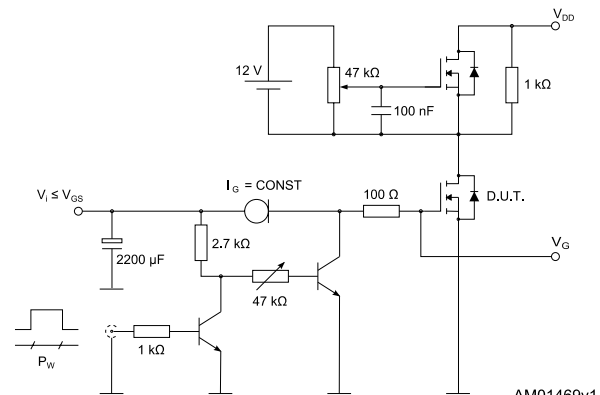
3 Test circuits

Figure 15: Switching times test circuit for resistive load



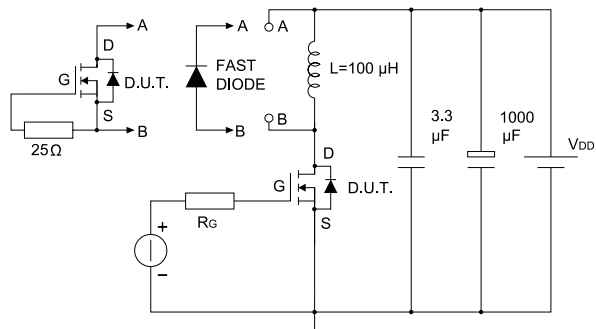
AM01468v1

Figure 16: Gate charge test circuit



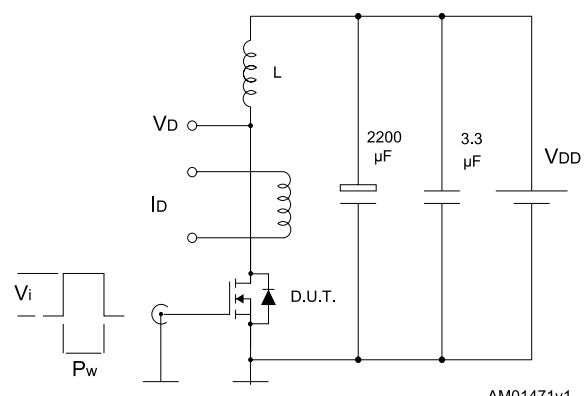
AM01469v1

Figure 17: Test circuit for inductive load switching and diode recovery times



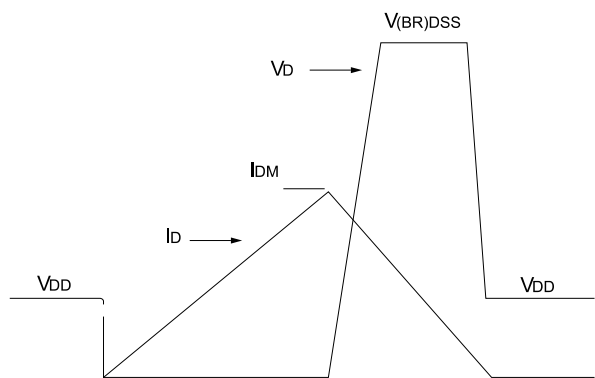
AM01470v1

Figure 18: Unclamped inductive load test circuit



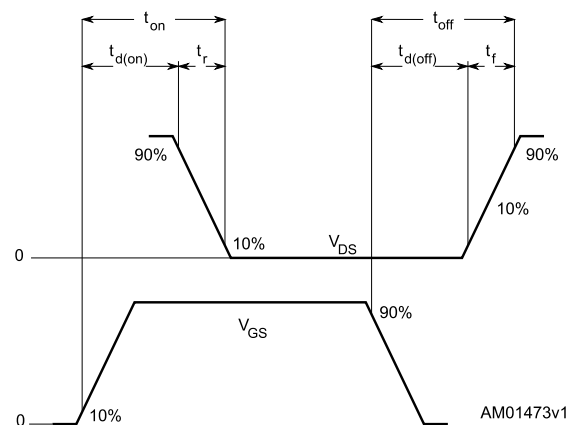
AM01471v1

Figure 19: Unclamped inductive waveform



AM01472v1

Figure 20: Switching time waveform



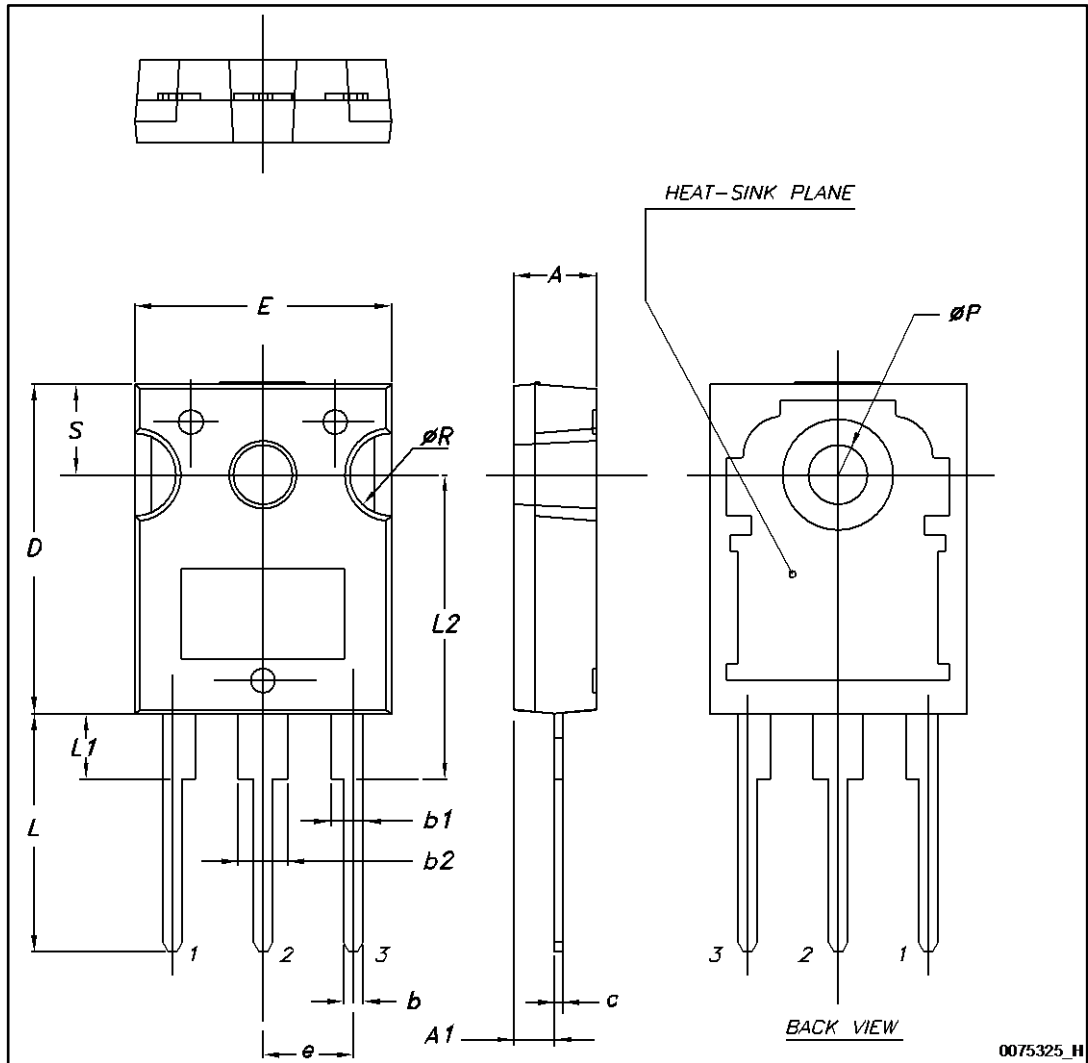
AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 TO-247 package information

Figure 21: TO-247 package outline



0075325_H

Table 10: TO-247 package mechanical data

Dim.	mm.		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70

5 Revision history

Table 11: Document revision history

Date	Revision	Changes
11-May-2015	1	First release.
30-Jun-2015	2	Updated title and features in cover page. Updated Section 4: "Electrical ratings" , Section 5: "Electrical characteristics" . Added Section 5.1: "Electrical characteristics (curves)" . Minor text changes.
07-Jul-2015	3	Updated Section 5.1: "Electrical characteristics (curves)" . Minor text changes.

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2015 STMicroelectronics – All rights reserved