



# STD6NF10 STU6NF10

N-channel 100 V, 0.22  $\Omega$ , 6 A, DPAK, IPAK  
low gate charge STripFET™ Power MOSFET

## Features

| Type     | V <sub>DSS</sub> | R <sub>DS(on)</sub> max | I <sub>D</sub> |
|----------|------------------|-------------------------|----------------|
| STD6NF10 | 100 V            | < 0.250 $\Omega$        | 6 A            |
| STU6NF10 | 100 V            | < 0.250 $\Omega$        | 6 A            |

- Exceptional dv/dt capability
- 100% avalanche tested

## Application

- Switching applications

## Description

This Power MOSFET series realized with STMicroelectronics unique STripFET process has specifically been designed to minimize input capacitance and gate charge. It is therefore suitable as primary switch in advanced high-efficiency, high-frequency isolated DC-DC converters for telecom and computer applications. It is also intended for any applications with low gate drive requirements.

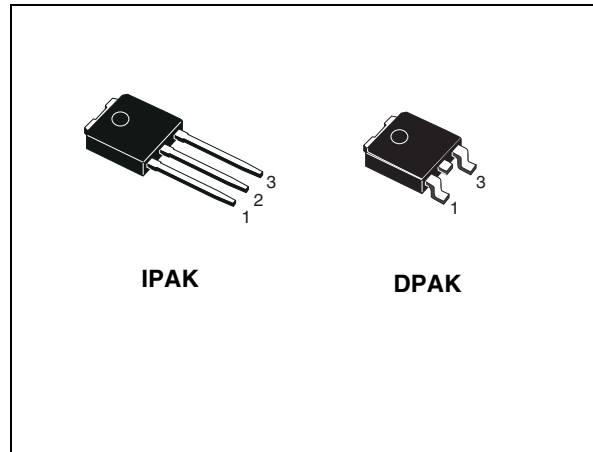


Figure 1. Internal schematic diagram

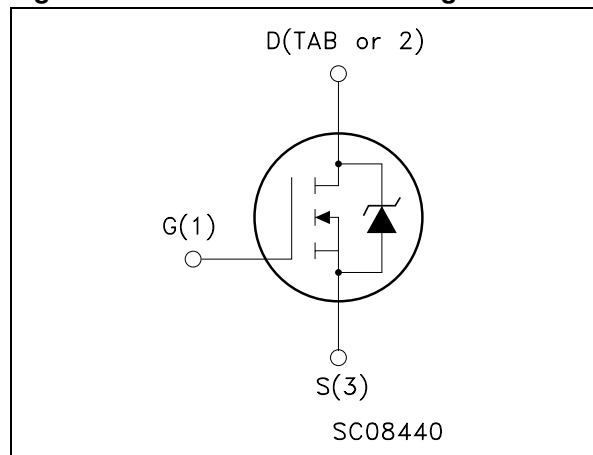


Table 1. Device summary

| Order codes | Marking | Package | Packaging     |
|-------------|---------|---------|---------------|
| STD6NF10T4  | D6NF10  | DPAK    | Tape and reel |
| STU6NF10    | 6NF10   | IPAK    | Tube          |

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

| Symbol         | Parameter                                                         | Value      | Unit                  |
|----------------|-------------------------------------------------------------------|------------|-----------------------|
| $V_{DS}$       | Drain-source voltage ( $V_{GS} = 0$ )                             | 100        | V                     |
| $V_{GS}$       | Gate- source voltage                                              | $\pm 20$   | V                     |
| $I_D$          | Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$  | 6          | A                     |
| $I_D$          | Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$ | 4          | A                     |
| $I_{DM}^{(1)}$ | Drain current (pulsed)                                            | 24         | A                     |
| $P_{tot}$      | Total dissipation at $T_C = 25\text{ }^{\circ}\text{C}$           | 30         | W                     |
|                | Derating factor                                                   | 0.2        | W/ $^{\circ}\text{C}$ |
| $dv/dt^{(2)}$  | Peak diode recovery voltage slope                                 | 40         | V/ns                  |
| $E_{AS}^{(3)}$ | Single pulse avalanche energy                                     | 200        | mJ                    |
| $T_{stg}$      | Storage temperature                                               | -65 to 175 | $^{\circ}\text{C}$    |
| $T_j$          | Max. operating junction temperature                               |            |                       |

1. Pulse width limited by safe operating area.
2.  $I_{SD} \leq 6\text{ A}$ ,  $di/dt \leq 300\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  $T_j \leq T_{JMAX}$
3. Starting  $T_j = 25\text{ }^{\circ}\text{C}$ ,  $I_D = 3\text{ A}$ ,  $V_{DD} = 50\text{ V}$

**Table 3. Thermal data**

| Symbol         | Parameter                                      | Value | Unit                        |
|----------------|------------------------------------------------|-------|-----------------------------|
| $R_{thj-case}$ | Thermal resistance junction-case max           | 5     | $^{\circ}\text{C}/\text{W}$ |
| $R_{thj-amb}$  | Thermal resistance junction-ambient max        | 100   | $^{\circ}\text{C}/\text{W}$ |
| $T_J$          | Maximum lead temperature for soldering purpose | 300   | $^{\circ}\text{C}$          |

## 2 Electrical characteristics

( $T_{CASE} = 25\text{ }^{\circ}\text{C}$  unless otherwise specified)

**Table 4. On/off states**

| Symbol        | Parameter                                        | Test conditions                                                                                       | Min. | Typ. | Max.      | Unit                           |
|---------------|--------------------------------------------------|-------------------------------------------------------------------------------------------------------|------|------|-----------|--------------------------------|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage                   | $I_D = 250\text{ }\mu\text{A}$ , $V_{GS} = 0$                                                         | 100  |      |           | V                              |
| $I_{DSS}$     | Zero gate voltage drain current ( $V_{GS} = 0$ ) | $V_{DS} = \text{max rating}$<br>$V_{DS} = \text{max rating}$ ,<br>$T_C = 125\text{ }^{\circ}\text{C}$ |      |      | 1<br>10   | $\mu\text{A}$<br>$\mu\text{A}$ |
| $I_{GSS}$     | Gate-body leakage current ( $V_{DS} = 0$ )       | $V_{GS} = \pm 20\text{ V}$                                                                            |      |      | $\pm 100$ | nA                             |
| $V_{GS(th)}$  | Gate threshold voltage                           | $V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$                                                    | 2    |      | 4         | V                              |
| $R_{DS(on)}$  | Static drain-source on resistance                | $V_{GS} = 10\text{ V}$ , $I_D = 3\text{ A}$                                                           |      | 0.22 | 0.25      | $\Omega$                       |

**Table 5. Dynamic**

| Symbol                                        | Parameter                                                               | Test conditions                                                                                                                         | Min. | Typ.               | Max. | Unit                 |
|-----------------------------------------------|-------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------|------|--------------------|------|----------------------|
| $g_{fs}^{(1)}$                                | Forward transconductance                                                | $V_{DS} = > I_{D(on)} \times R_{DS(on)max}$ , $I_D = 3\text{ A}$                                                                        |      | 34                 |      | S                    |
| $C_{iss}$<br>$C_{oss}$<br>$C_{rss}$           | Input capacitance<br>Output capacitance<br>Reverse transfer capacitance | $V_{DS} = 25\text{ V}$ , $f = 1\text{ MHz}$ ,<br>$V_{GS} = 0$                                                                           |      | 280<br>45<br>20    |      | pF<br>pF<br>pF       |
| $t_{d(on)}$<br>$t_r$<br>$t_{d(off)}$<br>$t_f$ | Turn-on delay time<br>Rise time<br>Turn-off delay time<br>Fall time     | $V_{DD} = 50\text{ V}$ , $I_D = 3\text{ A}$<br>$R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$<br>(see <a href="#">Figure 13</a> )   |      | 6<br>10<br>20<br>3 |      | ns<br>ns<br>ns<br>ns |
| $Q_g$<br>$Q_{gs}$<br>$Q_{gd}$                 | Total gate charge<br>Gate-source charge<br>Gate-drain charge            | $V_{DD} = 80\text{ V}$ , $I_D = 6\text{ A}$ ,<br>$V_{GS} = 10\text{ V}$ , $R_G = 4.7\text{ }\Omega$<br>(see <a href="#">Figure 14</a> ) |      | 10<br>2.5<br>4     | 14   | nC<br>nC<br>nC       |

1. Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

**Table 6. Source drain diode**

| Symbol                            | Parameter                                                                    | Test conditions                                                                                                                                                | Min. | Typ.           | Max.    | Unit          |
|-----------------------------------|------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------|------|----------------|---------|---------------|
| $I_{SD}$<br>$I_{SDM}^{(1)}$       | Source-drain current<br>Source-drain current<br>(pulsed)                     |                                                                                                                                                                |      |                | 6<br>24 | A<br>A        |
| $V_{SD}^{(2)}$                    | Forward on voltage                                                           | $I_{SD} = 6\text{ A}$ , $V_{GS} = 0$                                                                                                                           |      |                | 1.3     | V             |
| $t_{rr}$<br>$Q_{rr}$<br>$I_{RRM}$ | Reverse recovery time<br>Reverse recovery charge<br>Reverse recovery current | $I_{SD} = 6\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ ,<br>$V_{DD} = 10\text{ V}$ , $T_j = 150\text{ }^\circ\text{C}$<br>(see <a href="#">Figure 15</a> ) |      | 70<br>175<br>5 |         | ns<br>nC<br>A |

1. Pulse width limited by safe operating area.

2. Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

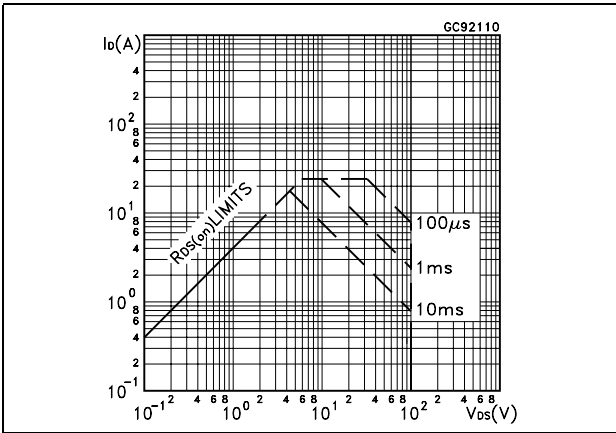


Figure 3. Thermal impedance

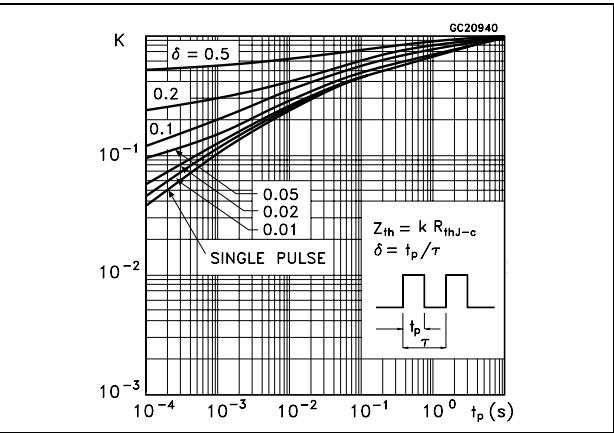


Figure 4. Output characteristics

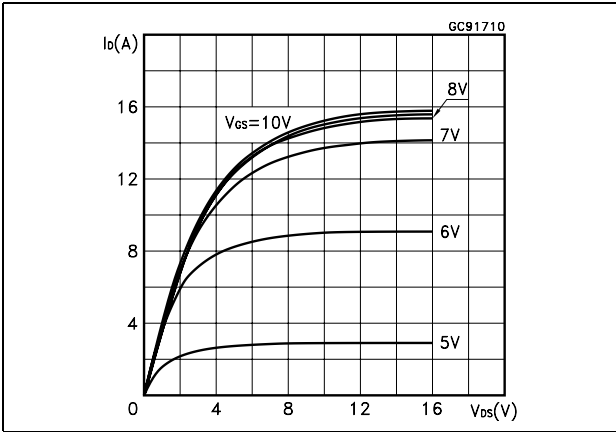


Figure 5. Transfer characteristics

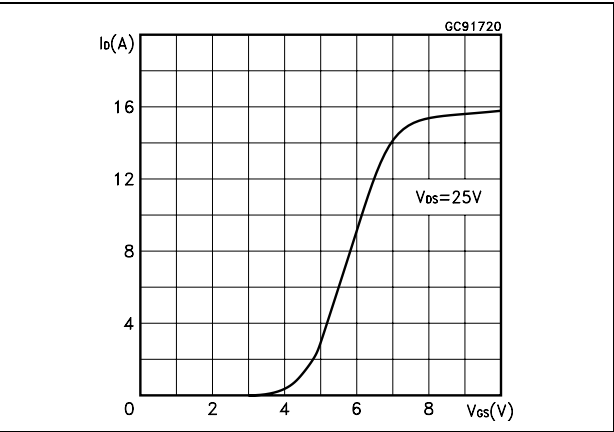


Figure 6. Transconductance

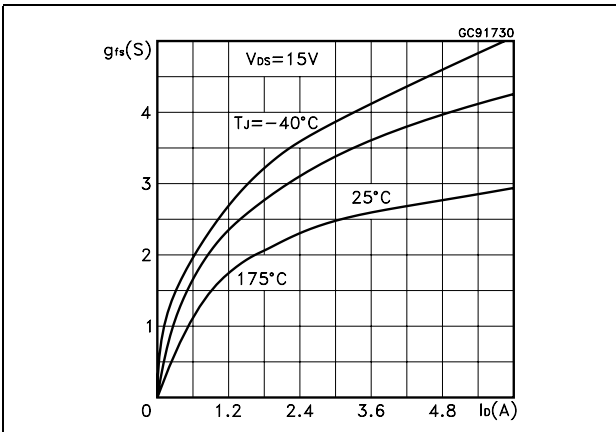


Figure 7. Static drain-source on resistance

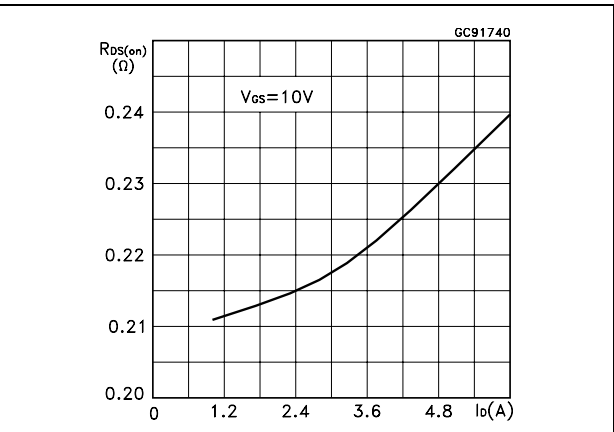


Figure 8. Gate charge vs. gate-source voltage Figure 9. Capacitance variations

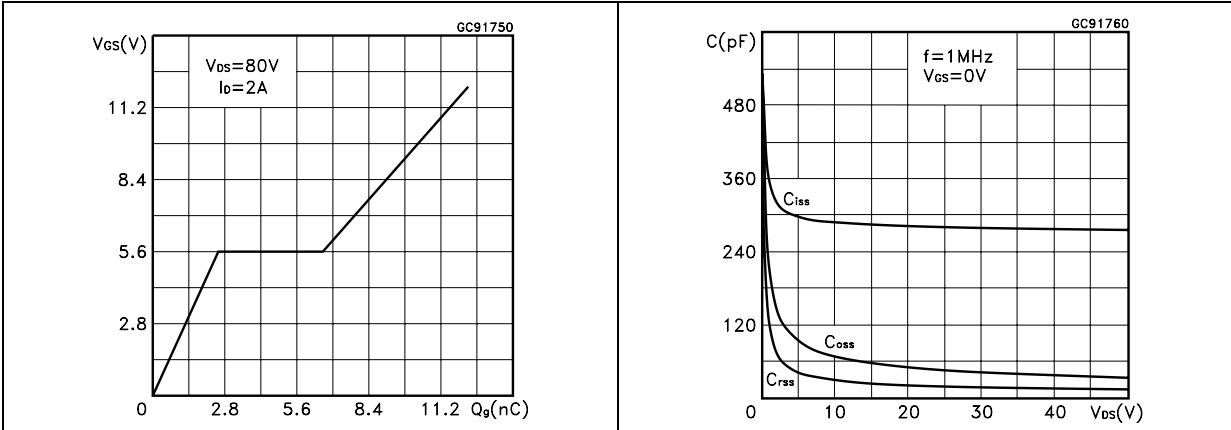


Figure 10. Normalized gate threshold voltage vs. temperature Figure 11. Normalized on resistance vs. temperature

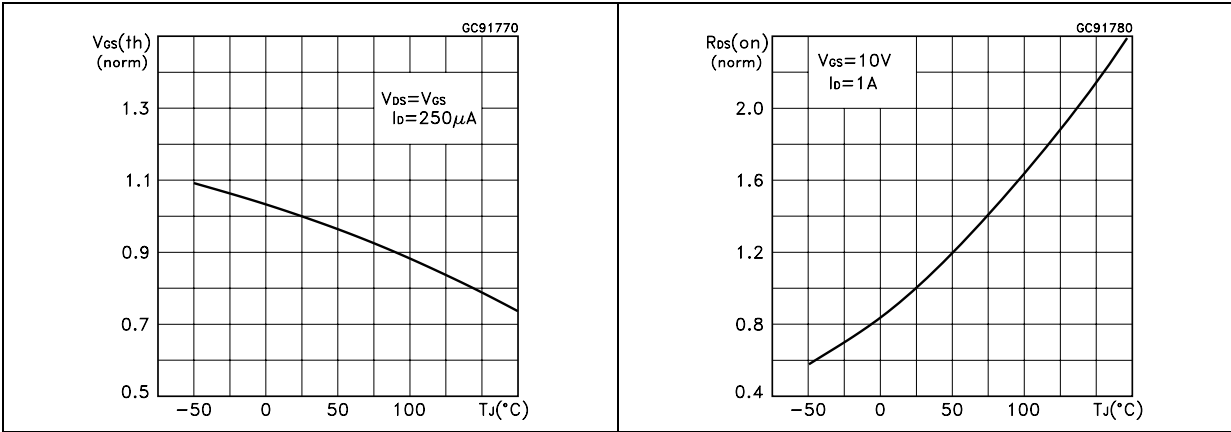
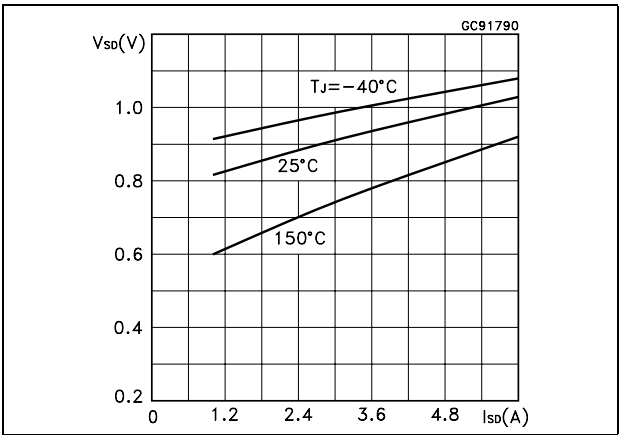
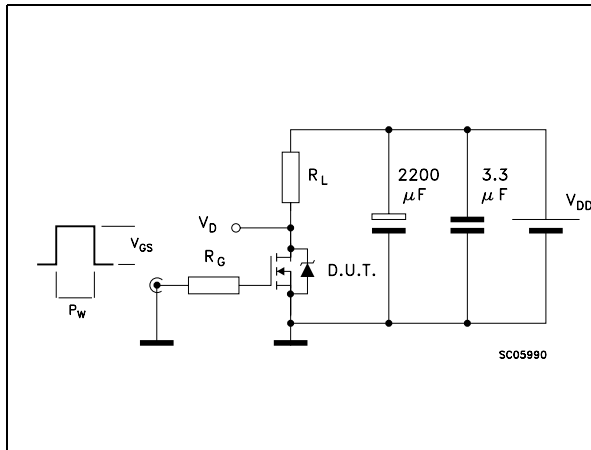


Figure 12. Source-drain diode forward characteristics

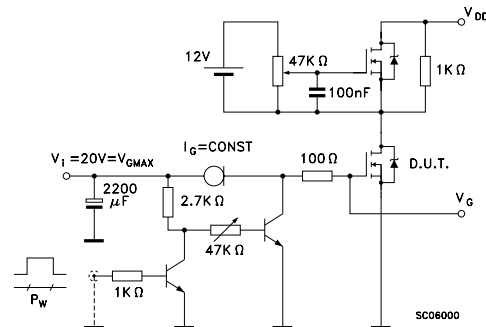


### 3 Test circuits

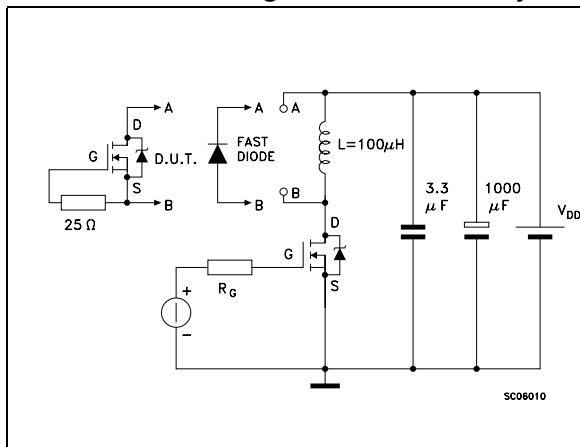
**Figure 13. Switching times test circuit for resistive load**



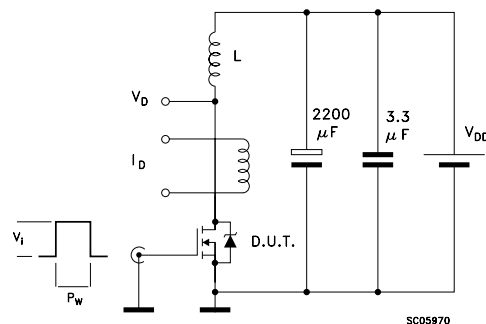
**Figure 14. Gate charge test circuit**



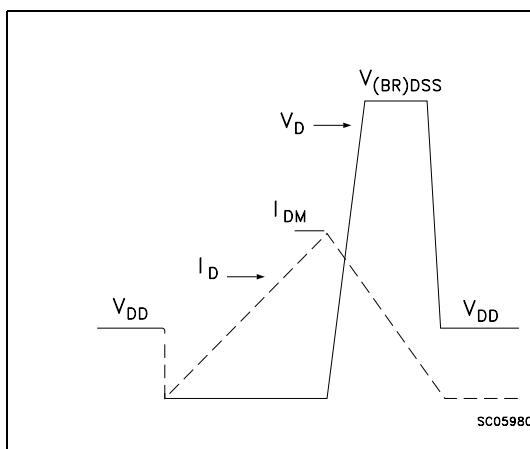
**Figure 15. Test circuit for inductive load switching and diode recovery times**



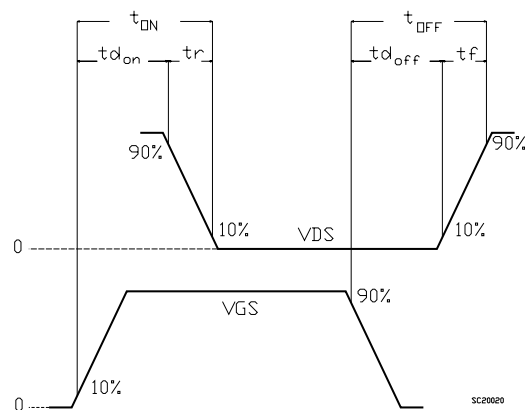
**Figure 16. Unclamped Inductive load test circuit**



**Figure 17. Unclamped inductive waveform**



**Figure 18. Switching time waveform**



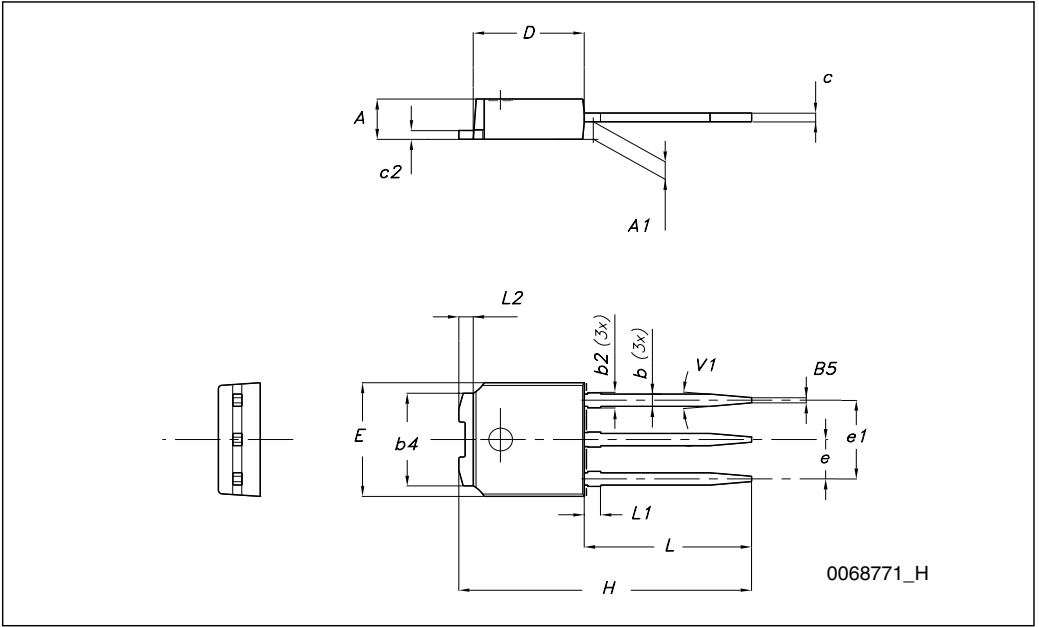


## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

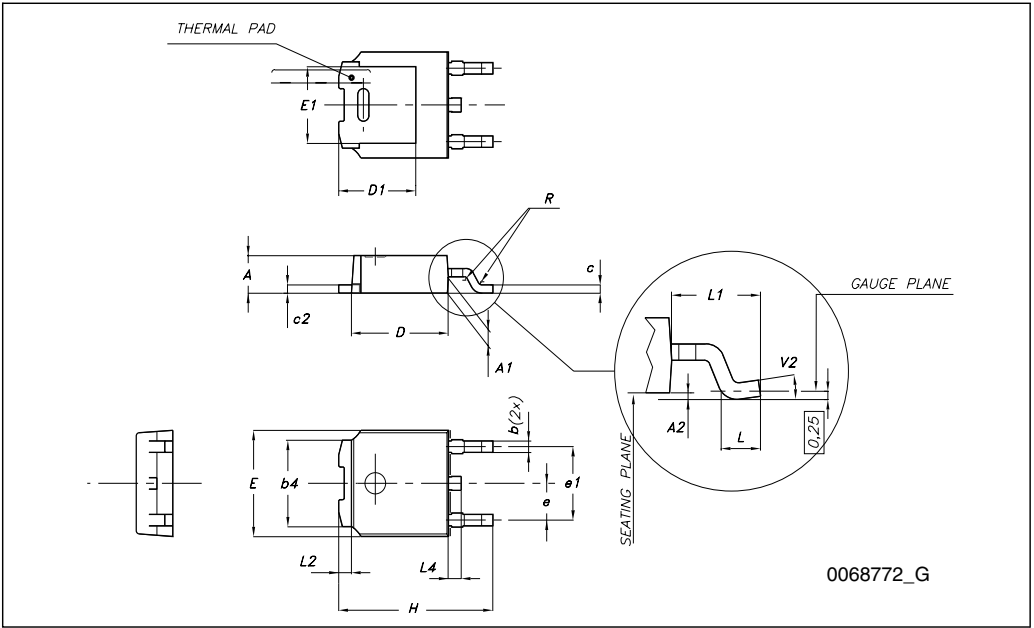
TO-251 (IPAK) mechanical data

| DIM. | mm.  |       |      |
|------|------|-------|------|
|      | min. | typ   | max. |
| A    | 2.20 |       | 2.40 |
| A1   | 0.90 |       | 1.10 |
| b    | 0.64 |       | 0.90 |
| b2   |      |       | 0.95 |
| b4   | 5.20 |       | 5.40 |
| c    | 0.45 |       | 0.60 |
| c2   | 0.48 |       | 0.60 |
| D    | 6.00 |       | 6.20 |
| E    | 6.40 |       | 6.60 |
| e    |      | 2.28  |      |
| e1   | 4.40 |       | 4.60 |
| H    |      | 16.10 |      |
| L    | 9.00 |       | 9.40 |
| (L1) | 0.80 |       | 1.20 |
| L2   |      | 0.80  |      |
| V1   |      | 10 °  |      |



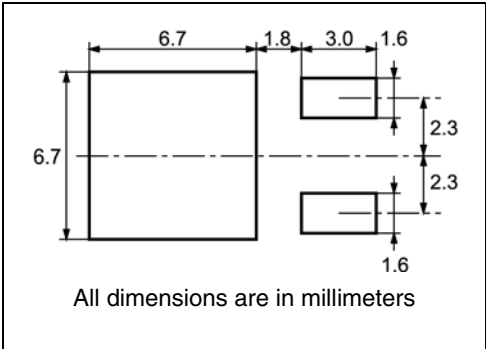
TO-252 (DPAK) mechanical data

| DIM. | mm.  |      |       |
|------|------|------|-------|
|      | min. | typ  | max.  |
| A    | 2.20 |      | 2.40  |
| A1   | 0.90 |      | 1.10  |
| A2   | 0.03 |      | 0.23  |
| b    | 0.64 |      | 0.90  |
| b4   | 5.20 |      | 5.40  |
| c    | 0.45 |      | 0.60  |
| c2   | 0.48 |      | 0.60  |
| D    | 6.00 |      | 6.20  |
| D1   |      | 5.10 |       |
| E    | 6.40 |      | 6.60  |
| E1   |      | 4.70 |       |
| e    |      | 2.28 |       |
| e1   | 4.40 |      | 4.60  |
| H    | 9.35 |      | 10.10 |
| L    | 1    |      |       |
| L1   |      | 2.80 |       |
| L2   |      | 0.80 |       |
| L4   | 0.60 |      | 1     |
| R    |      | 0.20 |       |
| V2   | 0°   |      | 8°    |

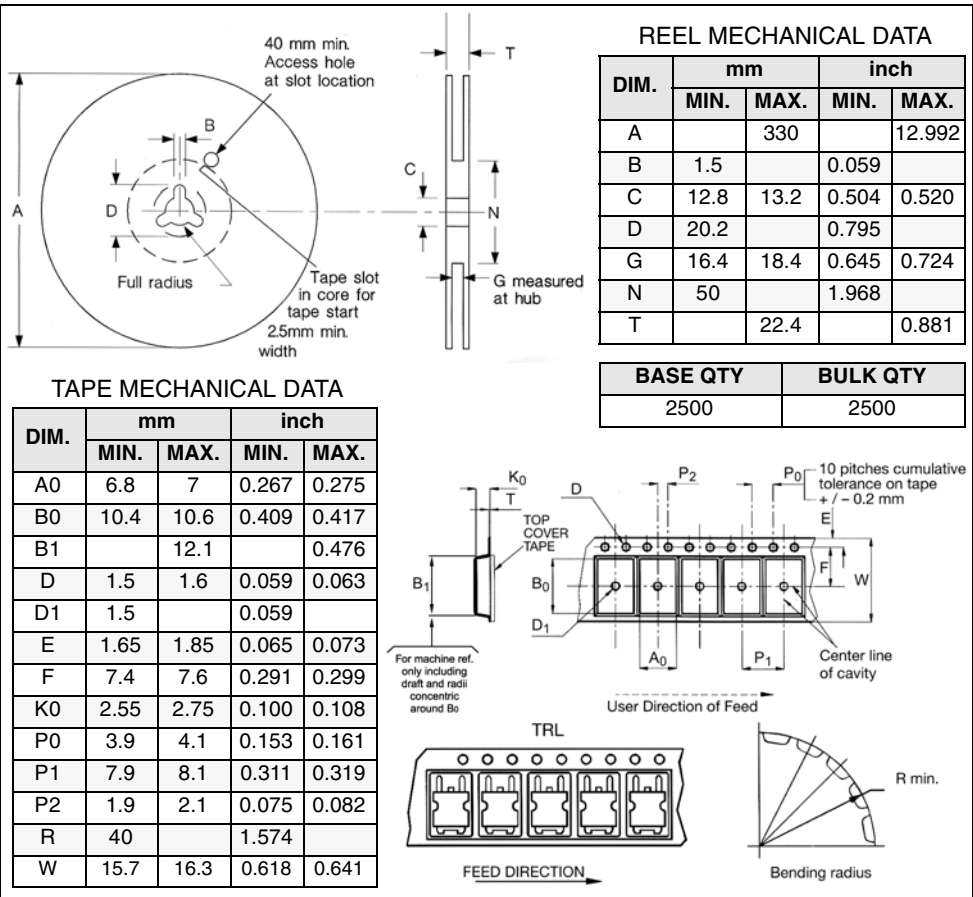


5 Packing mechanical data

DPAK FOOTPRINT



TAPE AND REEL SHIPMENT



## 6 Revision history

**Table 7. Document revision history**

| Date        | Revision | Changes                                                                                                                                          |
|-------------|----------|--------------------------------------------------------------------------------------------------------------------------------------------------|
| 21-Jun-2004 | 3        | Complete version                                                                                                                                 |
| 20-Jul-2006 | 4        | New template, no content change                                                                                                                  |
| 16-Sep-2008 | 5        | Corrected part number: STU6NF10                                                                                                                  |
| 19-Nov-2008 | 6        | Marking label in <a href="#">Table 1</a> for the device in IPAK has been updated.<br>$I_{GSS}$ value in <a href="#">Table 4</a> has been updated |

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