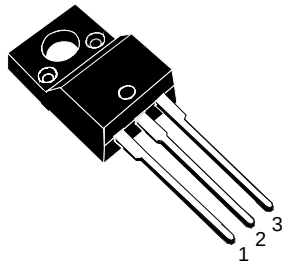
STFU10NK60Z

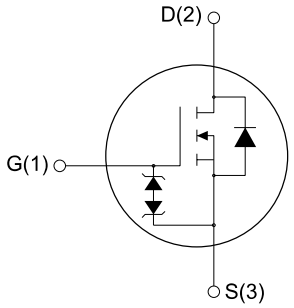
N-channel 600 V, 0.68 Ω typ., 10 A, SuperMESH™ Power MOSFET in a TO-220FP ultra narrow leads package

Datasheet - production data



TO-220FP
ultra narrow leads

Figure 1: Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D	P_{tot}
STFU10NK60Z	600 V	0.75 Ω	10 A	35 W

- Extremely high dv/dt capability
- 100% avalanche tested
- Gate charge minimized
- Zener-protected

Applications

- Switching applications

Description

This high voltage device is a Zener-protected N-channel Power MOSFET developed using the SuperMESH™ technology by STMicroelectronics, an optimization of the well-established PowerMESH™. In addition to a significant reduction in on-resistance, this device is designed to ensure a high level of dv/dt capability for the most demanding applications.

Table 1: Device summary

Order code	Marking	Package	Packaging
STFU10NK60Z	10NK60Z	TO-220FP ultra narrow leads	Tube

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	600	V
V_{GS}	Gate-source voltage	±30	V
I_D(1)	Drain current (continuous) at T_C= 25 °C	10	A
I_D(1)	Drain current (continuous) at T_C = 100 °C	5.7	A
I_{DM}(2)	Drain current (pulsed)	36	A
P_{TOT}	Total dissipation at T_C = 25 °C	35	W
ESD	Gate-source, human body model (R = 1.5 kΩ, C = 100 pF)	4	kV
dv/dt(3)	Peak diode recovery voltage slope	4.5	V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1s; T_C= 25 °C)	2500	V
T_j	Operation junction temperature range	-55 to 150	°C
T_{stg}	Storage temperature range		

Notes:

(1)Limited by package

(2)Pulse width limited by safe operating area

(3)I_{SD} < 10 A , di/dt < 200 A/µs , V_{DD} = 80 % $V_{(BR)DSS}$

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max	3.6	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient max	62.5	°C/W

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or non-repetitive (pulse width limited by T_J max)	10	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	300	mJ

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 5: On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 250 µA	600			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 600 V			1	µA
		V_{GS} = 0 V, V_{DS} = 600 V, T_C = 125 °C(1)			50	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = +20 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on- resistance	V_{GS} = 10 V, I_D = 4.5 A		0.68	0.75	Ω

Notes:

(1)Defined by design, not subject to production test.

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz	-	1370	-	pF
C_{oss}	Output capacitance		-	156	-	pF
C_{rss}	Reverse transfer capacitance		-	37	-	pF
$C_{oss\ eq}$(1)	Equivalent output capacitance	V_{GS}= 0 V, V_{DS}= 0 to 480 V	-	93	-	pF
Q_g	Total gate charge	V_{DD} = 480 V, I_D = 8 A, V_{GS} = 10 V (see *Figure 13: "Test circuit for gate charge behavior"*)	-	48	-	nC
Q_{gs}	Gate-source charge		-	8	-	nC
Q_{gd}	Gate-drain charge		-	25	-	nC

Notes:

(1)$C_{oss\ eq}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80%

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 300 V, I_D = 4 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 12: "Test circuit for resistive load switching times"* and *Figure 17: "Switching time waveform"*)	-	20	-	ns
t_r	Rise time		-	20	-	ns
$t_{d(off)}$	Turn-off delay time		-	55	-	ns
t_f	Fall time		-	30	-	ns

Table 8: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}(1)	Source-drain current		-		10	V
I_{SDM}(2)	Source-drain current (pulsed)		-		36	A
V_{SD}(3)	Forward on voltage	I_{SD}= 10 A, V_{GS} = 0 V	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 8 A, di/dt = 100 A/µs, V_{DD} = 40 V , T_J = 150 °C (see *Figure 14: "Test circuit for inductive load switching and diode recovery times"*)	-	570		ns
Q_{rr}	Reverse recovery charge		-	4.1		µC
I_{RRM}	Reverse recovery current		-	15		A

Notes:

(1)Limited by package

(2)Pulse width limited by safe operating area

(3)Pulsed: pulse duration = 300 µs, duty cycle 1.5%

Table 9: Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	I_{GS} = ±1 mA, I_D = 0 A	±30	-	-	V

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

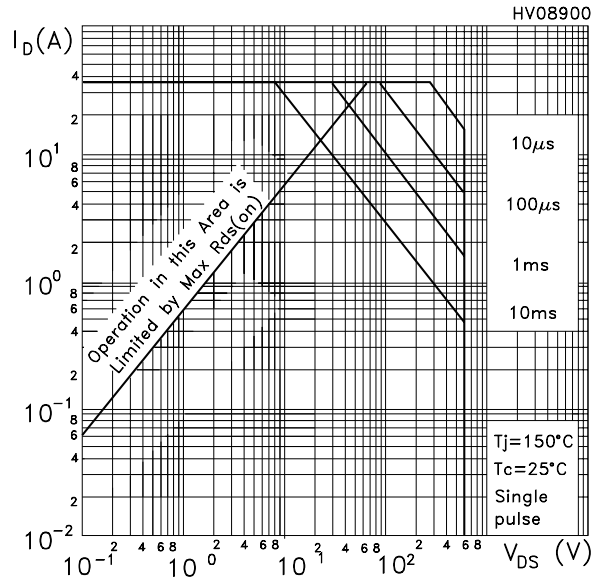


Figure 3: Thermal impedance

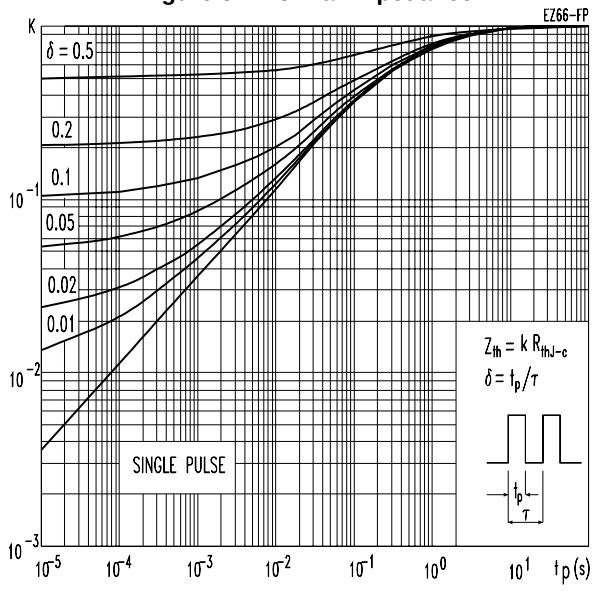


Figure 4: Output characteristics

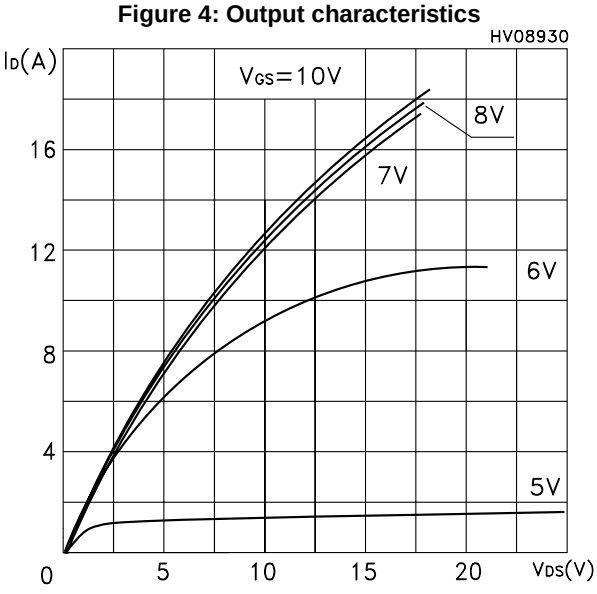


Figure 5: Gate charge vs gate-source voltage

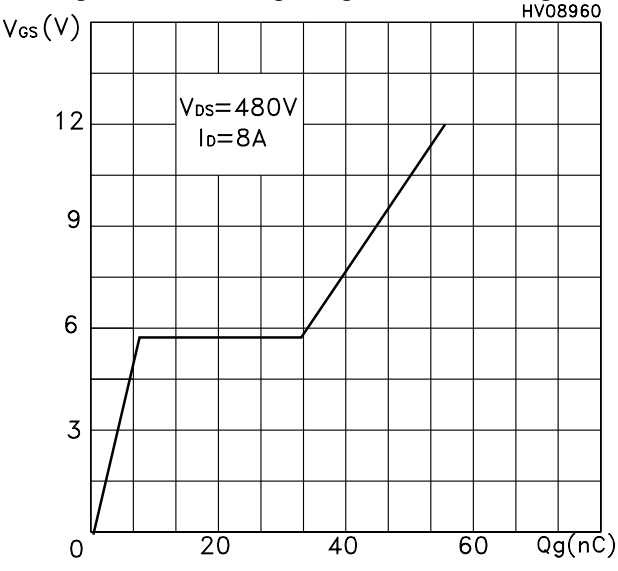


Figure 6: Capacitance variations

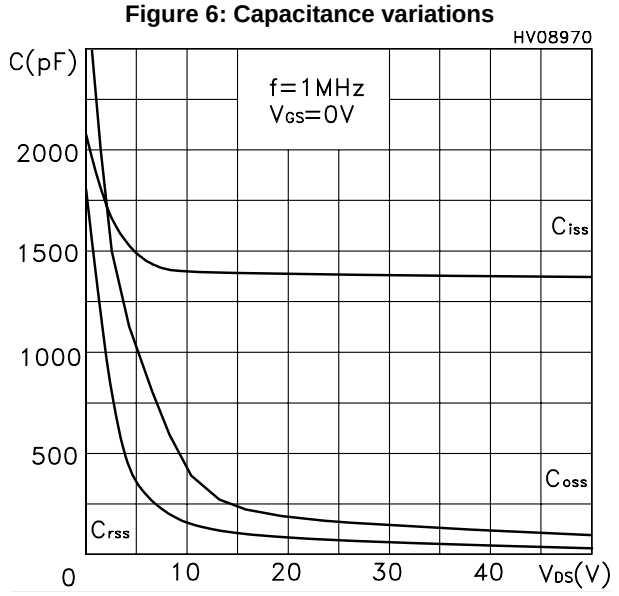


Figure 7: Static drain-source on-resistance

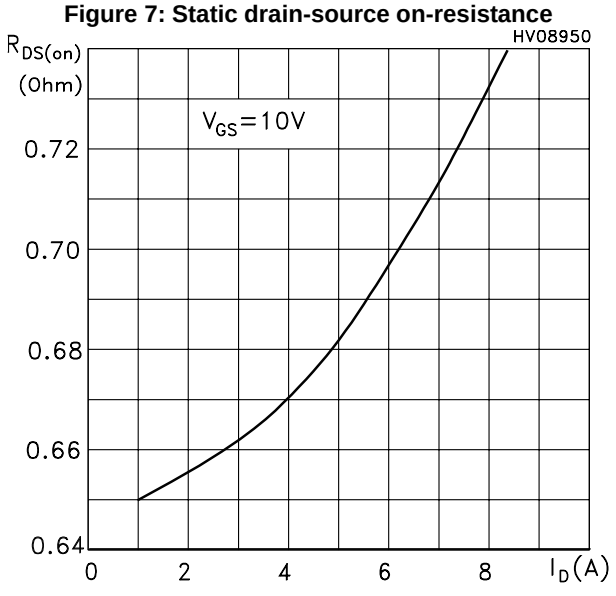


Figure 8: Normalized gate threshold voltage vs temperature

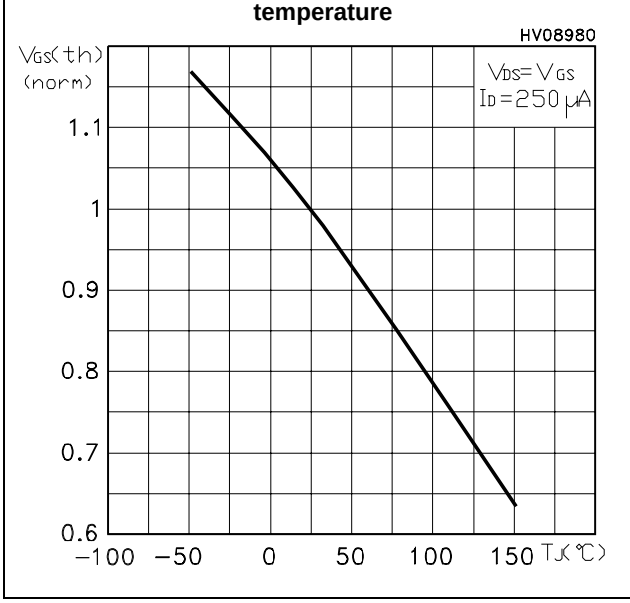


Figure 9: Normalized on-resistance vs temperature

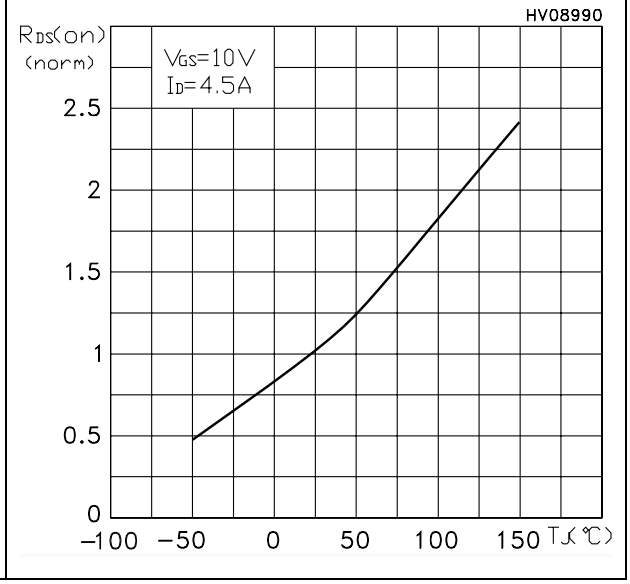


Figure 10: Source-drain diode forward characteristics

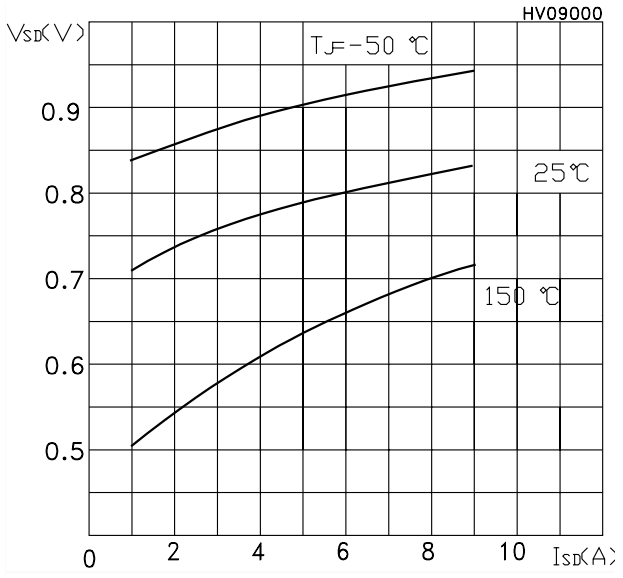
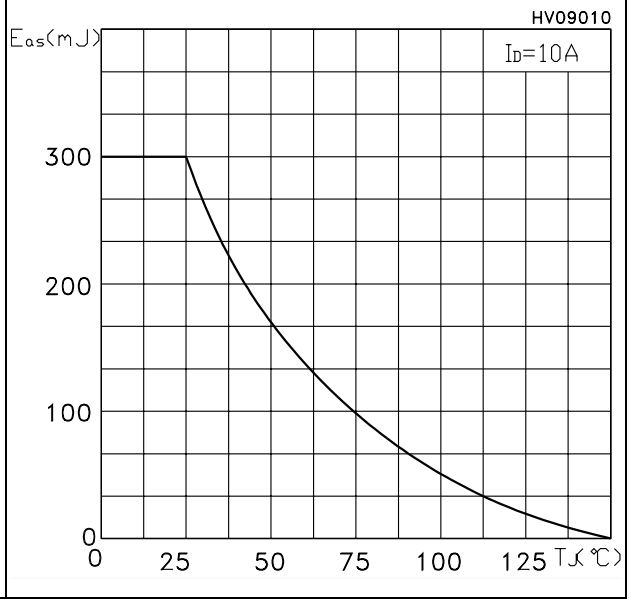


Figure 11: Maximum avalanche energy



3 Test circuits

Figure 12: Test circuit for resistive load switching times

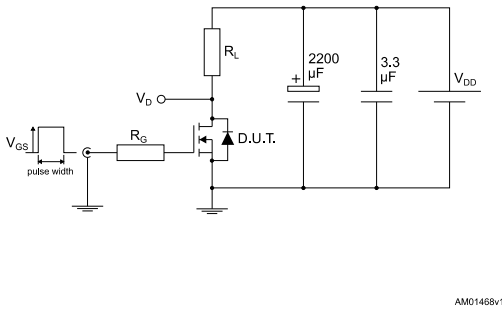


Figure 13: Test circuit for gate charge behavior

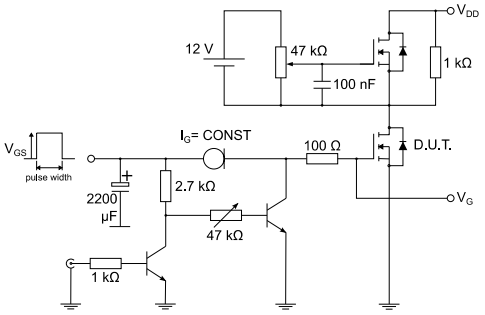


Figure 14: Test circuit for inductive load switching and diode recovery times

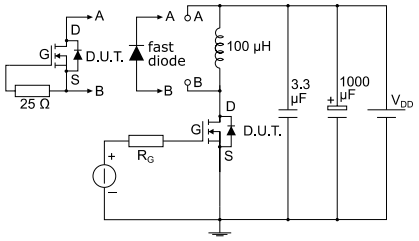


Figure 15: Unclamped inductive load test circuit

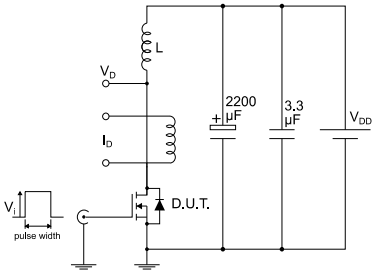


Figure 16: Unclamped inductive waveform

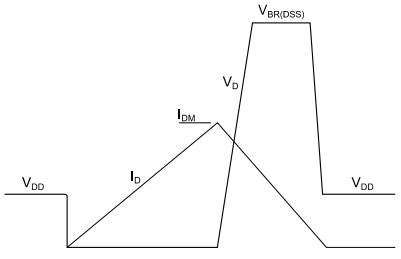
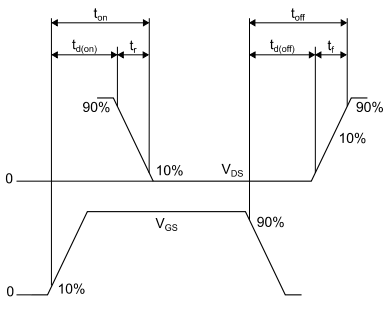


Figure 17: Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 TO-220FP ultra narrow leads package information

Figure 18: TO-220FP ultra narrow leads package outline

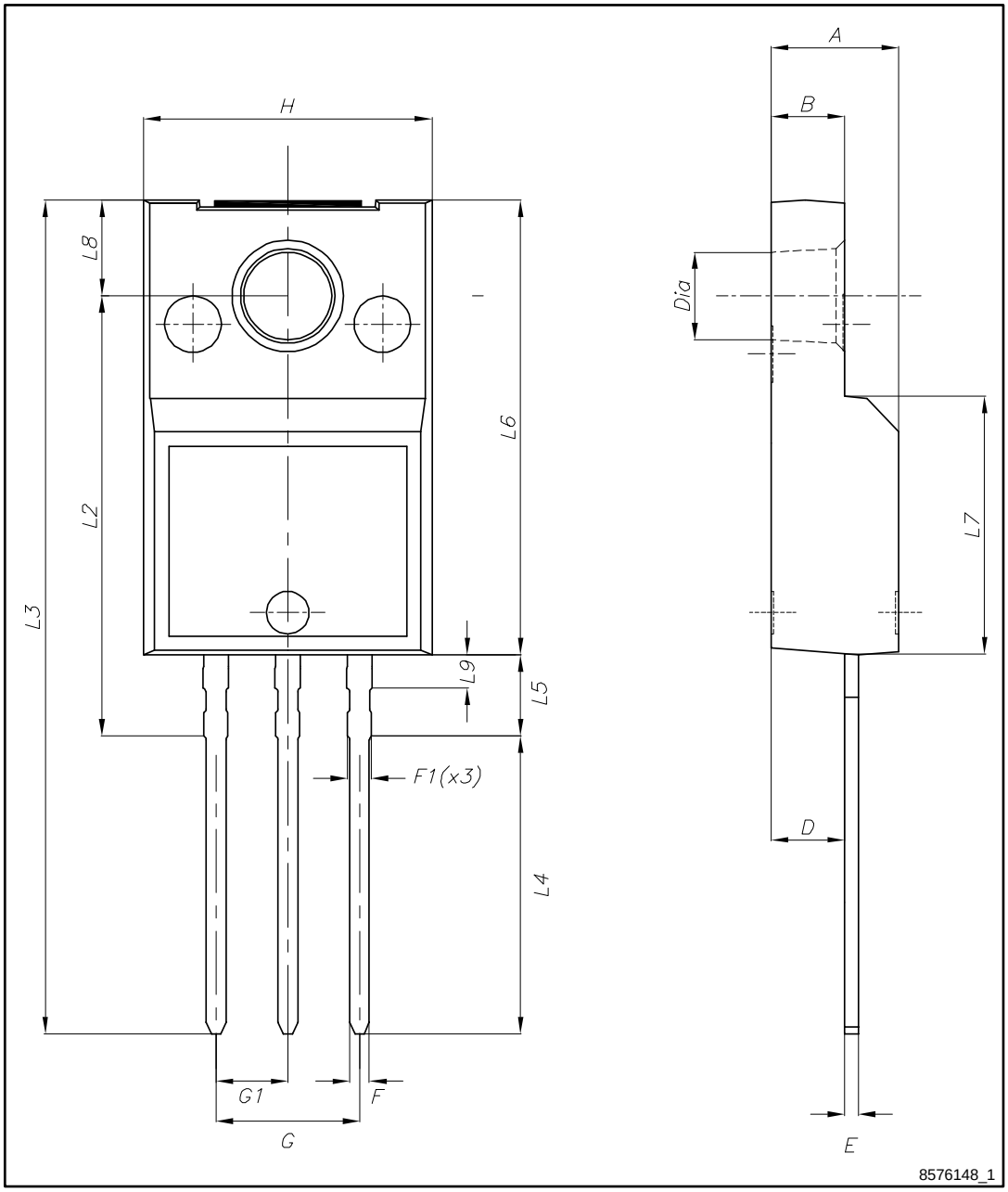


Table 10: TO-220FP ultra narrow leads mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
B	2.50		2.70
D	2.50		2.75
E	0.45		0.60
F	0.65		0.75
F1	-		0.90
G	4.95		5.20
G1	2.40	2.54	2.70
H	10.00		10.40
L2	15.10		15.90
L3	28.50		30.50
L4	10.20		11.00
L5	2.50		3.10
L6	15.60		16.40
L7	9.00		9.30
L8	3.20		3.60
L9	-		1.30
Dia.	3.00		3.20

5 Revision history

Table 11: Document revision history

Date	Revision	Changes
07-Jan-2016	1	Initial release.
12-Sep-2016	2	Document status changed from preliminary to production data. Minor text changes.
05-Dec-2016	3	Updated Features on cover page. Updated *Table 2: "Absolute maximum ratings"* and added *Table 4: "Avalanche characteristics"*. Updated *Table 5: "On /off states"*, *Table 6: "Dynamic"*, *Table 8: "Source drain diode"* and *Table 9: "Gate-source Zener diode"*. Minor text changes

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