



IMPORTANT NOTICE

10 December 2015

1. Global joint venture starts operations as WeEn Semiconductors

Dear customer,

As from November 9th, 2015 NXP Semiconductors N.V. and Beijing JianGuang Asset Management Co. Ltd established Bipolar Power joint venture (JV), **WeEn Semiconductors**, which will be used in future Bipolar Power documents together with new contact details.

In this document where the previous NXP references remain, please use the new links as shown below.

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Thank you for your cooperation and understanding,

WeEn Semiconductors





BTA201W-800E

3Q Hi-Com triac

13 August 2014

Product data sheet

1. General description

Planar passivated high commutation triac in a SOT223 surface mounted plastic package. This "series E" triac balances the requirements of commutation performance and gate sensitivity and is intended for interfacing with low power drivers and logic ICs including microcontrollers.

2. Features and benefits

- 3Q technology for improved noise immunity
- Direct triggering from low power drivers and logic ICs
- High commutation capability with sensitive gate
- High immunity to false turn-on by dV/dt
- High voltage capability
- Planar passivated for voltage ruggedness and reliability
- Sensitive gate for easy logic level triggering
- Surface mountable package
- Triggering in three quadrants only

3. Applications

- General purpose motor control
- Small loads in washing machines
- Solenoid drivers

4. Quick reference data

Table 1. Quick reference data

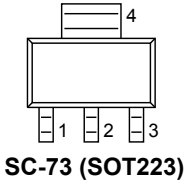
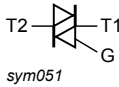
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	-	800	V
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(\text{init})} = 25\text{ }^{\circ}\text{C}$; $t_p = 20\text{ ms}$; Fig. 4 ; Fig. 5	-	-	12.5	A
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{sp} \leq 106\text{ }^{\circ}\text{C}$; Fig. 1 ; Fig. 2 ; Fig. 3	-	-	1	A
Static characteristics						
I_{GT}	gate trigger current	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G+; $T_j = 25\text{ }^{\circ}\text{C}$; Fig. 9	1	-	10	mA



Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		$V_D = 12\text{ V}; I_T = 0.1\text{ A}; T_2+ G-;$ $T_j = 25\text{ }^\circ\text{C};$ Fig. 9	1	-	10	mA
		$V_D = 12\text{ V}; I_T = 0.1\text{ A}; T_2- G-;$ $T_j = 25\text{ }^\circ\text{C};$ Fig. 9	1	-	10	mA

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	T1	main terminal 1	 <p>SC-73 (SOT223)</p>	 <p>sym051</p>
2	T2	main terminal 2		
3	G	gate		
4	T2	main terminal 2		

6. Ordering information

Table 3. Ordering information

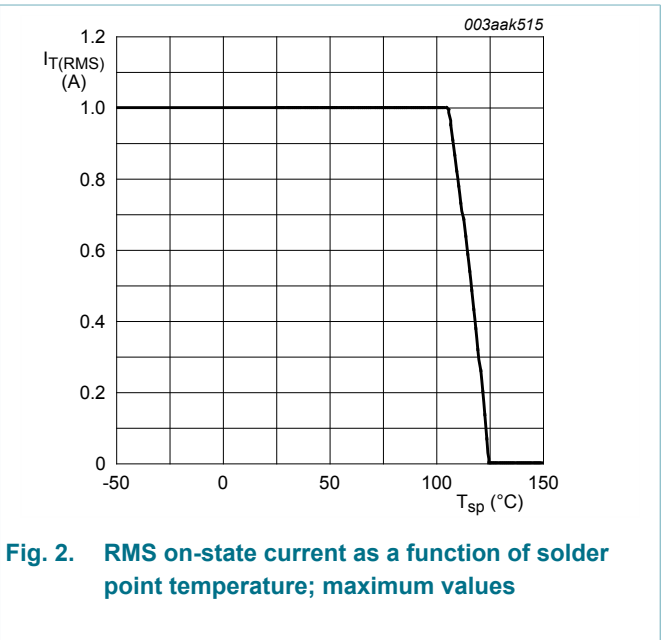
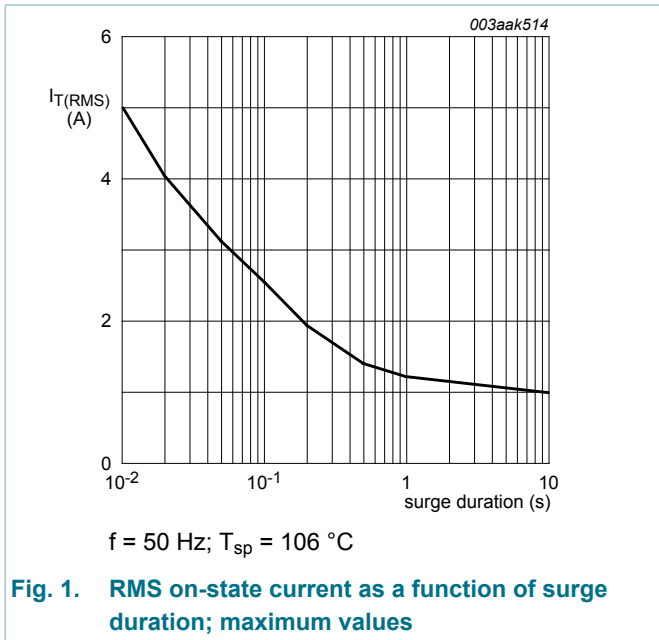
Type number	Package		
	Name	Description	Version
BTA201W-800E	SC-73	plastic surface-mounted package with increased heatsink; 4 leads	SOT223

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{sp} \leq 106\text{ °C}$; Fig. 1 ; Fig. 2 ; Fig. 3	-	1	A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(\text{init})} = 25\text{ °C}$; $t_p = 16.7\text{ ms}$	-	13.7	A
		full sine wave; $T_{j(\text{init})} = 25\text{ °C}$; $t_p = 20\text{ ms}$; Fig. 4 ; Fig. 5	-	12.5	A
I^2t	I^2t for fusing	$t_p = 10\text{ ms}$; SIN	-	0.78	A^2s
dl_T/dt	rate of rise of on-state current	$I_T = 1.5\text{ A}$; $I_G = 0.2\text{ A}$; $dl_G/dt = 0.2\text{ A}/\mu s$	-	100	$A/\mu s$
I_{GM}	peak gate current		-	1	A
P_{GM}	peak gate power		-	2	W
$P_{G(AV)}$	average gate power	over any 20ms period	-	0.1	W
T_{stg}	storage temperature		-40	150	$^{\circ}C$
T_j	junction temperature		-	125	$^{\circ}C$



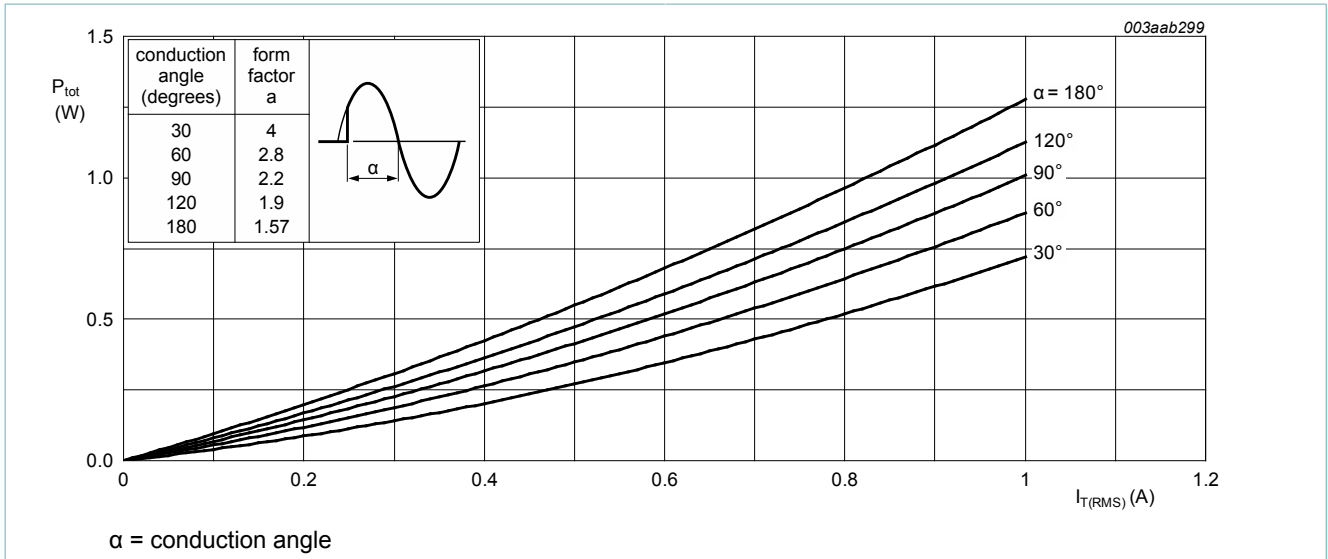


Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values

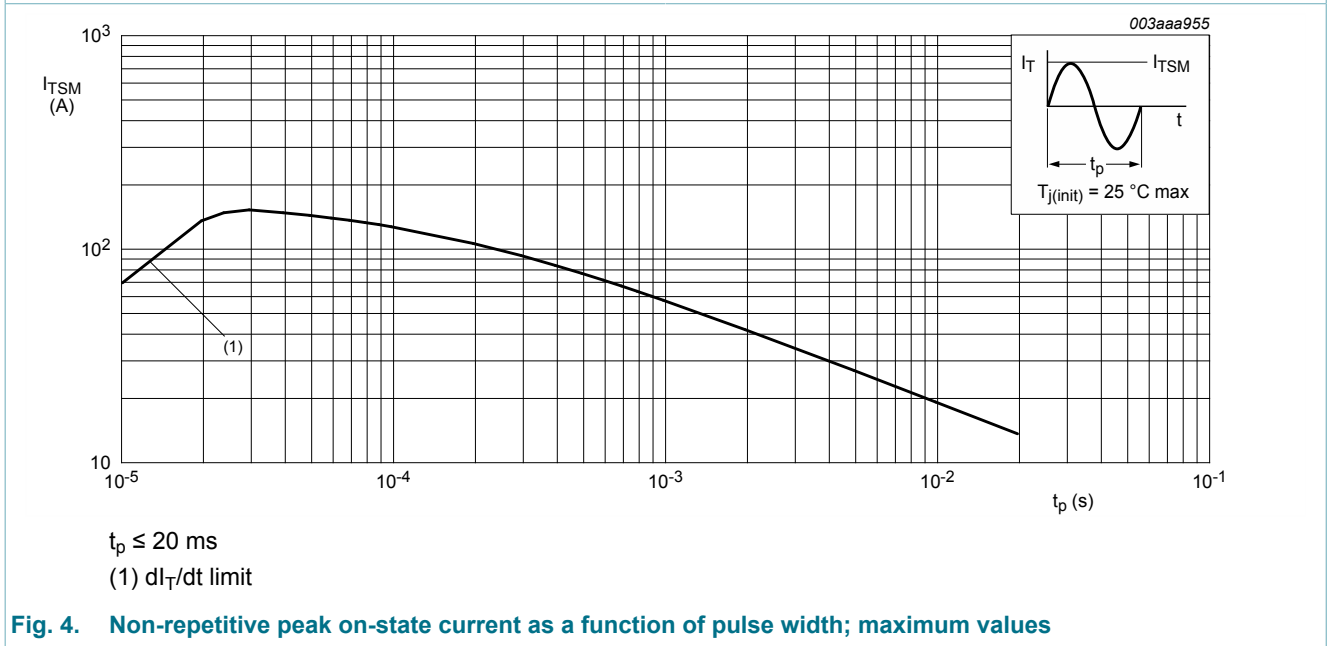
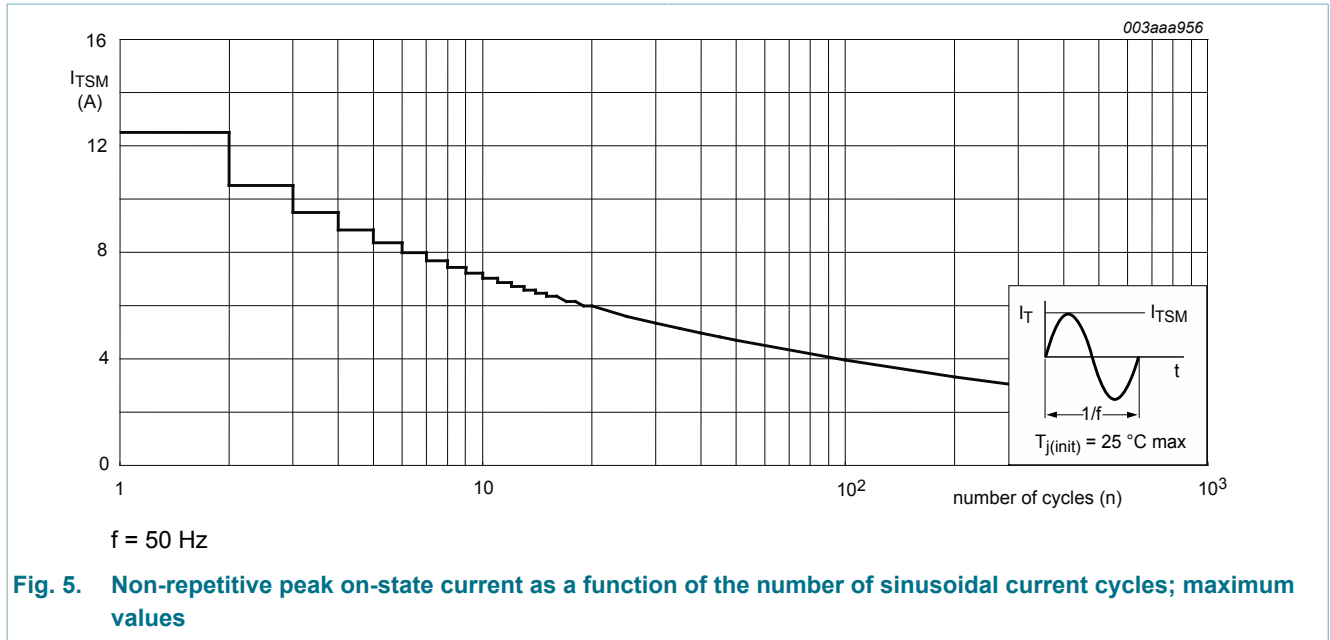


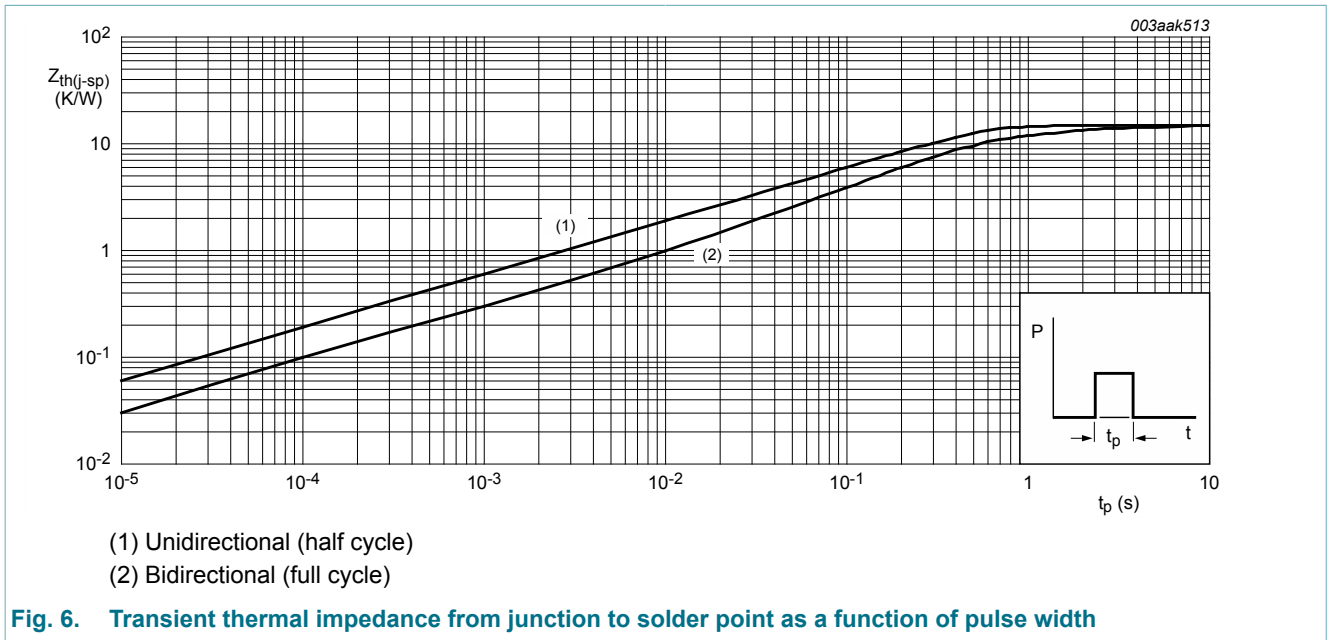
Fig. 4. Non-repetitive peak on-state current as a function of pulse width; maximum values

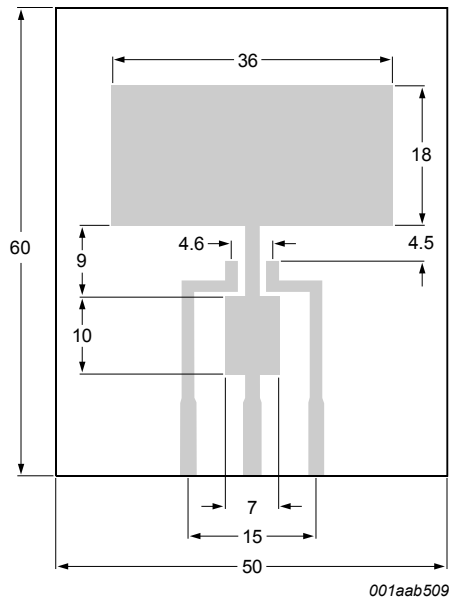


8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	full and half cycle; Fig. 6	-	-	15	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	printed circuit board mounted: minimum pad area; Fig. 7	-	70	-	K/W
		printed circuit board mounted: minimum footprint; Fig. 8	-	156	-	K/W





All dimensions are in mm
 Printed circuit board:
 FR4 epoxy glass (1.6 mm thick), copper laminate
 (35 μ m thick)

Fig. 7. Printed circuit board pad area: SOT223

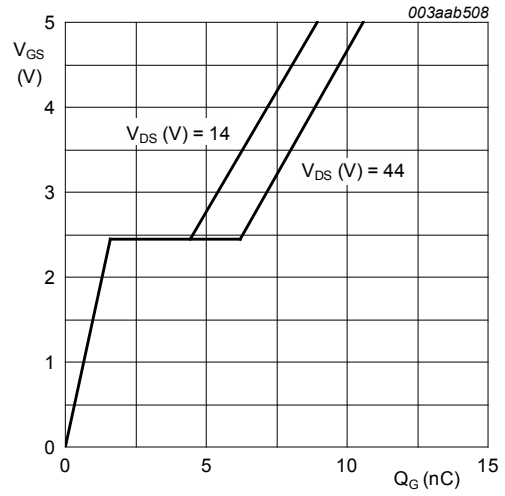


Fig. 8. Gate-source voltage as a function of gate charge; typical values

$$T_j = 25^\circ\text{C}; I_D = 10\text{A}$$

9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I_{GT}	gate trigger current	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G+; $T_j = 25\text{ °C}$; Fig. 9	1	-	10	mA
		$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G-; $T_j = 25\text{ °C}$; Fig. 9	1	-	10	mA
		$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2- G-; $T_j = 25\text{ °C}$; Fig. 9	1	-	10	mA
I_L	latching current	$V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; T2+ G-; $T_j = 25\text{ °C}$; Fig. 10	-	-	12	mA
		$V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; T2+ G+; $T_j = 25\text{ °C}$; Fig. 10	-	-	12	mA
		$V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; T2- G-; $T_j = 25\text{ °C}$; Fig. 10	-	-	12	mA
I_H	holding current	$V_D = 12\text{ V}$; $T_j = 25\text{ °C}$; Fig. 11	-	-	12	mA
V_T	on-state voltage	$I_T = 1.4\text{ A}$; $T_j = 25\text{ °C}$; Fig. 12	-	1.3	1.5	V
V_{GT}	gate trigger voltage	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; $T_j = 25\text{ °C}$; Fig. 13	-	0.7	1	V
		$V_D = 400\text{ V}$; $I_T = 0.1\text{ A}$; $T_j = 125\text{ °C}$; Fig. 13	0.2	0.3	-	V
I_D	off-state current	$V_D = 800\text{ V}$; $T_j = 125\text{ °C}$	-	0.1	0.5	mA
Dynamic characteristics						
dV_D/dt	rate of rise of off-state voltage	$V_{DM} = 536\text{ V}$; $T_j = 125\text{ °C}$; ($V_{DM} = 67\%$ of V_{DRM}); exponential waveform; gate open circuit; Fig. 14	600	-	-	V/ μ s
dI_{com}/dt	rate of change of commutating current	$V_D = 400\text{ V}$; $T_j = 125\text{ °C}$; $I_{T(RMS)} = 1\text{ A}$; $dV_{com}/dt = 20\text{ V/s}$; (snubberless condition); gate open circuit	2.5	-	-	A/ms
		$V_D = 400\text{ V}$; $T_j = 125\text{ °C}$; $I_{T(RMS)} = 1\text{ A}$; $dV_{com}/dt = 10\text{ V/s}$; gate open circuit	3.5	-	-	A/ms

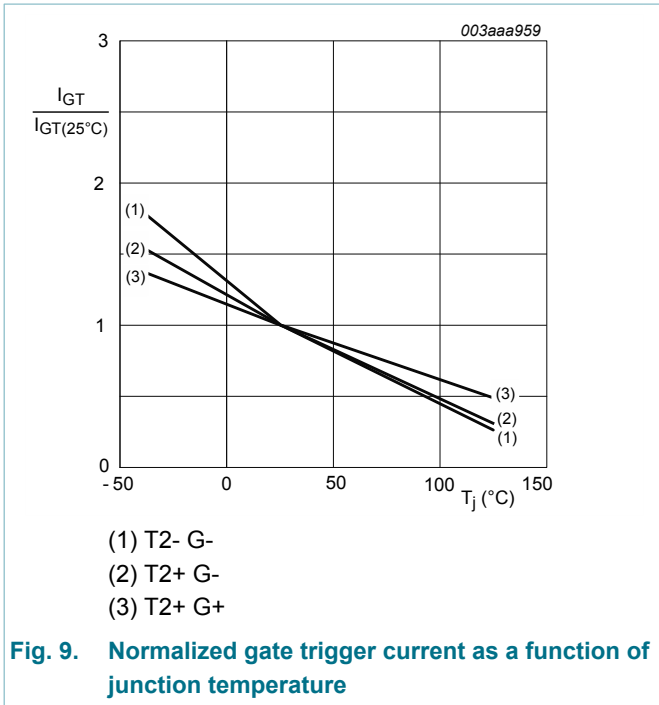


Fig. 9. Normalized gate trigger current as a function of junction temperature

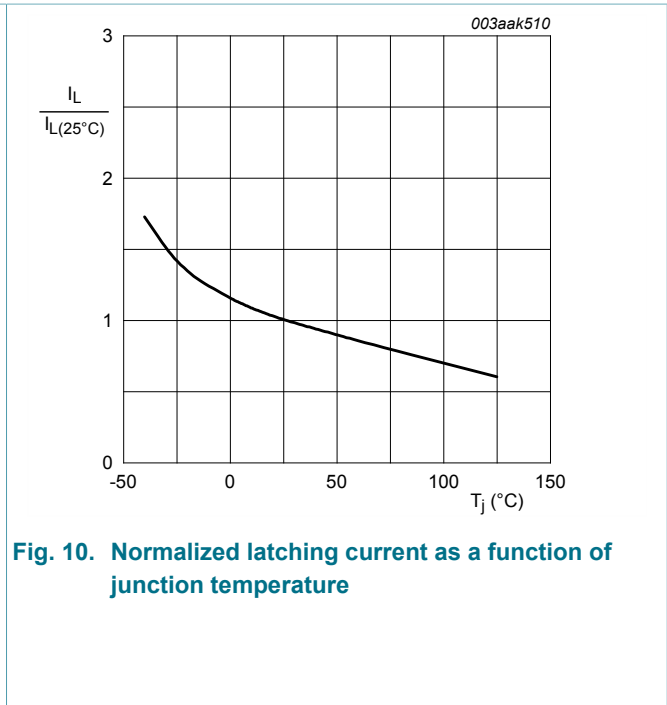


Fig. 10. Normalized latching current as a function of junction temperature

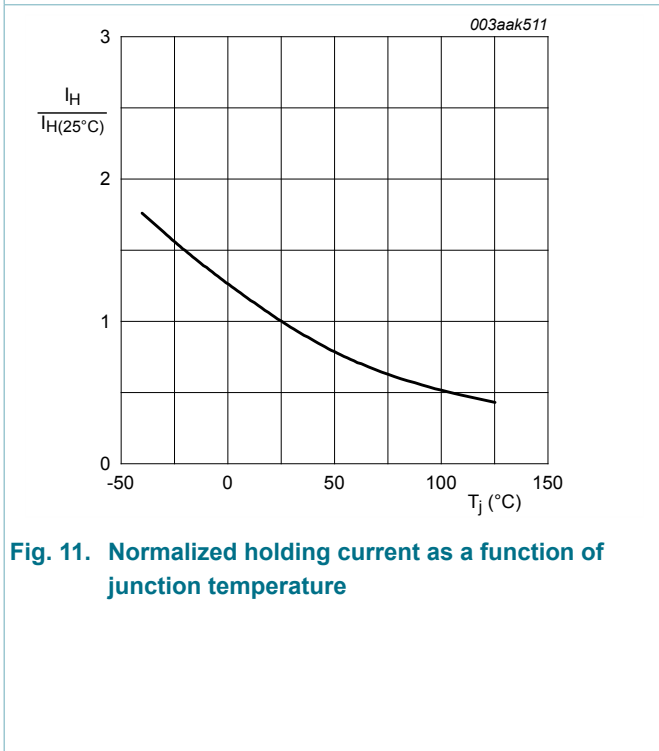


Fig. 11. Normalized holding current as a function of junction temperature

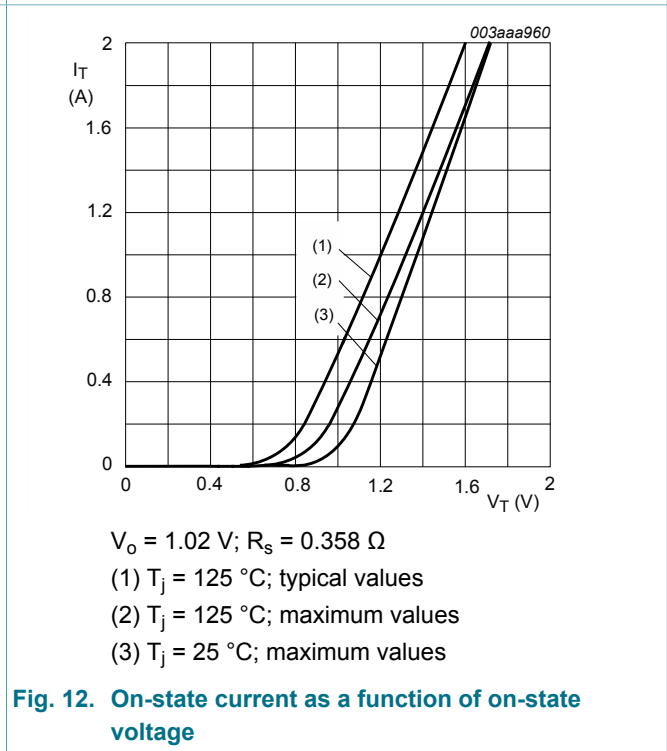


Fig. 12. On-state current as a function of on-state voltage

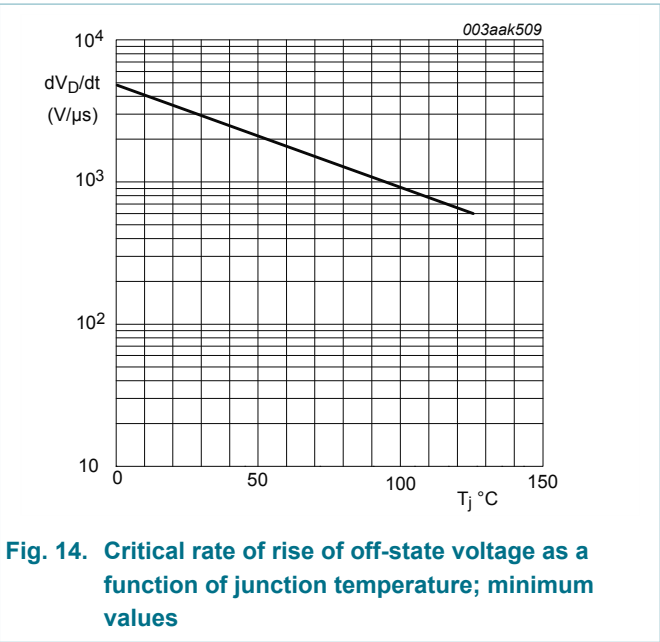
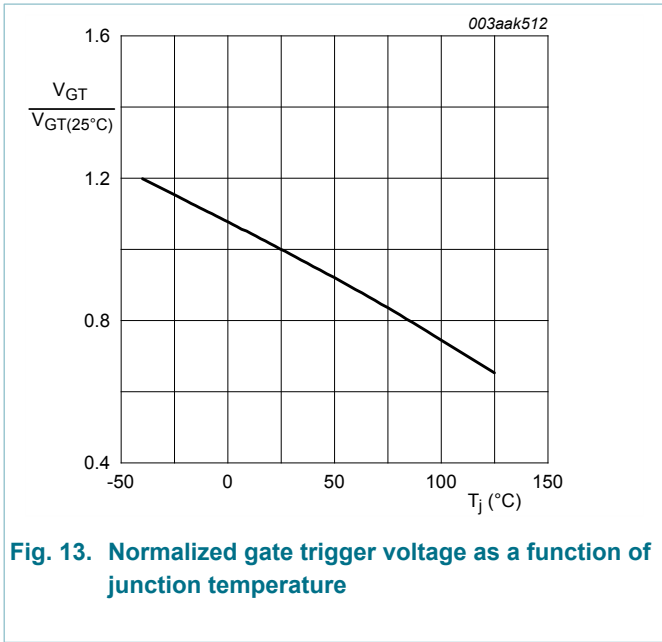


Fig. 13. Normalized gate trigger voltage as a function of junction temperature

Fig. 14. Critical rate of rise of off-state voltage as a function of junction temperature; minimum values

10. Package outline

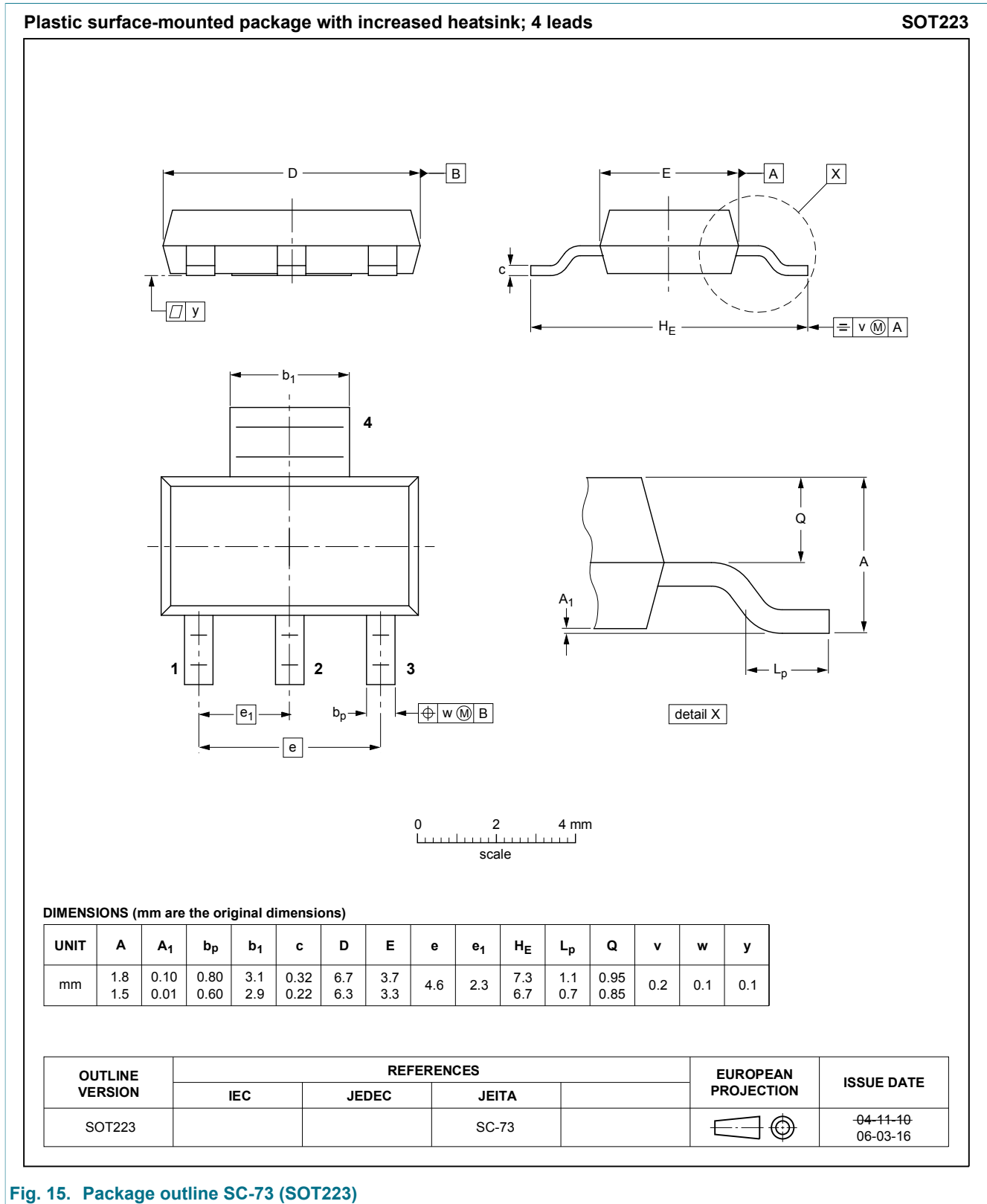


Fig. 15. Package outline SC-73 (SOT223)

11. Soldering

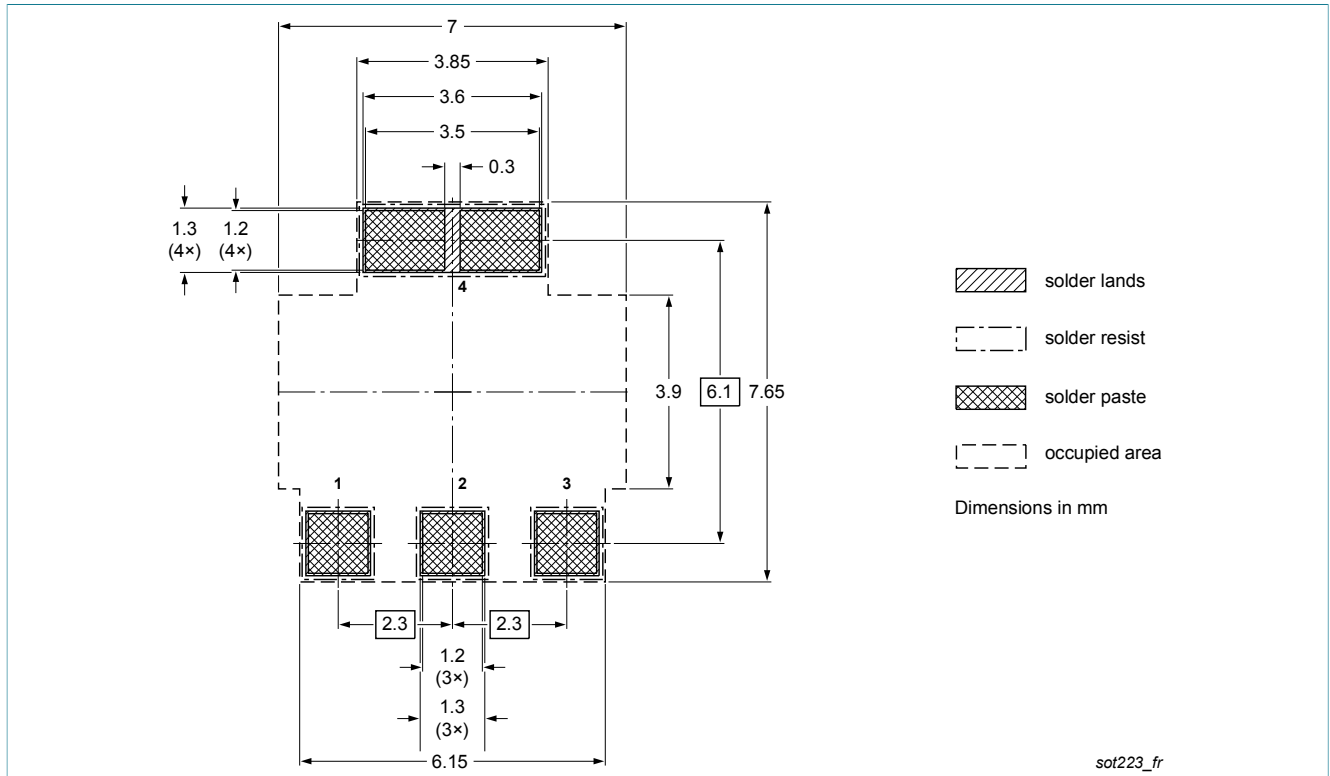


Fig. 16. Reflow soldering footprint for SC-73 (SOT223)

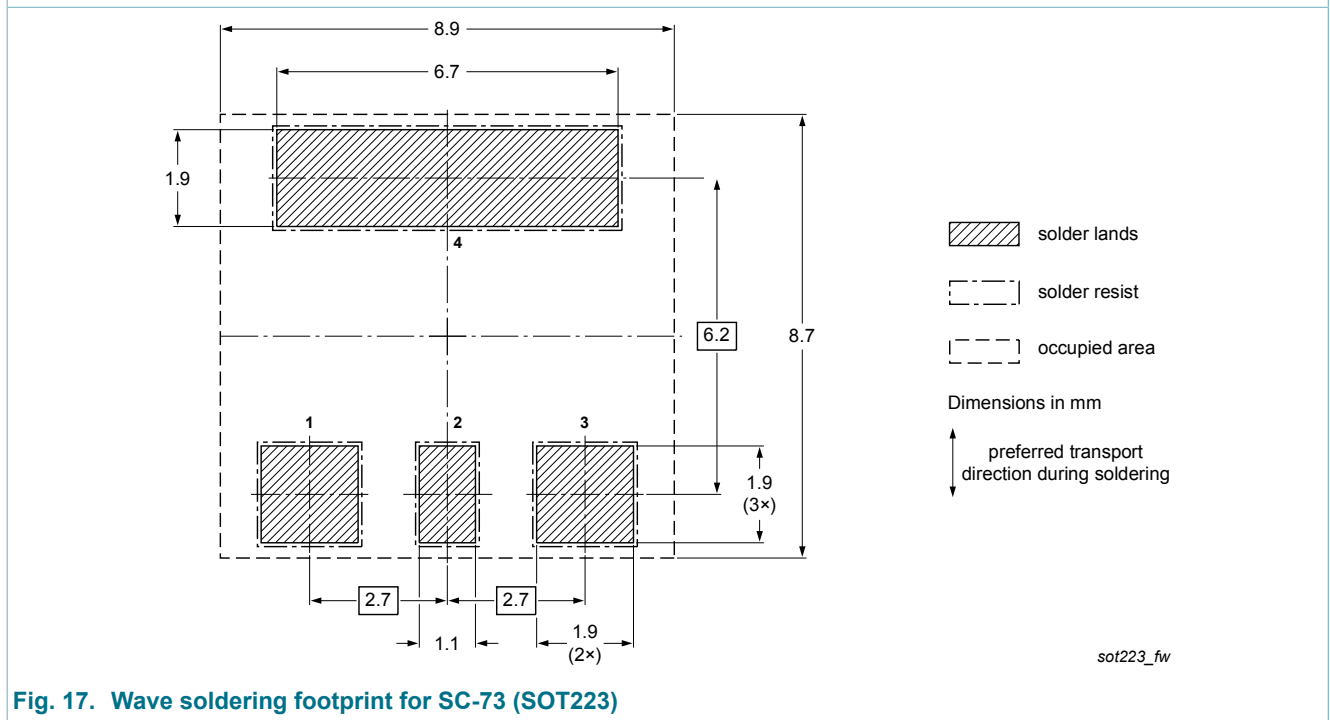


Fig. 17. Wave soldering footprint for SC-73 (SOT223)

12. Legal information

12.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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13. Contents

1	General description	1
2	Features and benefits	1
3	Applications	1
4	Quick reference data	1
5	Pinning information	2
6	Ordering information	2
7	Limiting values	3
8	Thermal characteristics	6
9	Characteristics	8
10	Package outline	11
11	Soldering	12
12	Legal information	13
12.1	Data sheet status	13
12.2	Definitions	13
12.3	Disclaimers	13
12.4	Trademarks	14

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