



BUK7S0R7-40H

N-channel 40 V, 0.7 mΩ standard level MOSFET in LPAK88

10 January 2025

Product data sheet

1. General description

Automotive qualified N-channel MOSFET using the latest Trench 9 low ohmic superjunction technology, housed in a copper-clip LPAK88 package. This product has been fully designed and qualified to meet beyond AEC-Q101 requirements delivering high performance and reliability.

2. Features and benefits

- Fully automotive qualified to beyond AEC-Q101:
 - 55 °C to +175 °C rating suitable for thermally demanding environments
- LPAK88 package:
 - Designed for smaller footprint and improved power density over older wire bond packages such as D²PAK for today's space constrained high power automotive applications
 - Thin package and copper clip enables LPAK88 to be highly efficient thermally
- LPAK copper clip technology enabling improvements over wire bond packages by:
 - Increased maximum current capability and excellent current spreading
 - Improved R_{DSon}
 - Low source inductance
 - Low thermal resistance R_{th}
- LPAK Gull Wing leads:
 - Flexible leads enabling high Board Level Reliability absorbing mechanical and thermal cycling stress, unlike traditional QFN packages
 - Visual (AOI) soldering inspection, no need for expensive x-ray equipment
 - Easy solder wetting for good mechanical solder joint
- Unique 40 V Trench 9 superjunction technology:
 - Reduced cell pitch and superjunction platform enables lower R_{DSon} in the same footprint
 - Improved SOA and avalanche capability compared to standard TrenchMOS
 - Tight $V_{GS(th)}$ limits enable easy paralleling of MOSFETs

3. Applications

- 12 V automotive systems
- 48 V DC/DC systems (on 12 V secondary side)
- Higher power motors, lamps and solenoid control
- Reverse polarity protection
- LED lighting
- Ultra high performance power switching

4. Quick reference data

Table 1. Quick reference data

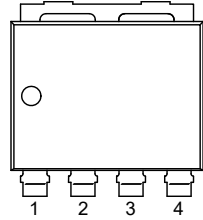
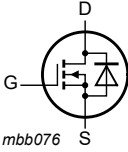
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$		-	-	40	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	[1]	-	-	425	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1		-	-	375	W

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 25 A; T _J = 25 °C; Fig. 9	0.43	0.62	0.7	mΩ
Dynamic characteristics						
Q _{GD}	gate-drain charge	I _D = 25 A; V _{DS} = 32 V; V _{GS} = 10 V; Fig. 11 ; Fig. 12	-	25	50	nC
Source-drain diode						
Q _r	recovered charge	I _S = 25 A; dI _S /dt = -100 A/μs; V _{GS} = 0 V; V _{DS} = 20 V [2]	-	74	-	nC
S	softness factor	I _S = 25 A; dI _S /dt = -100 A/μs; V _{GS} = 0 V; V _{DS} = 20 V; T _J = 25 °C	-	0.79	-	

- [1] 425A continuous current has been successfully demonstrated during application. practically the current will be limited by PCB, thermal design and operating temperature.
- [2] includes capacitive recovery

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 LFPAK88 (SOT1235)	 mbb076
2	S	source		
3	S	source		
4	S	source		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK7S0R7-40H	LFPAK88	plastic, single-ended surface-mounted package (LFPAK88); 4 leads; 2 mm pitch; 8 mm x 8 mm x 1.6 mm body	SOT1235

7. Marking

Table 4. Marking codes

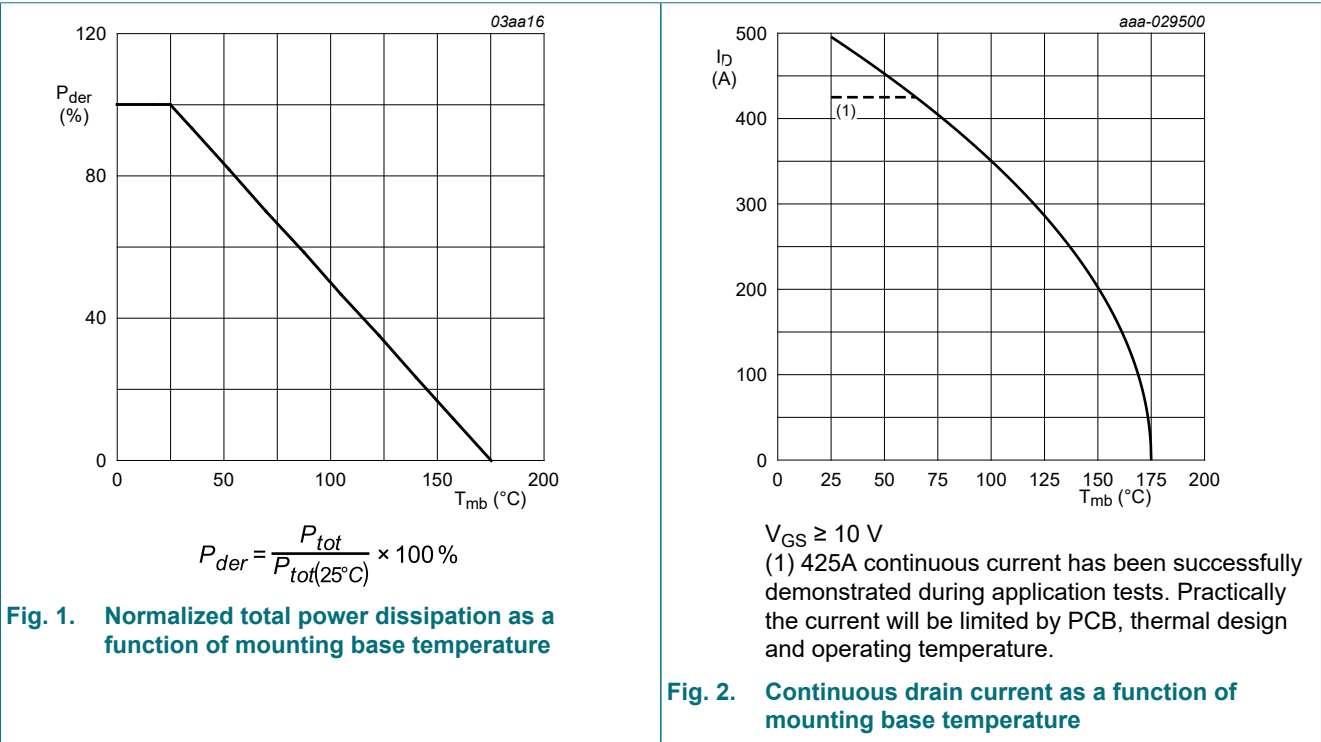
Type number	Marking code
BUK7S0R7-40H	7S0R740H

8. Limiting values

Table 5. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134). Tj = 25 °C unless otherwise stated.

Symbol	Parameter	Conditions		Min	Max	Unit
V _{DS}	drain-source voltage	25 °C ≤ T _j ≤ 175 °C		-	40	V
V _{GS}	gate-source voltage		[1]	-20	20	V
P _{tot}	total power dissipation	T _{mb} = 25 °C; Fig. 1		-	375	W
I _D	drain current	V _{GS} = 10 V; T _{mb} = 25 °C; Fig. 2	[2]	-	425	A
I _{DM}	peak drain current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C; Fig. 3		-	1983	A
T _{stg}	storage temperature			-55	175	°C
T _j	junction temperature			-55	175	°C
Source-drain diode						
I _S	source current	T _{mb} = 25 °C	[3]	-	500	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C		-	1983	A
Avalanche ruggedness						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I _D = 120 A; V _{sup} ≤ 40 V; R _{GS} = 50 Ω; V _{GS} = 10 V; T _{j(init)} = 25 °C; unclamped; Fig. 4	[4] [5]	-	940	mJ

- [1] Refer to application note AN90001 for further information.
- [2] 425A continuous current has been successfully demonstrated during application. practically the current will be limited by PCB, thermal design and operating temperature.
- [3] 500A continuous current has been successfully demonstrated during application. practically the current will be limited by PCB, thermal design and operating temperature.
- [4] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
- [5] Refer to application note AN10273 for further information.



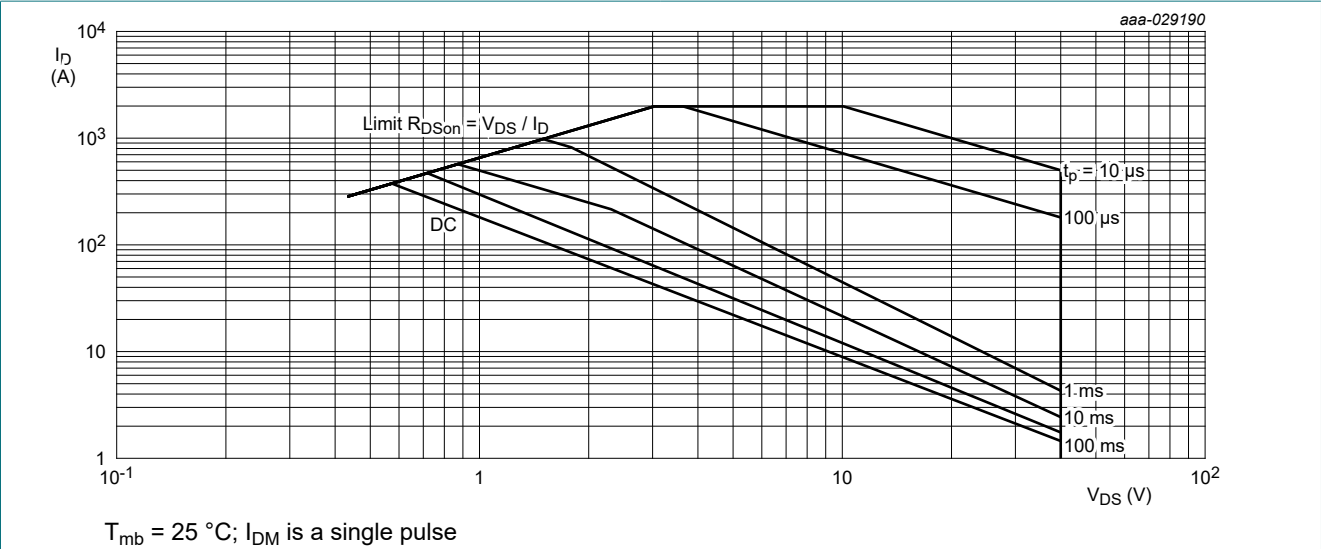


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

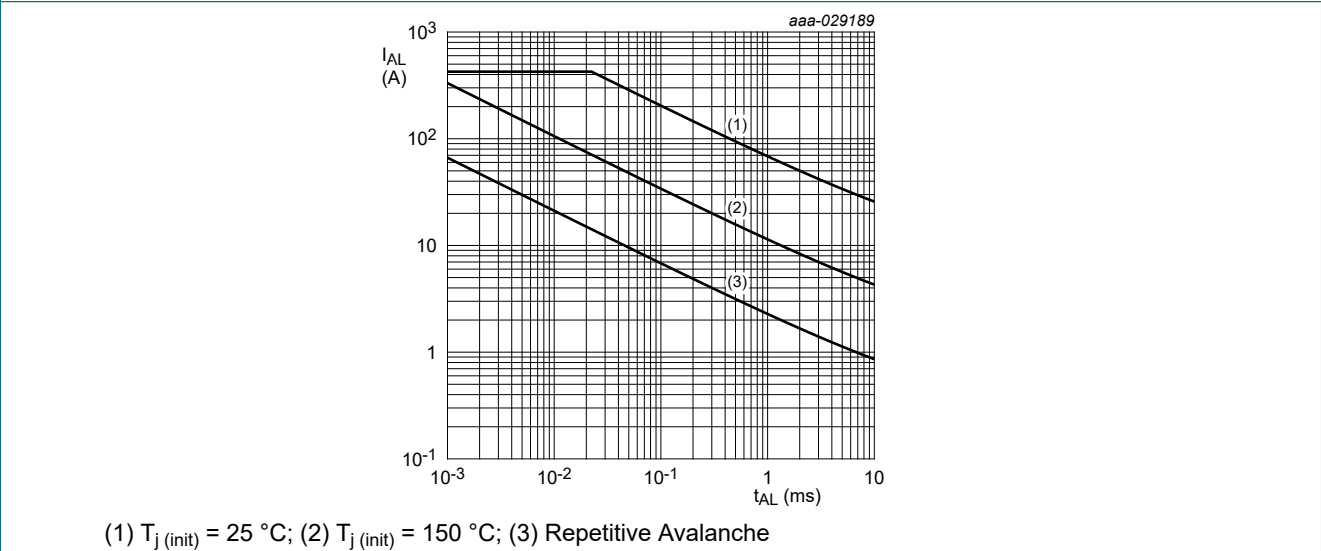
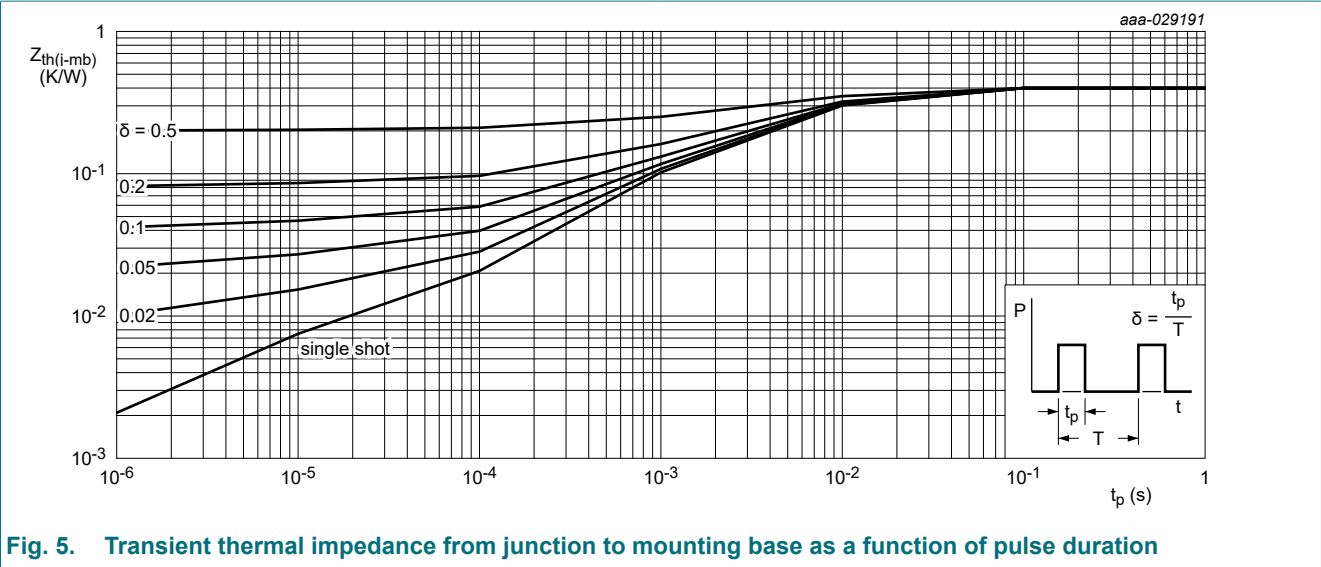


Fig. 4. Avalanche rating; avalanche current as a function of avalanche time

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	0.35	0.4	K/W



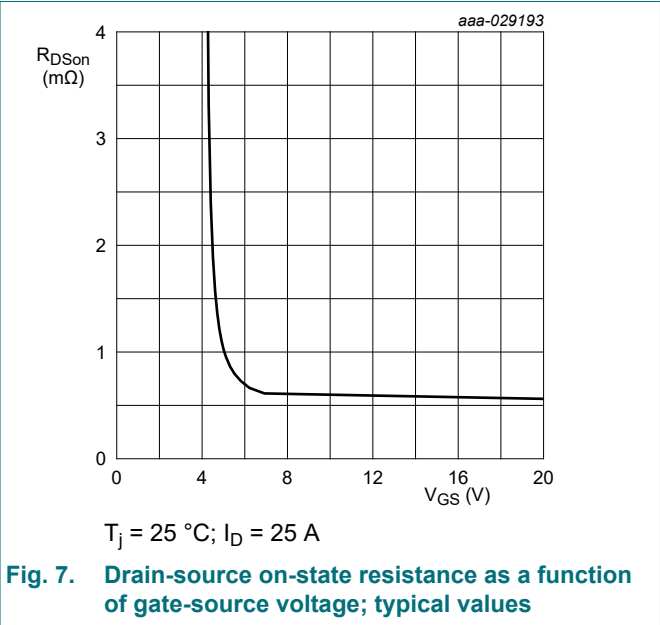
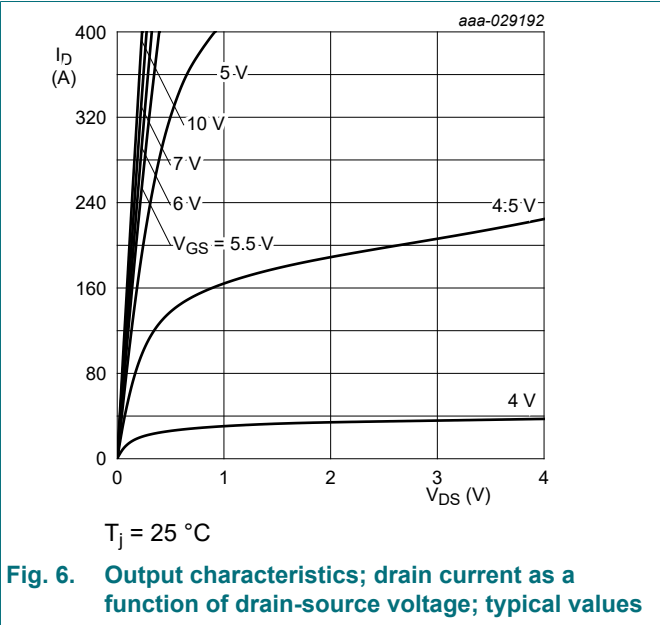
10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 250 μA; V _{GS} = 0 V; T _J = 25 °C	40	43	-	V
		I _D = 250 μA; V _{GS} = 0 V; T _J = -40 °C	-	40.5	-	V
		I _D = 250 μA; V _{GS} = 0 V; T _J = -55 °C	36	40	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} =V _{GS} ; T _J = 25 °C	2.4	3	3.6	V
		I _D = 1 mA; V _{DS} =V _{GS} ; T _J = -55 °C	-	-	4.3	V
		I _D = 1 mA; V _{DS} =V _{GS} ; T _J = 175 °C	1	-	-	V
I _{DSS}	drain leakage current	V _{DS} = 40 V; V _{GS} = 0 V; T _J = 25 °C	-	0.86	2.3	μA
		V _{DS} = 16 V; V _{GS} = 0 V; T _J = 125 °C	-	10	25	μA
		V _{DS} = 40 V; V _{GS} = 0 V; T _J = 175 °C	-	614	1500	μA
I _{GSS}	gate leakage current	V _{GS} = 20 V; V _{DS} = 0 V; T _J = 25 °C	-	2	100	nA
		V _{GS} = -16 V; V _{DS} = 0 V; T _J = 25 °C	-	2	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 25 A; T _J = 25 °C; Fig. 9	0.43	0.62	0.7	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _J = 105 °C; Fig. 10	0.61	0.9	1.11	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _J = 125 °C; Fig. 10	0.68	1	1.23	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _J = 175 °C; Fig. 10	0.85	1.23	1.53	mΩ
R _G	gate resistance	f = 1 MHz; T _J = 25 °C	0.5	1.2	3	Ω
Dynamic characteristics						
Q _{G(tot)}	total gate charge	I _D = 25 A; V _{DS} = 32 V; V _{GS} = 10 V; Fig. 11 ; Fig. 12	-	144	202	nC
Q _{GS}	gate-source charge		-	40	60	nC
Q _{GD}	gate-drain charge		-	25	50	nC

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
C _{iss}	input capacitance	V _{DS} = 25 V; V _{GS} = 0 V; f = 1 MHz; T _j = 25 °C; Fig. 13		-	11228	15719	pF
C _{oss}	output capacitance			-	2363	3308	pF
C _{rss}	reverse transfer capacitance			-	415	913	pF
t _{d(on)}	turn-on delay time	V _{DS} = 30 V; R _L = 1.2 Ω; V _{GS} = 10 V; R _{G(ext)} = 5 Ω		-	35	-	ns
t _r	rise time			-	30	-	ns
t _{d(off)}	turn-off delay time			-	94	-	ns
t _f	fall time			-	41	-	ns
Source-drain diode							
V _{SD}	source-drain voltage	I _S = 25 A; V _{GS} = 0 V; T _j = 25 °C; Fig. 14		-	0.75	1	V
t _{rr}	reverse recovery time	I _S = 25 A; dI _S /dt = -100 A/μs; V _{GS} = 0 V; V _{DS} = 20 V		-	53	-	ns
Q _r	recovered charge		[1]	-	74	-	nC
S	softness factor	I _S = 25 A; dI _S /dt = -100 A/μs; V _{GS} = 0 V; V _{DS} = 20 V; T _j = 25 °C		-	0.79	-	
		I _S = 25 A; dI _S /dt = -500 A/μs; V _{GS} = 0 V; V _{DS} = 20 V; T _j = 25 °C		-	0.73	-	

[1] includes capacitive recovery



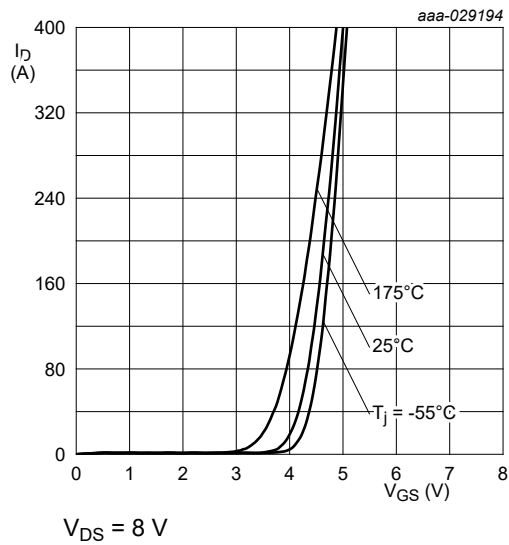


Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values

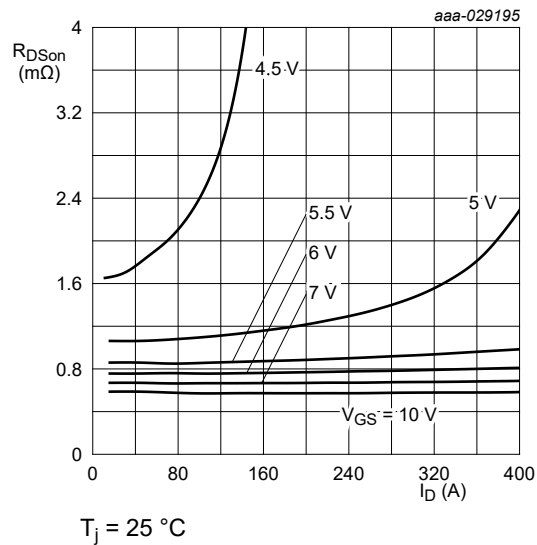


Fig. 9. Drain-source on-state resistance as a function of drain current; typical values

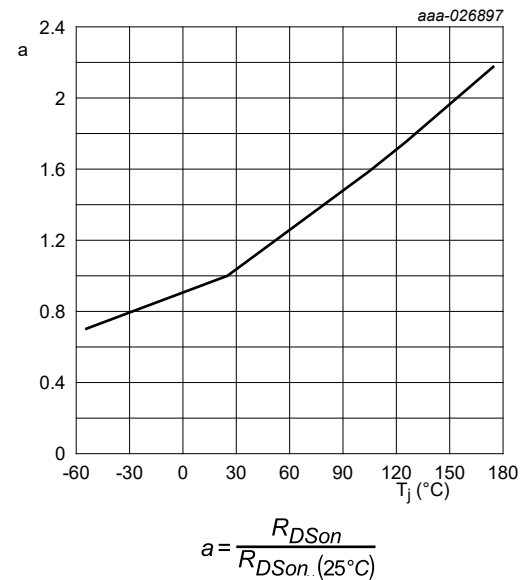


Fig. 10. Normalized drain-source on-state resistance factor as a function of junction temperature

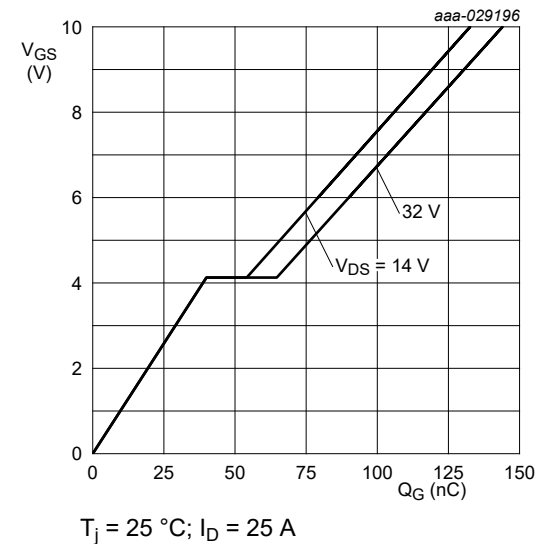


Fig. 11. Gate-source voltage as a function of gate charge; typical values

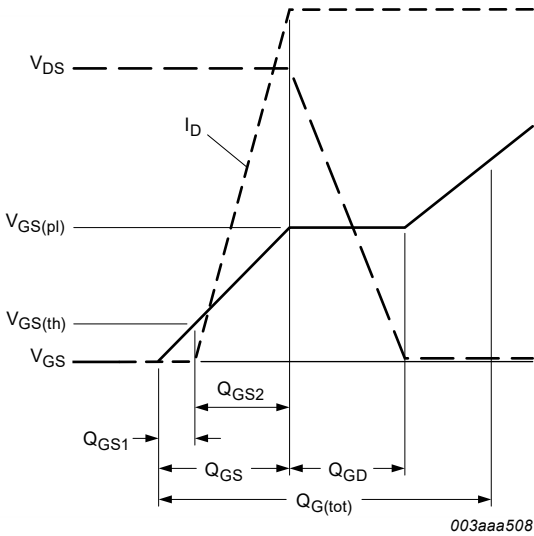


Fig. 12. Gate charge waveform definitions

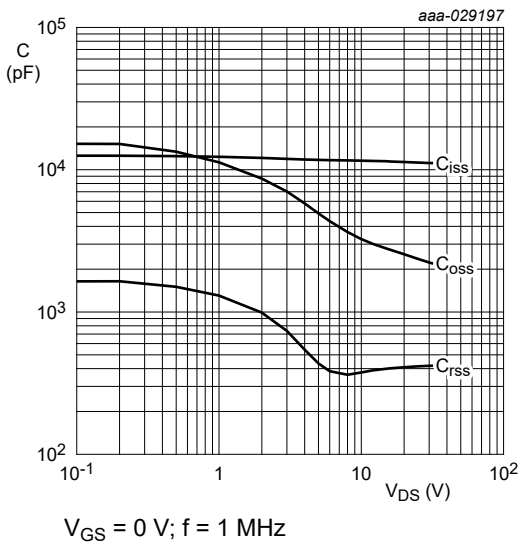
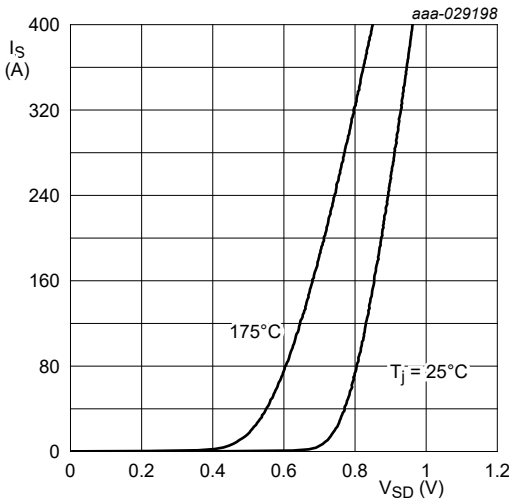


Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$V_{GS} = 0\text{ V}$

Fig. 14. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

11. Package outline

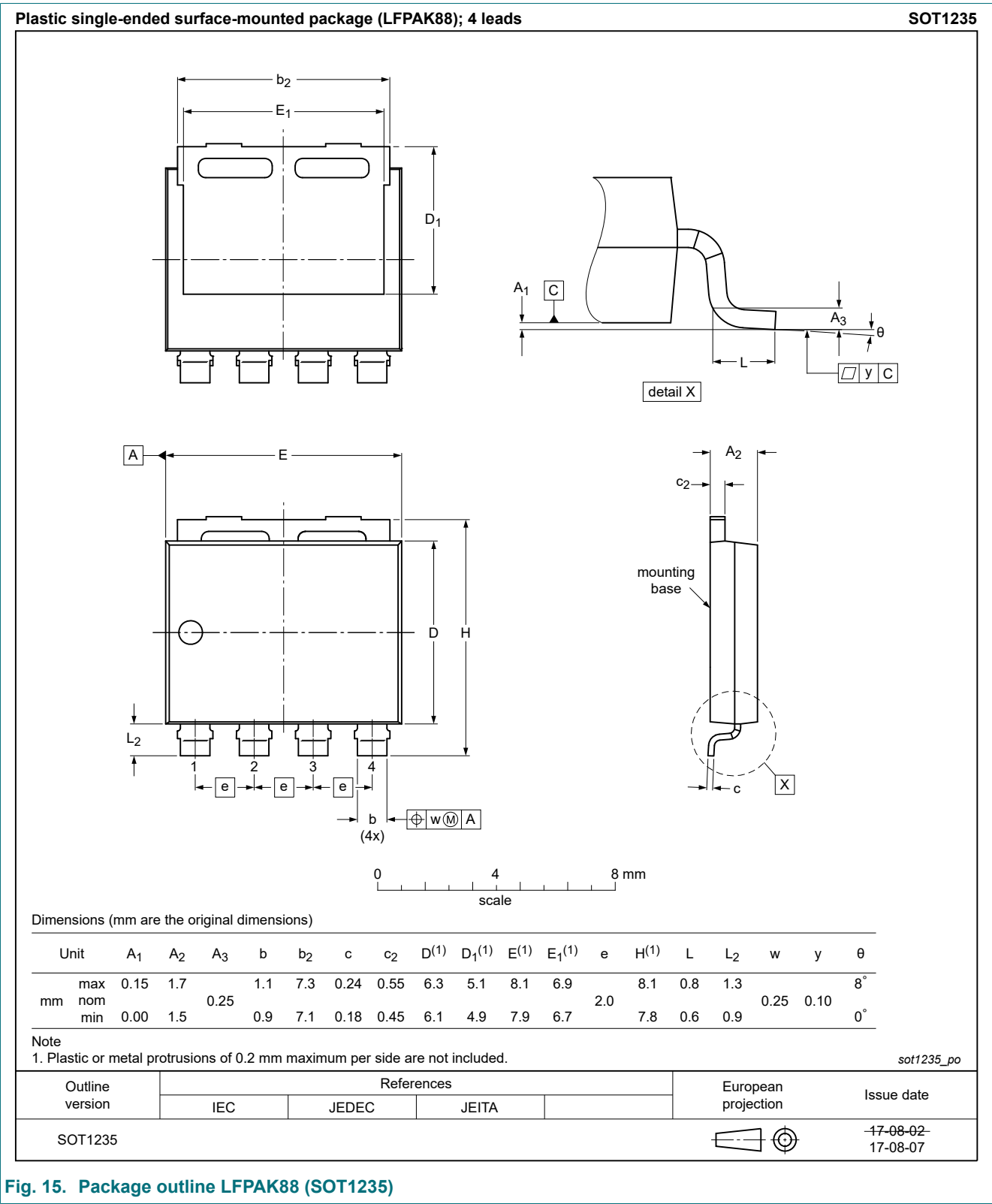


Fig. 15. Package outline LPAK88 (SOT1235)

12. Soldering

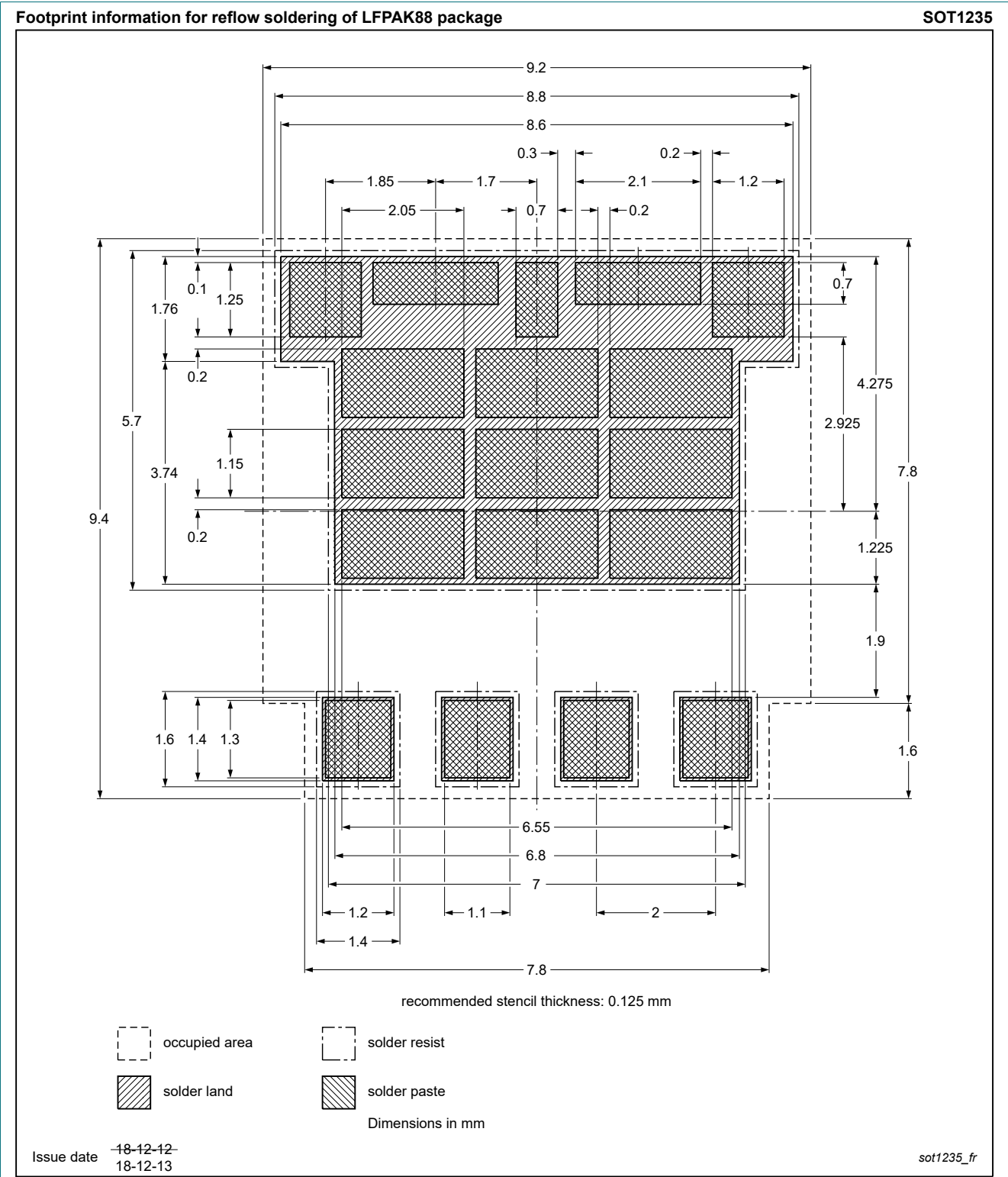


Fig. 16. Reflow soldering footprint for LPAK88 (SOT1235)

13. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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