

# MOSFET – Power, Dual N-Channel

## 80 V, 6.9 mΩ, 74 A

### NVMFD6H840NL

#### Features

- Small Footprint (5x6 mm) for Compact Design
- Low  $R_{DS(on)}$  to Minimize Conduction Losses
- Low  $Q_G$  and Capacitance to Minimize Driver Losses
- NVMFD6H840NLWF – Wettable Flank Option for Enhanced Optical Inspection
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

#### MAXIMUM RATINGS ( $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	$V_{DSS}$	80	V
Gate-to-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current $R_{\theta JC}$ (Notes 1, 2, 3)	Steady State	$T_C = 25\text{ }^\circ\text{C}$	$I_D$ 74 A
		$T_C = 100\text{ }^\circ\text{C}$	52
Power Dissipation $R_{\theta JC}$ (Notes 1, 2)	Steady State	$T_C = 25\text{ }^\circ\text{C}$	$P_D$ 90 W
		$T_C = 100\text{ }^\circ\text{C}$	45
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 3)	Steady State	$T_A = 25\text{ }^\circ\text{C}$	$I_D$ 14 A
		$T_A = 100\text{ }^\circ\text{C}$	10
Power Dissipation $R_{\theta JA}$ (Notes 1, 2)	Steady State	$T_A = 25\text{ }^\circ\text{C}$	$P_D$ 3.1 W
		$T_A = 100\text{ }^\circ\text{C}$	1.5
Pulsed Drain Current	$T_A = 25\text{ }^\circ\text{C}, t_p = 10\text{ }\mu\text{s}$	$I_{DM}$ 336	A
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to +175	$^\circ\text{C}$
Source Current (Body Diode)	$I_S$	75	A
Single Pulse Drain-to-Source Avalanche Energy ( $T_J = 25\text{ }^\circ\text{C}, I_{L(pk)} = 4.7\text{ A}$ )	$E_{AS}$	297	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	$T_L$	260	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

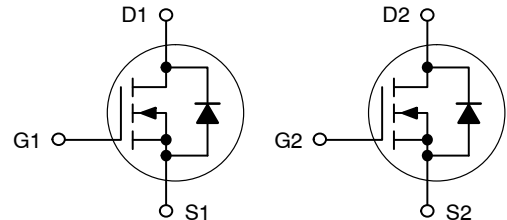
#### THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case – Steady State	$R_{\theta JC}$	1.67	$^\circ\text{C/W}$
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	48.7	

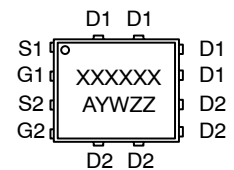
1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using a 650 mm<sup>2</sup>, 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

$V_{(BR)DSS}$	$R_{DS(ON)}\text{ MAX}$	$I_D\text{ MAX}$
80 V	6.9 mΩ @ 10 V	74 A
	8.8 mΩ @ 4.5 V	

#### Dual N-Channel



#### MARKING DIAGRAM



- A = Assembly Location
- Y = Year
- W = Work Week
- ZZ = Lot Traceability

#### ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

# NVMFD6H840NL

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25 °C unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	80			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V <sub>(BR)DSS</sub> /T <sub>J</sub>			45.9		mV/°C
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 80 V	T <sub>J</sub> = 25 °C		10	μA
			T <sub>J</sub> = 125 °C		250	
Gate-to-Source Leakage Current	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = 20 V			100	nA

### ON CHARACTERISTICS (Note 4)

Gate Threshold Voltage	V <sub>GS(TH)</sub>	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 96 μA	1.2		2.0	V
Threshold Temperature Coefficient	V <sub>GS(TH)</sub> /T <sub>J</sub>			-4.9		mV/°C
Drain-to-Source On Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 20 A	5.7	6.9	mΩ
		V <sub>GS</sub> = 4.5 V	I <sub>D</sub> = 20 A	7.0	8.8	
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> = 5 V, I <sub>D</sub> = 20 A		99		S

### CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C <sub>ISS</sub>	V <sub>GS</sub> = 0 V, f = 1 MHz, V <sub>DS</sub> = 40 V		2002		pF
Output Capacitance	C <sub>OSS</sub>			249		
Reverse Transfer Capacitance	C <sub>RSS</sub>			11		
Total Gate Charge	Q <sub>G(TOT)</sub>	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 40 V; I <sub>D</sub> = 20 A		32		nC
Total Gate Charge	Q <sub>G(TOT)</sub>	V <sub>GS</sub> = 4.5 V, V <sub>DS</sub> = 40 V; I <sub>D</sub> = 20 A		15		
Threshold Gate Charge	Q <sub>G(TH)</sub>			3.0		
Gate-to-Source Charge	Q <sub>GS</sub>			5.1		
Gate-to-Drain Charge	Q <sub>GD</sub>			5.3		
Plateau Voltage	V <sub>GP</sub>			2.8		

### SWITCHING CHARACTERISTICS (Note 5)

Turn-On Delay Time	t <sub>d(ON)</sub>	V <sub>GS</sub> = 4.5 V, V <sub>DS</sub> = 64 V, I <sub>D</sub> = 20 A, R <sub>G</sub> = 2.5 Ω		15		ns
Rise Time	t <sub>r</sub>			34		
Turn-Off Delay Time	t <sub>d(OFF)</sub>			52		
Fall Time	t <sub>f</sub>			22		

### DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V <sub>SD</sub>	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 20 A	T <sub>J</sub> = 25 °C		0.8	1.2	V
			T <sub>J</sub> = 125 °C		0.7		
Reverse Recovery Time	t <sub>RR</sub>	V <sub>GS</sub> = 0 V, dI <sub>S</sub> /dt = 100 A/μs, I <sub>S</sub> = 20 A		45		ns	
Charge Time	t <sub>a</sub>			24			
Discharge Time	t <sub>b</sub>			22			
Reverse Recovery Charge	Q <sub>RR</sub>			50		nC	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.

5. Switching characteristics are independent of operating junction temperatures.

# NVMFD6H840NL

## TYPICAL CHARACTERISTICS

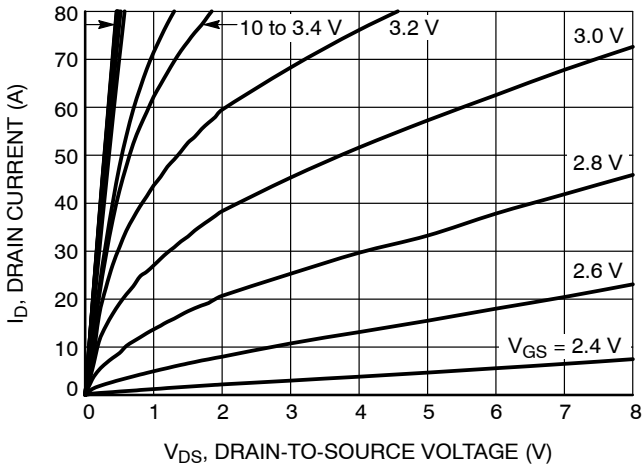


Figure 1. On-Region Characteristics

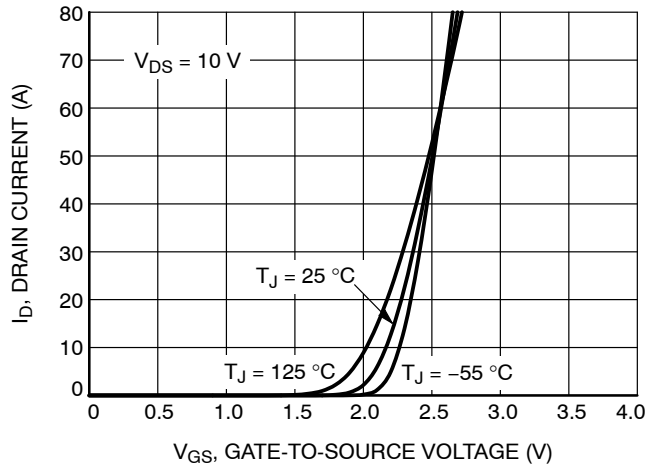


Figure 2. Transfer Characteristics

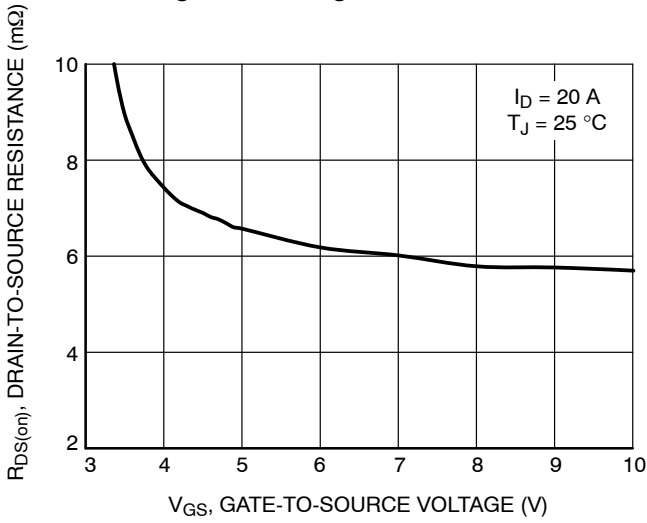


Figure 3. On-Resistance vs. Gate-to-Source Voltage

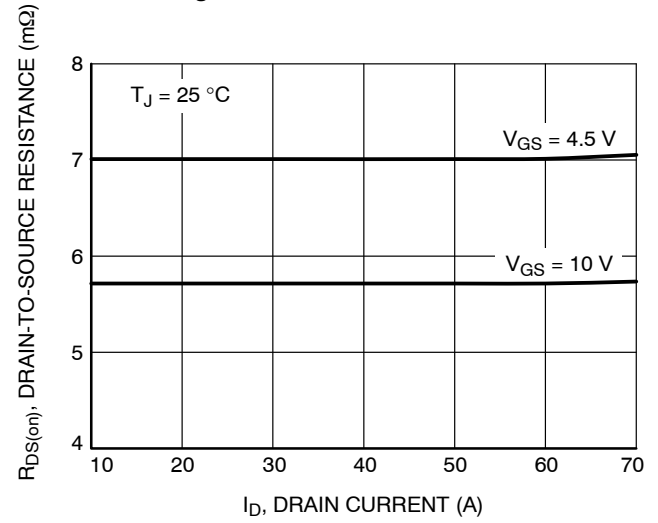


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

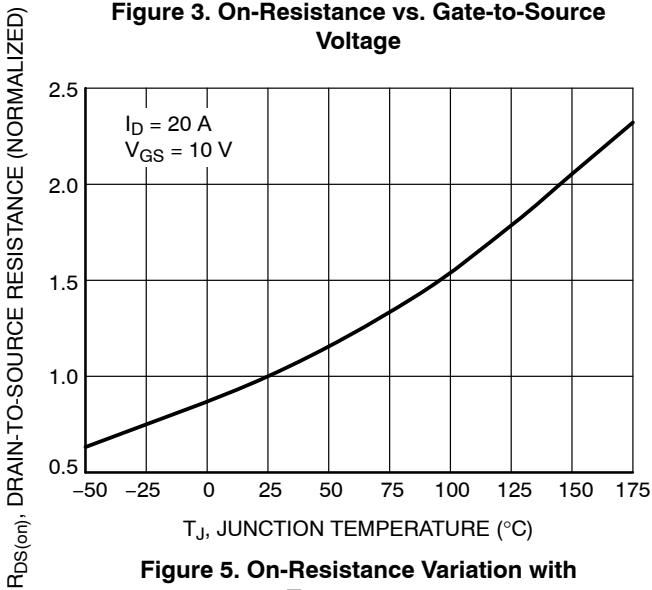


Figure 5. On-Resistance Variation with Temperature

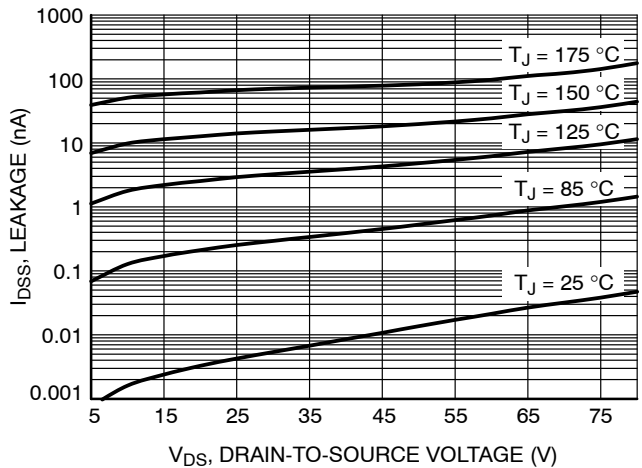


Figure 6. Drain-to-Source Leakage Current vs. Voltage

# NVMFD6H840NL

## TYPICAL CHARACTERISTICS

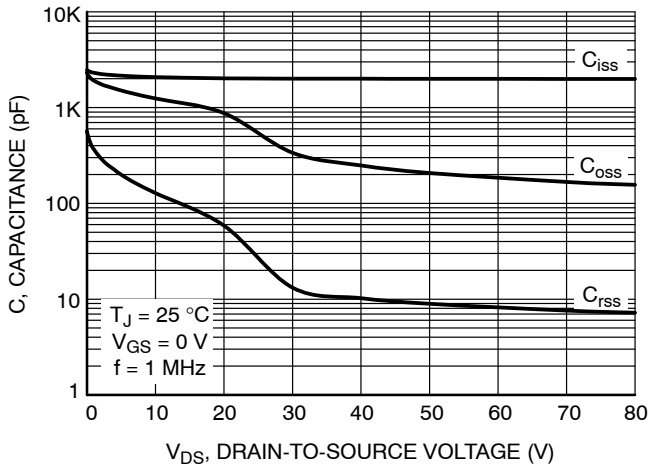


Figure 7. Capacitance Variation

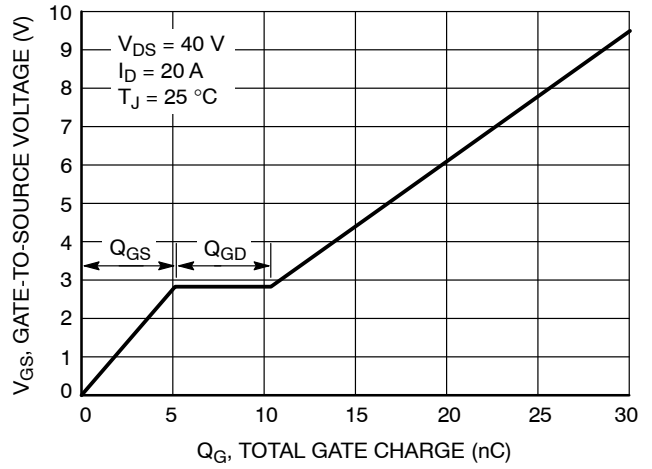


Figure 8. Gate-to-Source vs. Total Charge

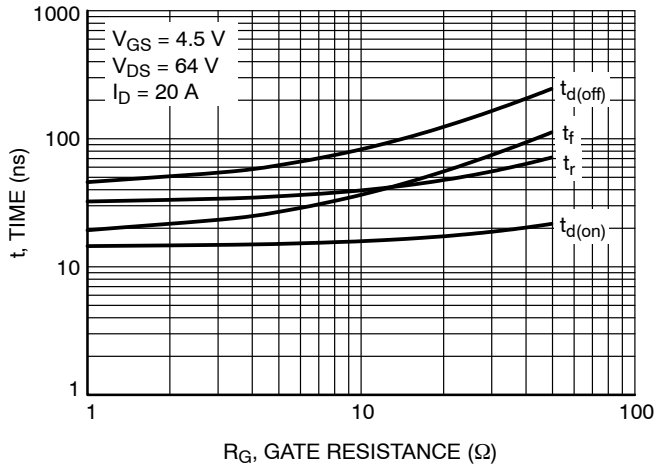


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

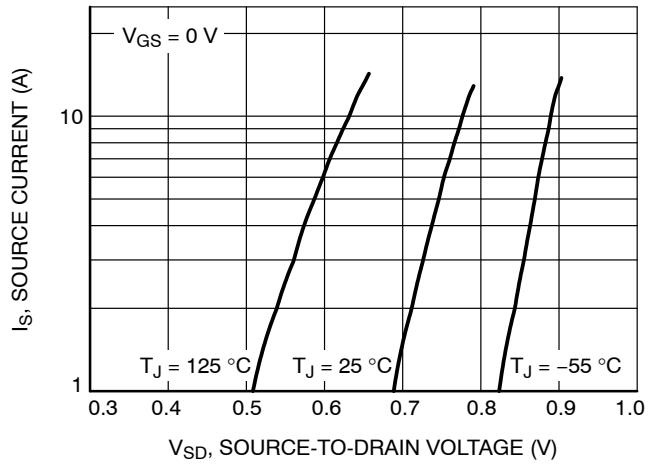


Figure 10. Diode Forward Voltage vs. Current

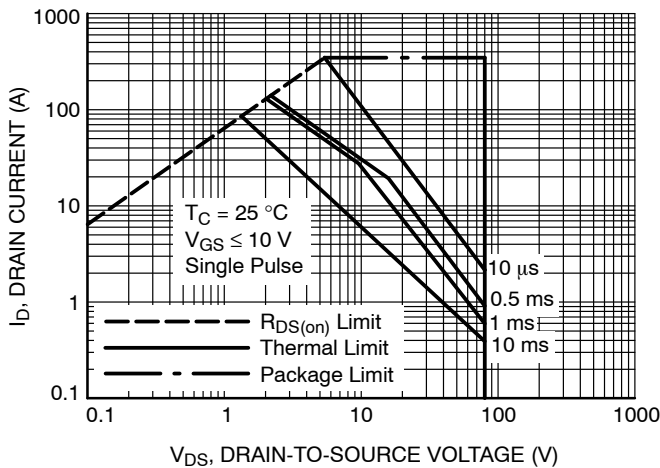


Figure 11. Maximum Rated Forward Biased Safe Operating Area

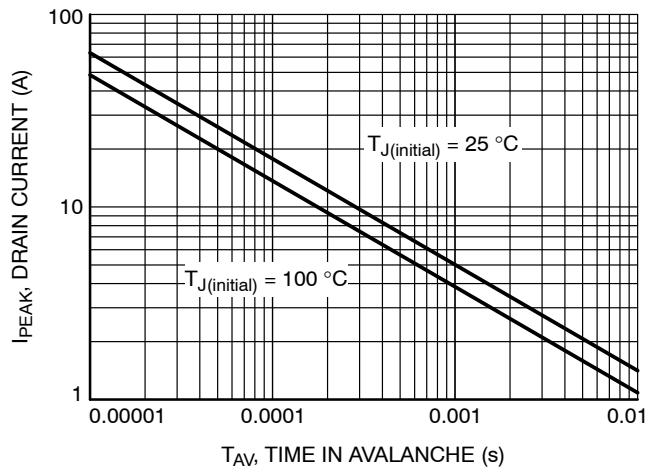
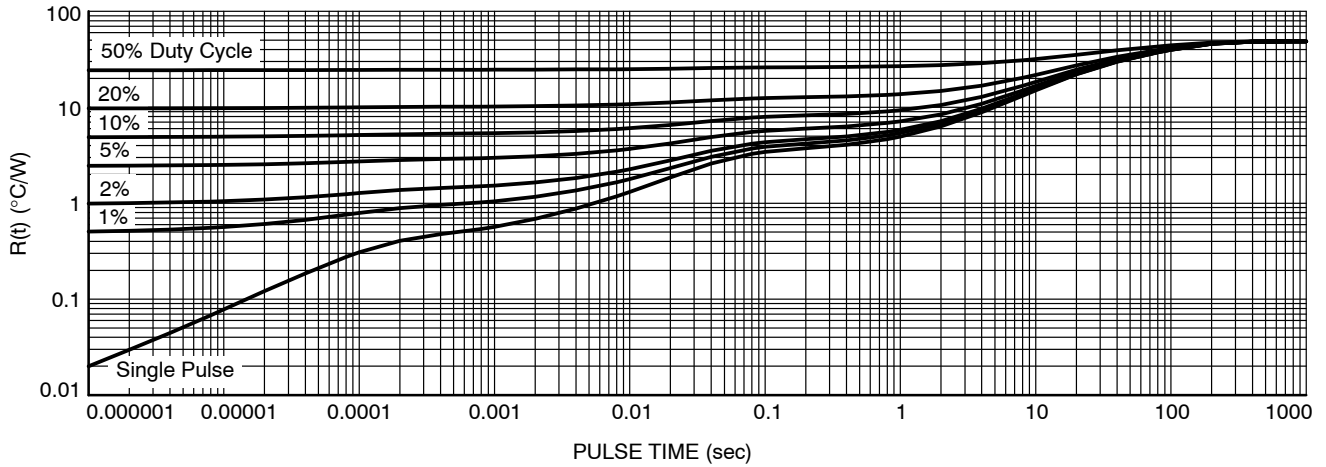


Figure 12. Maximum Drain Current vs. Time in Avalanche

# NVMFD6H840NL

## TYPICAL CHARACTERISTICS



**Figure 13. Thermal Response**

### DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping†
NVMFD6H840NLT1G	6H840L	DFN8 (Pb-Free)	1500 / Tape & Reel
NVMFD6H840NLWFT1G	840LWF	DFN8 (Pb-Free, Wettable Flanks)	1500 / Tape & Reel

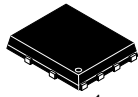
† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

# NVMFD6H840NL

## REVISION HISTORY

Revision	Description of Changes	Date
1	Document rebranded to <b>onsemi</b> format.	10/8/2025

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.



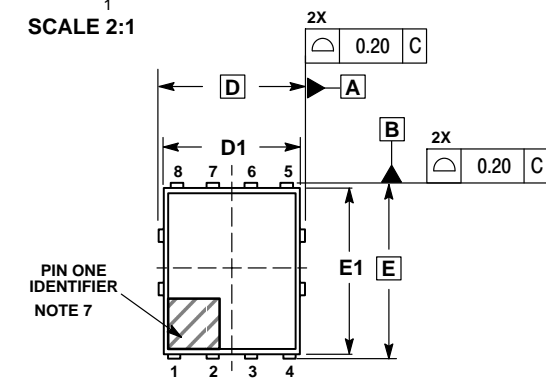
SCALE 2:1

DFN8 5x6, 1.27P Dual Flag (SO8FL-Dual)  
CASE 506BT  
ISSUE F

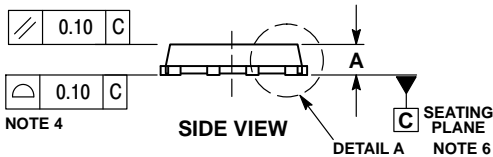
DATE 23 NOV 2021

NOTES:

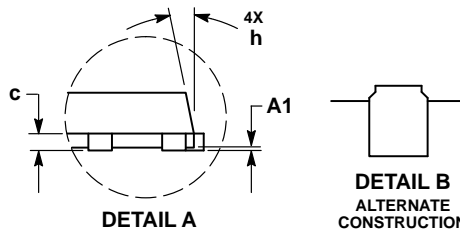
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. PROFILE TOLERANCE APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
6. SEATING PLANE IS DEFINED BY THE TERMINALS. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
7. A VISUAL INDICATOR FOR PIN 1 MUST BE LOCATED IN THIS AREA.



TOP VIEW

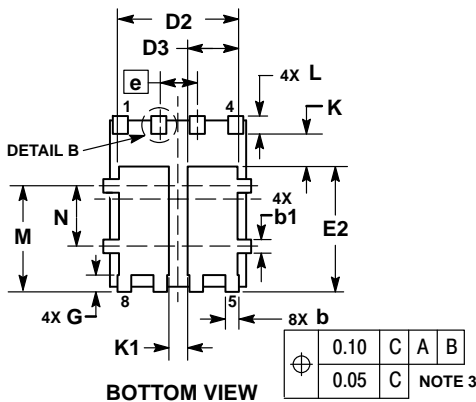


SIDE VIEW



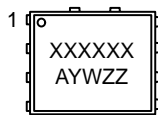
DETAIL A

DETAIL B  
ALTERNATE  
CONSTRUCTION



BOTTOM VIEW

GENERIC  
MARKING DIAGRAM\*

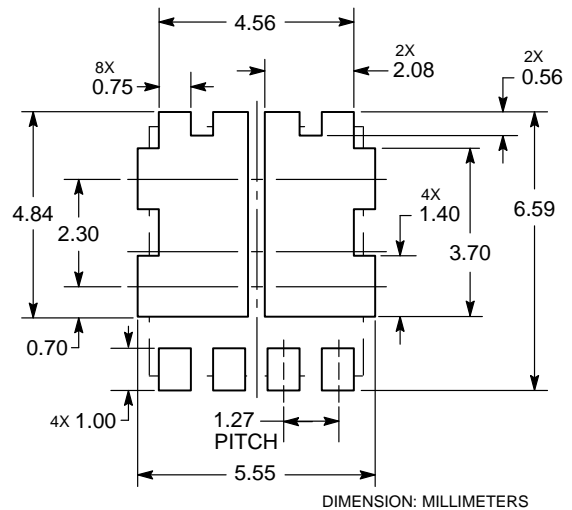


XXXXXX = Specific Device Code  
A = Assembly Location  
Y = Year  
W = Work Week  
ZZ = Lot Traceability

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	---	1.10
A1	---	---	0.05
b	0.33	0.42	0.51
b1	0.33	0.42	0.51
c	0.20	---	0.33
D	5.15 BSC		
D1	4.70	4.90	5.10
D2	3.90	4.10	4.30
D3	1.50	1.70	1.90
E	6.15 BSC		
E1	5.70	5.90	6.10
E2	3.90	4.15	4.40
e	1.27 BSC		
G	0.45	0.55	0.65
h	---	---	12 °
K	0.51	---	---
K1	0.56	---	---
L	0.48	0.61	0.71
M	3.25	3.50	3.75
N	1.80	2.00	2.20

SOLDERING FOOTPRINT\*



DIMENSION: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	98AON50417E	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	DFN8 5X6, 1.27P DUAL FLAG (SO8FL-DUAL)	PAGE 1 OF 1

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