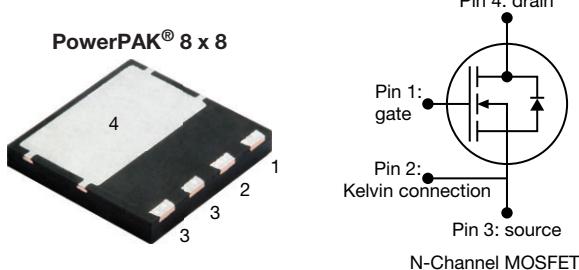


EF Series Power MOSFET With Fast Body Diode



FEATURES

- 4th generation E series technology
- Low figure-of-merit (FOM) $R_{on} \times Q_g$
- Low effective capacitance ($C_{o(er)}$)
- Reduced switching and conduction losses
- Avalanche energy rated (UIS)
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE
GREEN
(S-2008)

APPLICATIONS

- Server and telecom power supplies
- Switch mode power supplies (SMPS)
- Power factor correction power supplies (PFC)
- Lighting
 - High-intensity discharge (HID)
 - Fluorescent ballast lighting
- Industrial
 - Welding
 - Induction heating
 - Motor drives
 - Battery chargers
 - Solar (PV inverters)

PRODUCT SUMMARY	
V_{DS} (V) at T_J max.	650
$R_{DS(on)}$ typ. (Ω) at 25 °C	$V_{GS} = 10$ V 0.061
Q_g max. (nC)	75
Q_{gs} (nC)	20
Q_{gd} (nC)	17
Configuration	Single

ORDERING INFORMATION	
Package	PowerPAK 8 x 8
Lead (Pb)-free and halogen-free	SiHH070N60EF-T1GE3

ABSOLUTE MAXIMUM RATINGS ($T_C = 25$ °C, unless otherwise noted)				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		V_{DS}	600	V
Gate-source voltage		V_{GS}	± 30	
Continuous drain current ($T_J = 150$ °C)	V_{GS} at 10 V	I_D	36	A
	$T_C = 25$ °C		23	
Pulsed drain current ^a		I_{DM}	93	
Linear derating factor			1.6	W/°C
Single pulse avalanche energy ^b		E_{AS}	226	mJ
Maximum power dissipation		P_D	202	W
Operating junction and storage temperature range		T_J, T_{stg}	-55 to +150	°C
Drain-source voltage slope	$T_J = 125$ °C	dv/dt	100	V/ns
Reverse diode dv/dt ^d			50	

Notes

- Repetitive rating; pulse width limited by maximum junction temperature
- $V_{DD} = 140$ V, starting $T_J = 25$ °C, $L = 28.2$ mH, $R_g = 25$ Ω, $I_{AS} = 4$ A
- 1.6 mm from case
- $I_{SD} \leq I_D$, $di/dt = 900$ A/μs, starting $T_J = 25$ °C

THERMAL RESISTANCE RATINGS

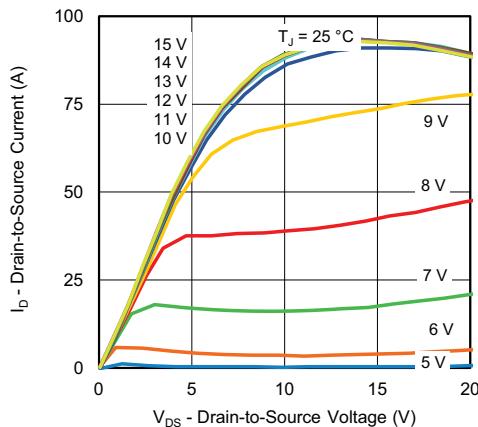
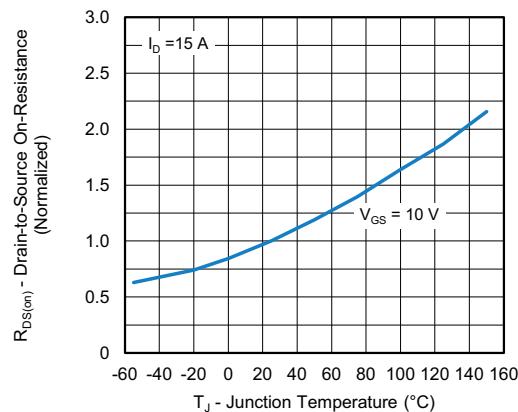
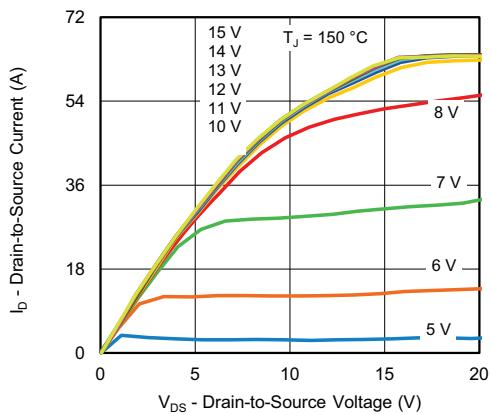
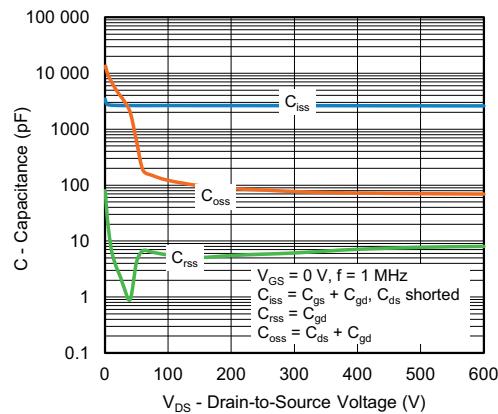
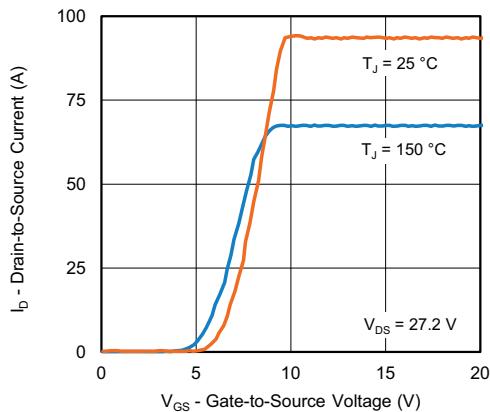
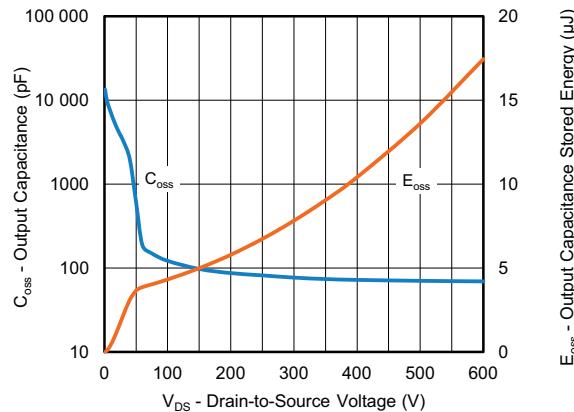
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	R_{thJA}	38	50	$^{\circ}\text{C}/\text{W}$
Maximum junction-to-case (drain)	R_{thJC}	0.48	0.62	

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0 \text{ V}$, $I_D = 250 \mu\text{A}$		600	-	-	V
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, $I_D = 20 \text{ mA}$		-	0.51	-	$^{\circ}\text{C}/\text{C}$
Gate-source threshold voltage (N)	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250 \mu\text{A}$		3	-	5	V
Gate-source leakage	I_{GSS}	$V_{GS} = \pm 20 \text{ V}$		-	-	± 100	nA
		$V_{GS} = \pm 30 \text{ V}$		-	-	± 1	μA
Zero gate voltage drain current	I_{DSS}	$V_{DS} = 480 \text{ V}$, $V_{GS} = 0 \text{ V}$		-	-	1	μA
		$V_{DS} = 480 \text{ V}$, $V_{GS} = 0 \text{ V}$, $T_J = 125 \text{ }^{\circ}\text{C}$		-	-	2	mA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS} = 10 \text{ V}$	$I_D = 15 \text{ A}$	-	0.061	0.071	Ω
Forward transconductance ^a	g_{fs}	$V_{DS} = 20 \text{ V}$, $I_D = 15 \text{ A}$		-	10.5	-	S
Dynamic							
Input capacitance	C_{iss}	$V_{GS} = 0 \text{ V}$, $V_{DS} = 100 \text{ V}$, $f = 1 \text{ MHz}$		-	2647	-	pF
Output capacitance	C_{oss}			-	122	-	
Reverse transfer capacitance	C_{rss}			-	6	-	
Effective output capacitance, energy related ^a	$C_{o(er)}$	$V_{DS} = 0 \text{ V}$ to 480 V , $V_{GS} = 0 \text{ V}$		-	90	-	
Effective output capacitance, time related ^b	$C_{o(tr)}$			-	560	-	
Total gate charge	Q_g	$V_{GS} = 10 \text{ V}$	$I_D = 15 \text{ A}$, $V_{DS} = 480 \text{ V}$	-	50	75	nC
Gate-source charge	Q_{gs}			-	20	-	
Gate-drain charge	Q_{gd}			-	17	-	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 480 \text{ V}$, $I_D = 15 \text{ A}$, $V_{GS} = 10 \text{ V}$, $R_g = 9.1 \Omega$		-	36	72	ns
Rise time	t_r			-	79	119	
Turn-off delay time	$t_{d(off)}$			-	55	83	
Fall time	t_f			-	38	76	
Gate input resistance	R_g	$f = 1 \text{ MHz}$		0.3	0.7	1.4	Ω
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	I_S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	36	A
Pulsed diode forward current	I_{SM}			-	-	93	
Diode forward voltage	V_{SD}	$T_J = 25 \text{ }^{\circ}\text{C}$, $I_S = 15 \text{ A}$, $V_{GS} = 0 \text{ V}$		-	-	1.2	V
Reverse recovery time	t_{rr}	$T_J = 25 \text{ }^{\circ}\text{C}$, $I_F = I_S = 15 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$, $V_R = 400 \text{ V}$		-	136	272	ns
Reverse recovery charge	Q_{rr}			-	0.9	1.8	
Reverse recovery current	I_{RRM}			-	12	-	

Notes

- a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS}
b. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS}

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Fig. 1 - Typical Output Characteristics

Fig. 4 - Normalized On-Resistance vs. Temperature

Fig. 2 - Typical Output Characteristics

Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

Fig. 3 - Typical Transfer Characteristics

Fig. 6 - C_{oss} and E_{oss} vs. V_{DS}

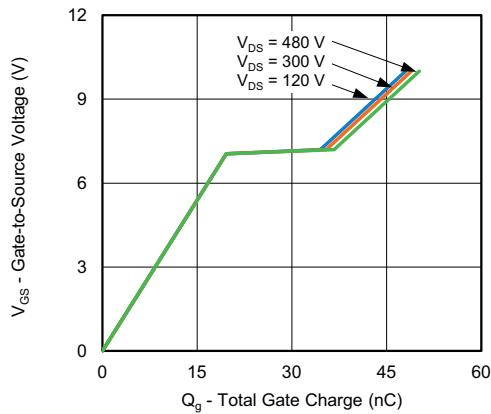


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

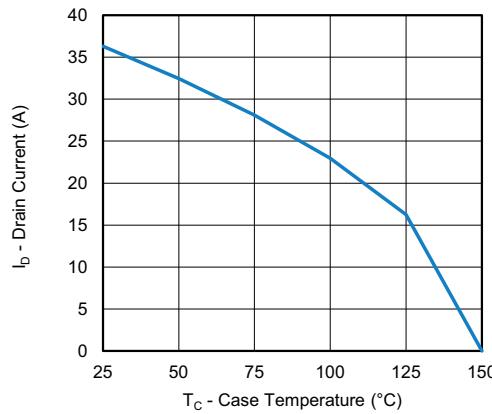


Fig. 10 - Maximum Drain Current vs. Case Temperature

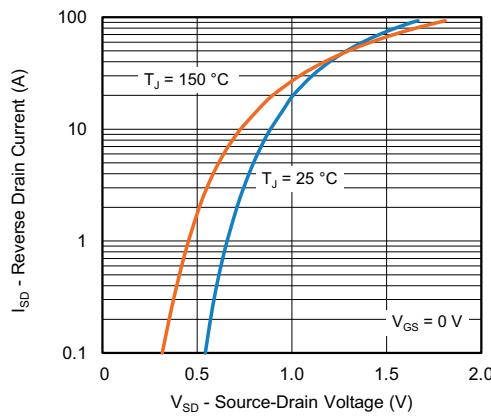


Fig. 8 - Typical Source-Drain Diode Forward Voltage

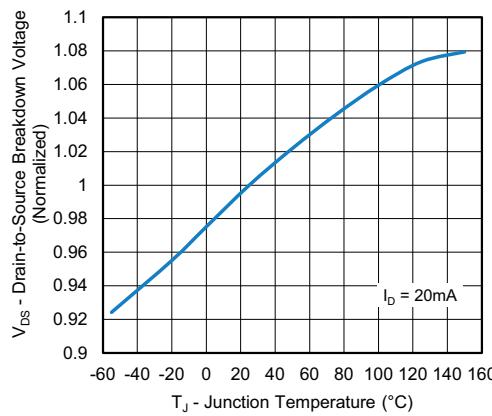


Fig. 11 - Temperature vs. Drain-to-Source Voltage

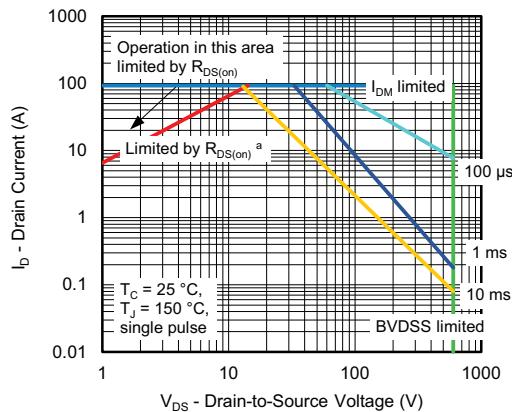


Fig. 9 - Maximum Safe Operating Area

Note

a. $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified

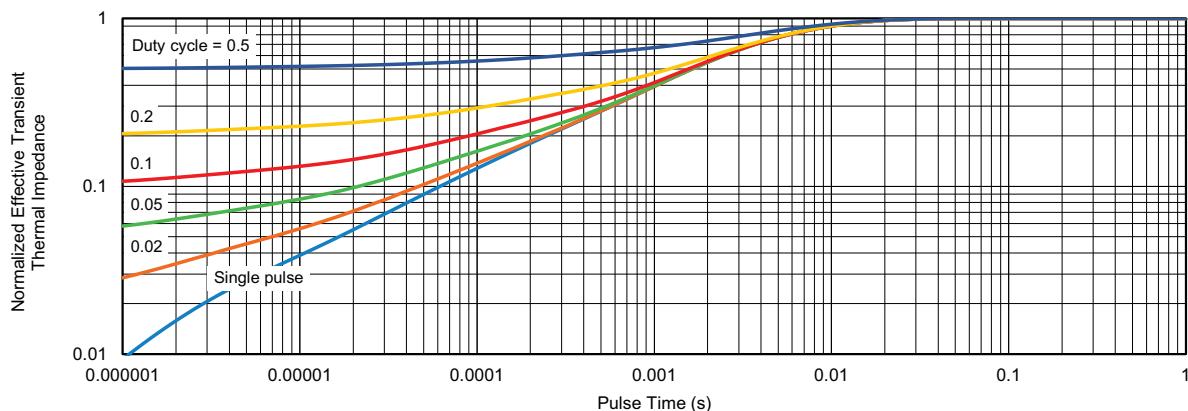


Fig. 12 - Normalized Transient Thermal Impedance, Junction-to-Case

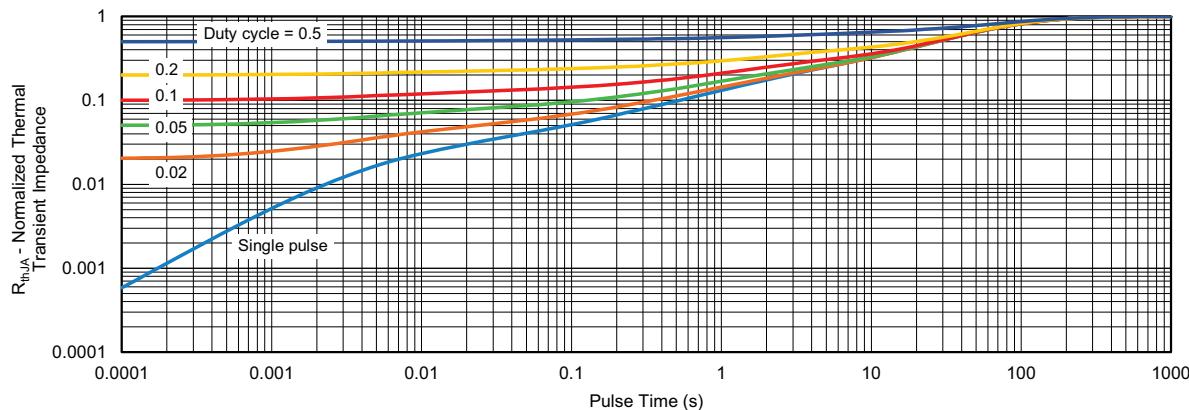


Fig. 13 - Normalized Transient Thermal Impedance, Junction-to-Ambient

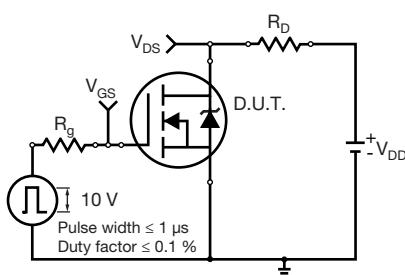


Fig. 14 - Switching Time Test Circuit

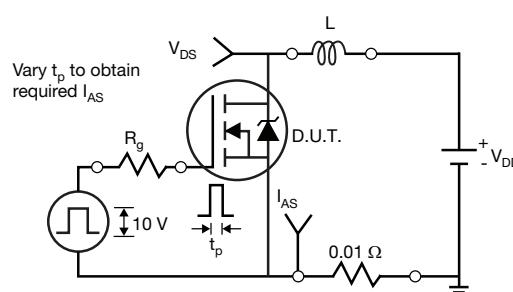


Fig. 16 - Unclamped Inductive Test Circuit

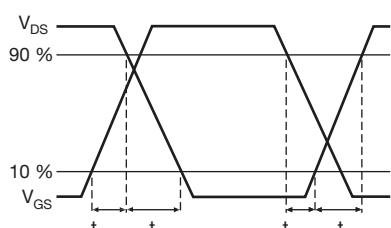


Fig. 15 - Switching Time Waveforms

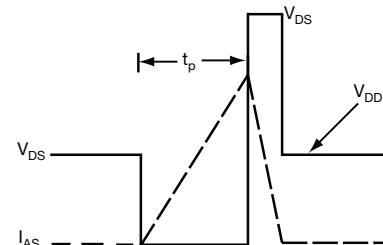


Fig. 17 - Unclamped Inductive Waveforms

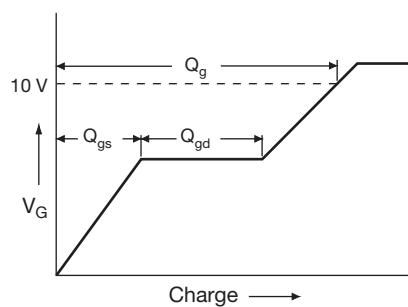


Fig. 18 - Basic Gate Charge Waveform

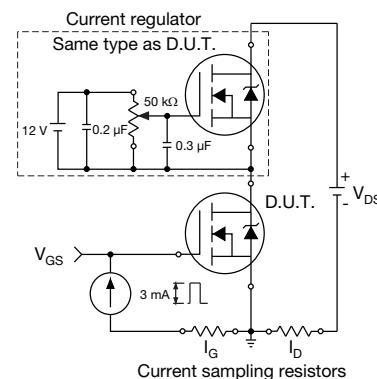


Fig. 19 - Gate Charge Test Circuit

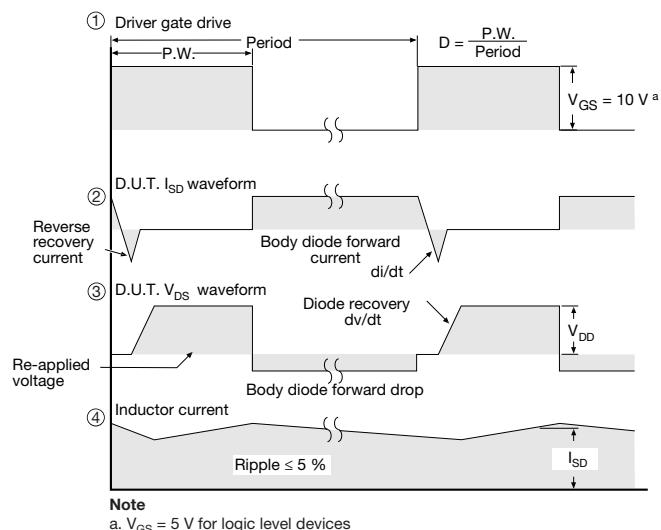
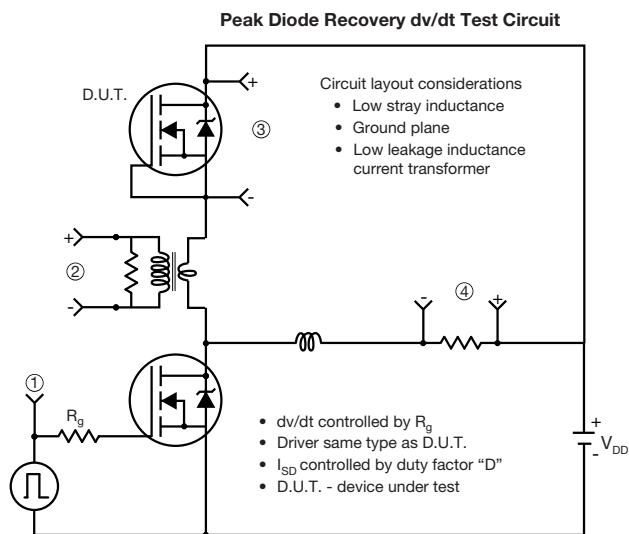
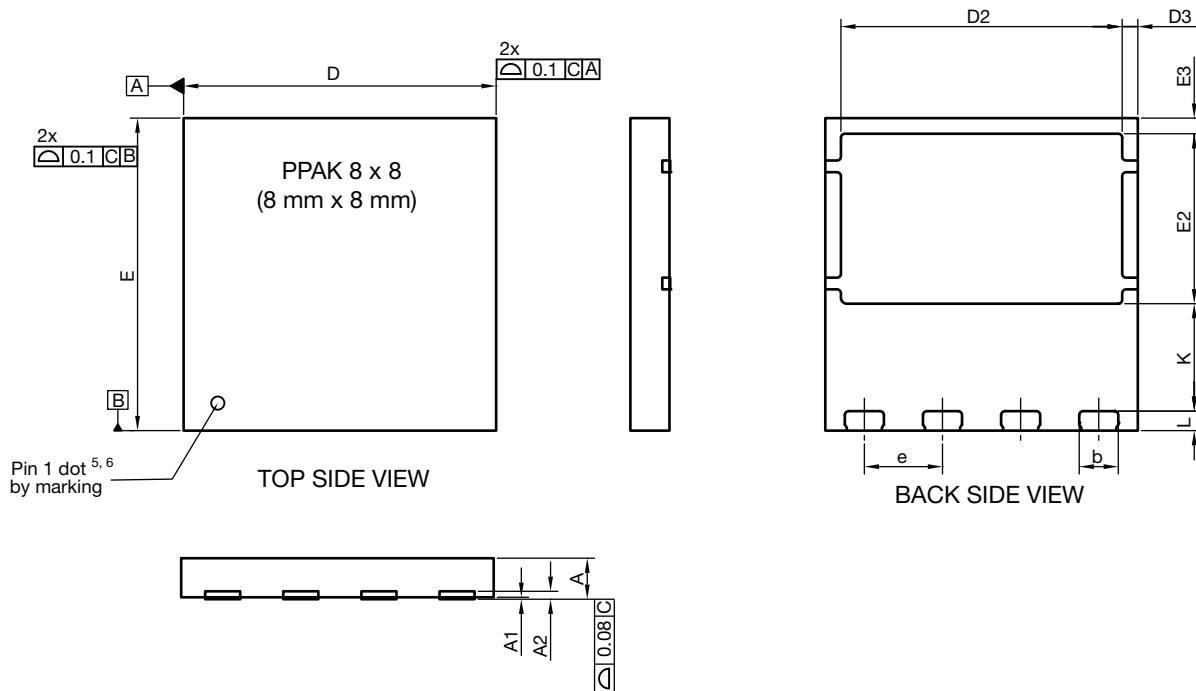


Fig. 20 - For N-Channel

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PowerPAK® 8 x 8 Case Outline

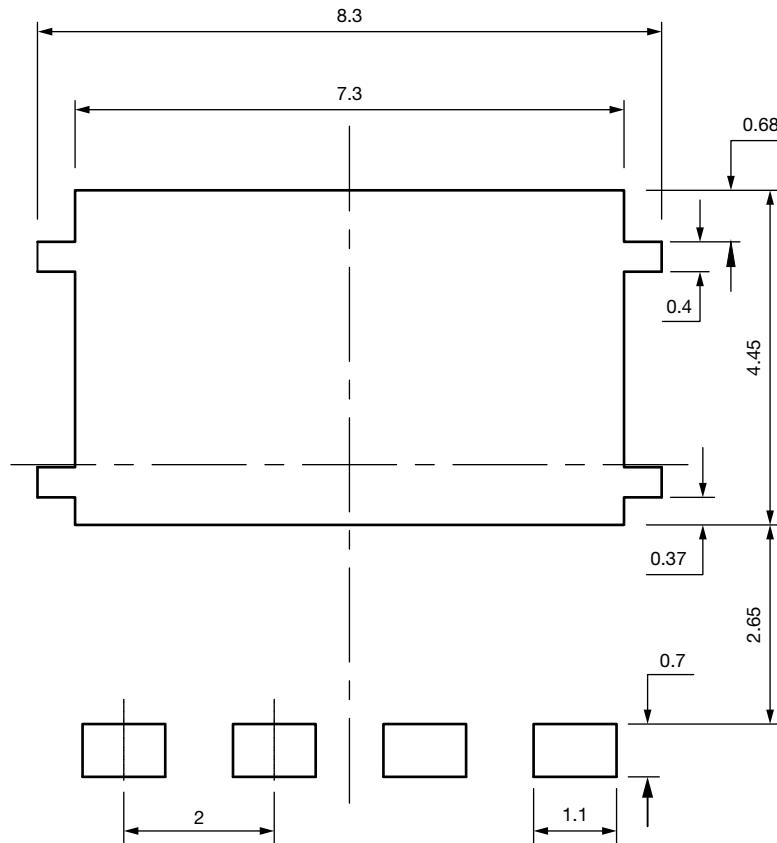


DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.95	1.00	1.05	0.037	0.039	0.041
A1	0.00	-	0.05	0.000	-	0.002
A2	020 ref.			0.008 ref.		
b	0.95	1.00	1.05	0.037	0.039	0.041
D	7.90	8.00	8.10	0.311	0.315	0.319
D2	7.10	7.20	7.30	0.280	0.283	0.287
D3	0.40 BSC			0.016 BSC		
e	2.00 BSC			0.079 BSC		
E	7.90	8.00	8.10	0.311	0.315	0.319
E2	4.30	4.35	4.40	0.169	0.171	0.173
E3	0.40 BSC			0.016 BSC		
K	2.75 BSC			0.108 BSC		
L	0.45	0.50	0.55	0.018	0.020	0.022
N ⁽³⁾	8			8		

Notes

- (1) Use millimeters as the primary measurement
- (2) Dimensioning and tolerances conform to ASME Y14.5 M - 1994
- (3) N is the number of terminals
- (4) The pin 1 identifier must be existed on the top surface of the package by using indentation mark or other feature of package body
- (5) Exact shape and size of this feature is optional

ECN: E20-0518-Rev. B, 28-Sep-2020
 DWG: 6041

Recommended Minimum PADs for PowerPAK® 8 mm x 8 mm

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