Description

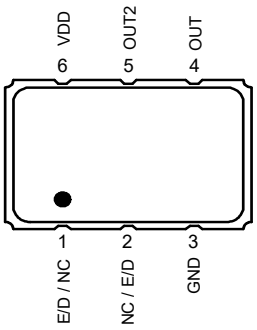
The Renesas XL devices (XO and VCXO options) are ultra-precision crystal oscillators with 750 to 890fs typical phase jitter over 12kHz to 20MHz bandwidth. Available in a wide frequency range from 0.750MHz to 1350MHz, the XL series crystal oscillators utilize a family of proprietary ASICs, with a key focus on noise reduction technologies.

The 3rd order Delta Sigma Modulator reduces noise to the levels that are comparable to traditional Bulk Quartz and SAW oscillators. With short lead-time, low cost, low noise, wide frequency range, excellent ambient performance, the XL devices are an excellent choice over the conventional technologies. The XL (XO option) devices have stabilities as tight as ±20ppm and the XL (VCXO option) devices have ±50ppm APR. Either option provides extremely quick delivery for both standard and custom frequencies.

Pin Assignments

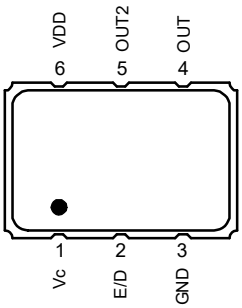
(XO Option)

NOTE: To minimize power supply line noise, a 0.01µF bypass capacitor should be placed between V_{DD} (Pin 6) and GND (Pin 3).



(VCXO Option)

NOTE: To minimize power supply line noise, a 0.01µF bypass capacitor should be placed between V_{DD} (Pin 6) and GND (Pin 3).



Features

- Output types: LVDS, LVPECL, LVCMOS
- Phase jitter (12kHz to 20MHz): 750fs to 890fs typical
- Supply voltage: 2.5V or 3.3V
- Package options:
  - 3.2 × 2.5 × 1.0 mm (not available for VCXO)
  - 5.0 × 3.2 × 1.2 mm
  - 7.0 × 5.0 × 1.3 mm
- Operating temperature: -20°C to +70°C
  - Frequency stability options: ±20, ±25, ±50, or ±100 ppm (XO only)
  - ±50ppm APR (VCXO only)
- Operating temperature: -40°C to +85°C
  - Frequency stability options: ±25, ±50, or ±100 ppm (XO only)
  - ±50ppm APR (VCXO only)
- Operating temperature: -40°C to +105°C (XO only)
  - Frequency stability options: ±50 or ±100 ppm
- kV of 85ppm/volt typical from 0.5VDC to VDD (VCXO only)
  - Better than ±10% linearity for Vc range

Pin Descriptions

Table 1. XO Pin Description

Number	Name	Description
1	E/D NC	Enable/Disable [a][b] No connect
2	NC E/D	No connect Enable/Disable [a][b]
3	GND	Connect to ground
4	OUT	Output
5	OUT2	Complementary output [c]
6	V_{DD}	Supply voltage

[a] Pulled high internally.

[b] Low = output disabled.

[c] Do not connect for LVCMOS. For XLVCMOS, both OUT and OUT2 are ON and in opposite phase.

See Ordering Information (XO) for more details.

Table 2. VCXO Pin Description

Number	Name	Description
1	Vc	Voltage control
2	E/D	Enable/Disable [a][b]
3	GND	Connect to ground
4	OUT	Output
5	OUT2	Complementary output (NC LVCMOS)
6	V_{DD}	Supply voltage

[a] Pulled high internally.

[b] Low = output disabled.

See Ordering Information (VCXO) for more details.

Ordering Information (XO)

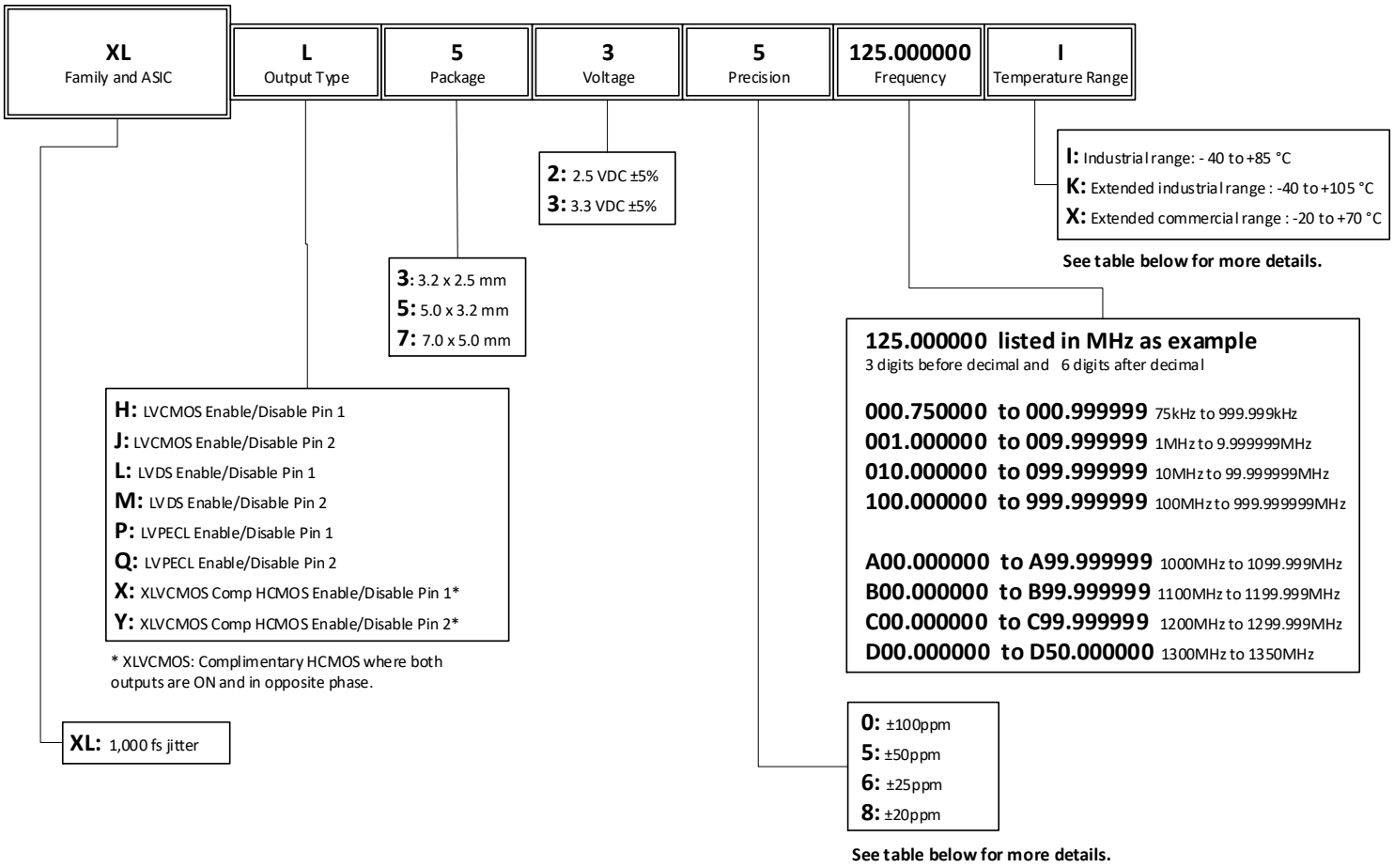
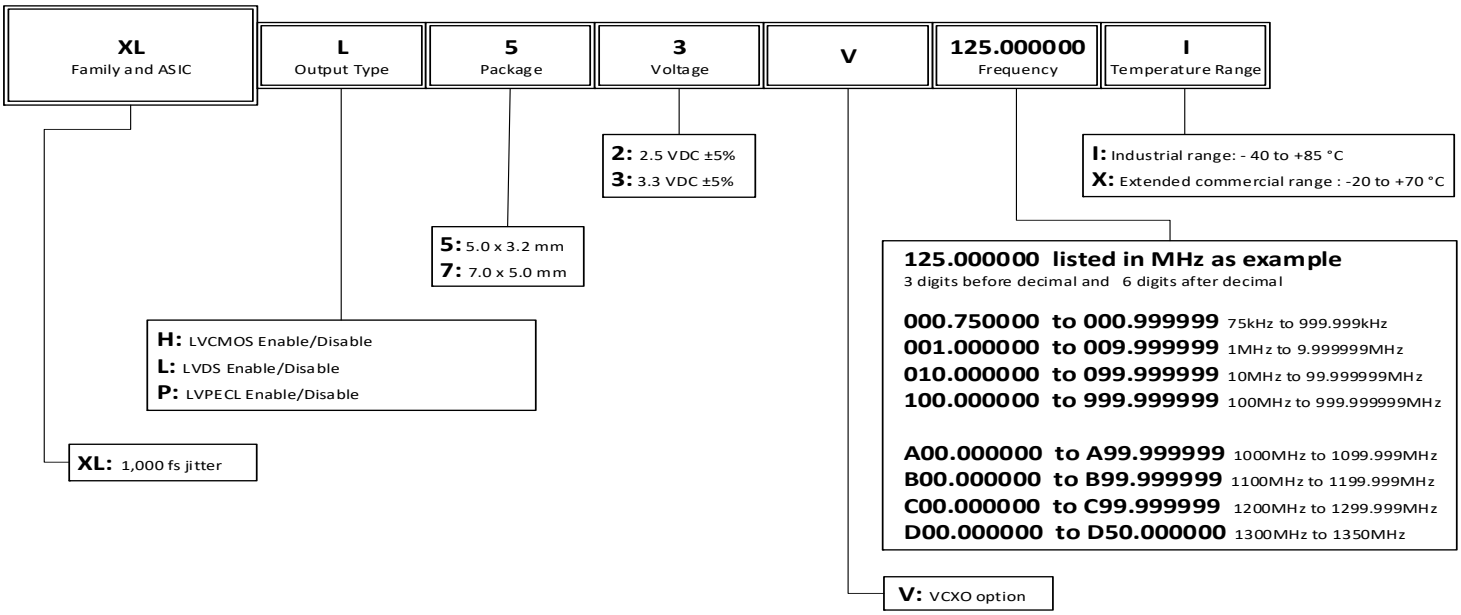


Table 3. Frequency Stability and Operating Temperature Decoder

"Precision" and "Temperature Range" Codes	Operating Temperature	Frequency Stability		
		Minimum	Maximum	Units
"8" and "X"	-20°C to +70°C	-20	+20	ppm
"6" and "X"	-20°C to +70°C	-25	+25	ppm
"5" and "X"	-20°C to +70°C	-50	+50	ppm
"0" and "X"	-20°C to +70°C	-100	+100	ppm
"6" and "I"	-40°C to +85°C	-25	+25	ppm
"5" and "I"	-40°C to +85°C	-50	+50	ppm
"0" and "I"	-40°C to +85°C	-100	+100	ppm
"5" and "K"	-40° to +105°C	-50	+50	ppm
"0" and "K"	-40° to +105°C	-100	+100	ppm

Ordering Information (VCXO)



Contents

Description . . . 1
Pin Assignments . . . 1
(XO Option) . . . 1
(VCXO Option) . . . 1
Features . . . 1
Pin Descriptions . . . 2
Ordering Information (XO) . . . 3
Ordering Information (VCXO) . . . 4
Absolute Maximum Ratings . . . 6
ESD Compliance . . . 6
Mechanical Testing . . . 6
Solder Reflow Profile . . . 6
DC Electrical Characteristics . . . 7
AC Electrical Characteristics . . . 10
Output Waveforms – LVDS . . . 13
Output Waveforms – LVPECL . . . 13
Output Waveforms – LVCMOS . . . 14
Package Outline Drawings . . . 15
Marking Diagrams . . . 15
Revision History . . . 16

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the device. These ratings, which are standard values for Renesas commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Table 4. Absolute Maximum Ratings

Item	Rating					
V_{DD}	-0.5 to +5.0V					
E/D	-0.5V to V_{DD} + 0.5V					
OUT	-0.5V to V_{DD} + 0.5V					
Storage Temperature	-55°C to 125°C					
Maximum Junction Temperature	125°C					
Core Current	65mA maximum					
Theta J_A	JU6	75.9 °C/W	JS6	89.6 °C/W	JX6	94.7 °C/W
Theta J_B	7.0 × 5.0 × 1.3 mm	48.6°C/W	5.0 × 3.2 × 1.2 mm	54.3 °C/W	3.2 × 2.5 × 1.0 mm	66.8 °C/W

ESD Compliance

Table 5. ESD Compliance

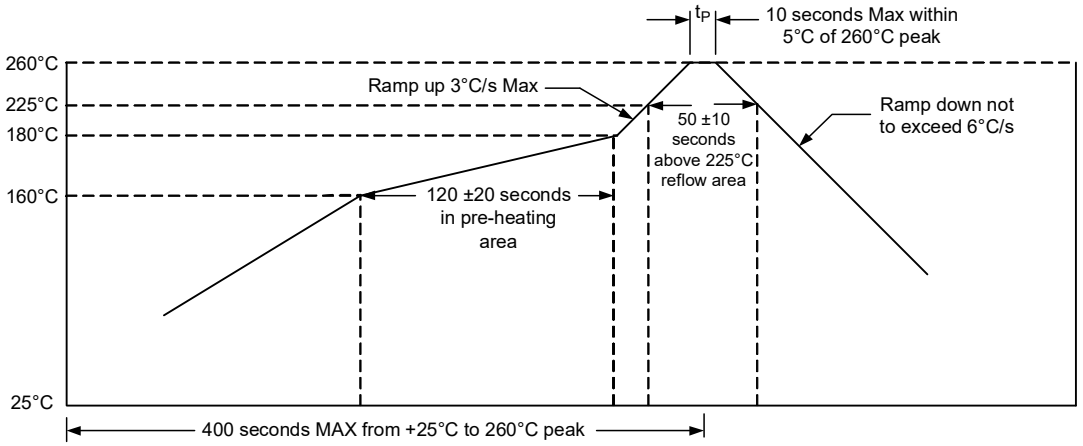
Human Body Model (HBM	1000V
Machine Model (MM)	150V

Mechanical Testing

Table 6. Mechanical Testing

Parameter	Test Method
Mechanical Shock	Drop from 75cm to hardwood surface–3 times.
Mechanical Vibration	10–55Hz, 1.5mm amplitude, 1 minute sweep; 2 hours each in 3 directions (X, Y, Z).
High Temperature Burn-in	Under power at 125°C for 2000 hours.
Hermetic Seal	He pressure: 4 ±1kgf/cm^2 2 hour soak.

Solder Reflow Profile



DC Electrical Characteristics

Table 7. 3.3V IDD DC Electrical Characteristics

V_{DD} = 3.3V ±5%, T_A = -20°C to +70°C; -40°C to +85°C, -40°C to +105°C.

Symbol	Parameter	Output Type	Conditions	Minimum	Typical	Maximum	Units
I_{DD}	Power Supply Current	LVDS	0.75MHz to 40MHz.	-	32	37	mA
			40+MHz to 220MHz.	-	40	47	
			220+MHz to 630MHz.	-	49	57	
			630+MHz to 1350MHz.	-	72	100	
		LVPECL[a]	0.75MHz to 40MHz.	-	26	31	
			40+MHz to 220MHz.	-	38	45	
			220+MHz to 630MHz.	-	56	64	
			630+MHz to 1350MHz.	-	96	120	
		LVCMOS	0.75MHz to 20MHz.	-	27	32	
			20+MHz to 50MHz.	-	32	35	
			50+MHz to 130MHz.	-	43	47	
			130+MHz to 200MHz.	-	48	55	
			200+MHz to 250MHz.	-	48	60	

[a] Without termination resistors.

Table 8. 2.5V IDD DC Electrical Characteristics

V_{DD} = 2.5V ±5%, T_A = -20°C to +70°C; -40°C to +85°C, -40°C to +105°C.

Symbol	Parameter	Output Type	Conditions	Minimum	Typical	Maximum	Units
I_{DD}	Power Supply Current	LVDS	0.75MHz to 20MHz.	-	24	26	mA
			20+MHz to 220MHz.	-	29	34	
			220+MHz to 630MHz.	-	36	44	
			630+MHz to 1000MHz.	-	46	65	
		LVPECL[a]	0.75MHz to 20MHz.	-	20	33	
			20+MHz to 220MHz.	-	28	41	
			220+MHz to 630MHz.	-	41	63	
			630+MHz to 1000MHz.	-	56	72	
		LVCMOS	0.75MHz to 20MHz.	-	17	22	
			20+MHz to 50MHz.	-	23	25	
			50+MHz to 100MHz.	-	28	29	
			100+MHz to 130MHz.	-	30	32	
			130+MHz to 160MHz.	-	32	35	
			160+MHz to 180MHz.	-	33	37	

[a] Without termination resistors.

Table 9. LVDS DC Electrical Characteristics

V_{DD} = 3.3V, 2.5V ±5%, T_A = -20°C to +70°C; -40°C to +85°C, -40°C to +105°C. Below are guaranteed for listed standard frequencies.

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage	V_{DD} = 3.3V ±5%.	-	-	0.6	V
		V_{DD} = 2.5V ±5%.	-	-	0.4	
V_{OS}	Output Offset Voltage	V_{DD} = 3.3V ±5%.	-	-	1.3	
		V_{DD} = 2.5V ±5%.	-	-	1.25	
V_{IH}	Enable/Disable Input High Voltage (Output enabled)	-	70% V_{DD}	-	-	
V_{IL}	Enable/Disable Input Low Voltage (Output disabled)	-	-	-	30% V_{DD}	

Table 10. LVPECL DC Electrical Characteristics

V_{DD} = 3.3V, 2.5V ±5%, T_A = -20°C to +70°C; -40°C to +85°C, -40°C to +105°C. Below are guaranteed for listed standard frequencies.

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage	V_{DD} = 3.3V ±5%.	2.055		2.405	V
		V_{DD} = 2.5V ±5%.	-	1.4	-	
V_{OS}	Output Offset Voltage	V_{DD} = 3.3V ±5%.	1.305		1.65	
		V_{DD} = 2.5V ±5%.	-	0.68	-	
V_{IH}	Enable/Disable Input High Voltage (Output enabled)	-	70% V_{DD}	-	-	
V_{IL}	Enable/Disable Input Low Voltage (Output disabled)	-	-	-	30% V_{DD}	

Table 11. LVCMOS DC Electrical Characteristics

V_{DD} = 3.3V, 2.5V ±5%, T_A = -20°C to +70°C; -40°C to +85°C, -40°C to +105°C. Below are guaranteed for listed standard frequencies.

Symbol	Parameter	Conditions		Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage	V_{DD} = 3.3V ±5%.	0.75MHz to 150MHz.	90% V_{DD}	-	-	V
			150+MHz to 250MHz.	80% V_{DD}	-	-	
		V_{DD} = 2.5V ±5%.	0.75MHz to 160MHz.	90% V_{DD}	-	-	
			160+MHz to 180MHz.	80% V_{DD}	-	-	
V_{OL}	Output Low Voltage	V_{DD} = 3.3V ±5%.	0.75MHz to 150MHz.	-	-	10% V_{DD}	
			150+MHz to 250MHz.	-	-	20% V_{DD}	
		V_{DD} = 2.5V ±5%.	0.75MHz to 160MHz.	-	-	10% V_{DD}	
			160+MHz to 180MHz.	-	-	20% V_{DD}	
V_{IH}	Enable/Disable Input High Voltage (Output enabled)	-	-	70% V_{DD}	-	-	
V_{IL}	Enable/Disable Input Low Voltage (Output disabled)	-	-	-	-	30% V_{DD}	

AC Electrical Characteristics

Table 12. 3.3V AC Electrical Characteristics

V_{DD} = 3.3V ±5%, T_A = -20°C to +70°C; -40°C to +85°C, -40°C to +105°C.

Symbol	Parameter	Test Condition		Minimum	Typical	Maximum	Units
F	Output Frequency Range	LVDS.		0.75	-	1350	MHz
		LVPECL.		0.75	-	1350	
		LVCMOS.		0.75	-	250	
	Frequency Stability	Temperature = -20°C to +70°C.		-20 -25 -50 -100	-	+20 +25 +50 +100	ppm
		Temperature = -40°C to +85°C.		-25 -50 -100	-	+25 +50 +100	ppm
		Temperature = -40°C to +105°C.		-50 -100	-	+50 +100	ppm
	Output Load	LVDS.	Differential.	-	100	-	Ω
		LVPECL.	V_{DD} - 2.0V.	-	50	-	
		LVCMOS.	To GND.	-	15	-	pF
T_{ST}	Start-up Time	Output valid time after V_{DD} meets minimum specified level.		-	-	10	ms
t_R	Output Rise Time	LVDS.	20% to 80% Vpp.	-	-	400	ps
		LVPECL.		-	-	400	
		LVCMOS.	10% to 90% $V_{DD.}$	-	-	3	ns
t_F	Output Fall Time	LVDS.	80% to 20% Vpp.	-	-	400	ps
		LVPECL.		-	-	400	
		LVCMOS.	90% to 10% $V_{DD.}$	-	-	3	ns
O_{DC}	Output Clock Duty Cycle	LVDS.		47	-	53	%
		LVPECL.		47	-	53	
		LVCMOS.		47	-	53	
T_{OE}	Output Enable/ Disable Time	-		-	-	100	ns
J_{PER}	Period Jitter, RMS	LVDS.		-	3	-	ps
		LVPECL.		-	5.8	-	
		LVCMOS.	F_{OUT} = 125MHz.	-	5	-	
R_J	Random Jitter	LVDS.		-	1.3	-	ps
		LVPECL.		-	1.29	-	
		LVCMOS.	F_{OUT} = 125MHz.	-	0.6	-	

Table 12. 3.3V AC Electrical Characteristics (Cont.)

V_{DD} = 3.3V ±5%, T_A = -20°C to +70°C; -40°C to +85°C, -40°C to +105°C.

Symbol	Parameter	Test Condition		Minimum	Typical	Maximum	Units
D_J	Deterministic Jitter	LVDS.		-	5.8	-	ps
		LVPECL.		-	9.3	-	
		LVCMOS.	F_{OUT} = 125MHz.	-	10	-	
T_J	Total Jitter	LVDS.		-	23.6	-	ps
		LVPECL.		-	27.7	-	
		LVCMOS.	F_{OUT} = 125MHz.	-	19	-	
f_{JITTER}	Phase Jitter (12kHz–20MHz)	LVDS.		-	890	-	fs
		LVPECL.		-	860	-	
		LVCMOS.	F_{OUT} = 125MHz.	-	750	-	

Table 13. 2.5V AC Electrical Characteristics

V_{DD} = 2.5V ±5%, T_A = -20°C to +70°C; -40°C to +85°C, -40°C to +105°C.

Symbol	Parameter	Test Condition		Minimum	Typical	Maximum	Units
F	Output Frequency Range	LVDS.		0.75	-	1000	MHz
		LVPECL.		0.75	-	1000	
		LVCMOS.		0.75	-	180	
	Frequency Stability	Temperature = -20°C to +70°C.		-20 -25 -50 -100	-	+20 +25 +50 +100	ppm
		Temperature = -40°C to +85°C.		-25 -50 -100	-	+25 +50 +100	ppm
		Temperature = -40°C to +105°C.		-50 -100	-	+50 +100	ppm
	Output Load	LVDS.	Differential.	-	100	-	Ω
		LVPECL.	V_{DD} - 2.0V.	-	50	-	
		LVCMOS.	To GND.	-	15	-	pF
T_{ST}	Start-up Time	Output valid time after V_{DD} meets minimum specified level.		-	-	10	ms
t_R	Output Rise Time	LVDS.	20% to 80% Vpp.	-	-	400	ps
		LVPECL.		-	-	400	
		LVCMOS.	10% to 90% $V_{DD.}$	-	-	3.5	ns
t_F	Output Fall Time	LVDS.	80% to 20% Vpp.	-	-	400	ps
		LVPECL.		-	-	400	
		LVCMOS.	90% to 10% $V_{DD.}$	-	-	3	ns

Table 13. 2.5V AC Electrical Characteristics (Cont.)

V_{DD} = 2.5V ±5%, T_A = -20°C to +70°C; -40°C to +85°C, -40°C to +105°C.

Symbol	Parameter	Test Condition		Minimum	Typical	Maximum	Units
O_{DC}	Output Clock Duty Cycle	LVDS.		47	-	53	%
		LVPECL.		47	-	53	
		LVCMOS.		47	-	53	
T_{OE}	Output Enable/ Disable Time	—		-	-	100	ns
J_{PER}	Period Jitter, RMS	LVDS.		-	4	-	ps
		LVPECL.		-	5.12	-	
		LVCMOS.	F_{OUT} = 125MHz.	-	3.3	-	
R_J	Random Jitter	LVDS.		-	1.4	-	ps
		LVPECL.		-	1.36	-	
		LVCMOS.	F_{OUT} = 125MHz.	-	1.3	-	
D_J	Deterministic Jitter	LVDS.		-	9.2	-	ps
		LVPECL.		-	10	-	
		LVCMOS.	F_{OUT} = 125MHz.	-	6.7	-	
T_J	Total Jitter	LVDS.		-	29.2	-	ps
		LVPECL.		-	29.3	-	
		LVCMOS.	F_{OUT} = 125MHz.	-	25.6	-	
f_{JITTER}	Phase Jitter (12kHz–20MHz)	LVDS.		-	1040	-	fs
		LVPECL.		-	1200	-	
		LVCMOS.	F_{OUT} = 125MHz.	-	850	-	

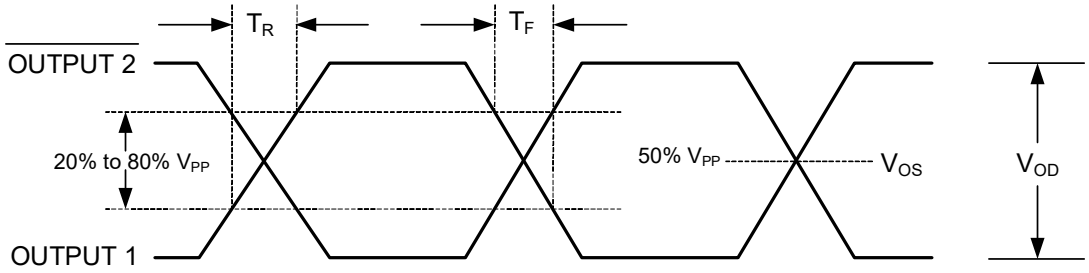
Notes for all AC Electrical Characteristics tables:

[1] All jitter values provided at 156.25MHz, unless noted otherwise.

[2] Stability is inclusive of 25°C tolerance, operating temperature range, input voltage change, load change, aging, shock and vibration.

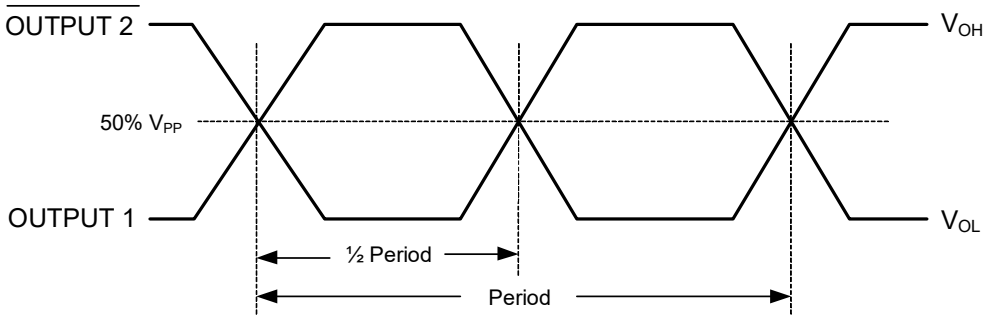
Output Waveforms – LVDS

Output Levels/Rise Time/Fall Time Measurements



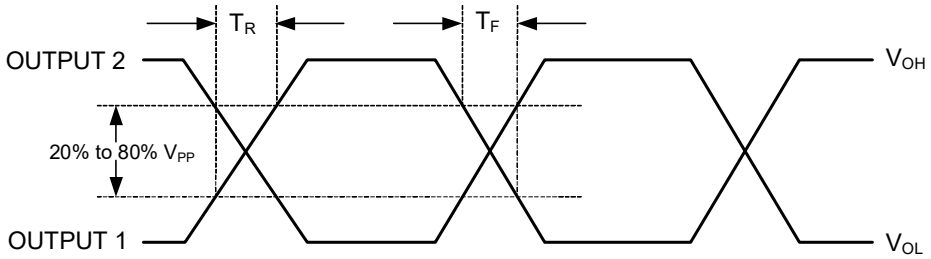
Oscillator Symmetry

Ideally, Symmetry should be 50/50 for ½ period –Other expressions are 45/55 or 55/45

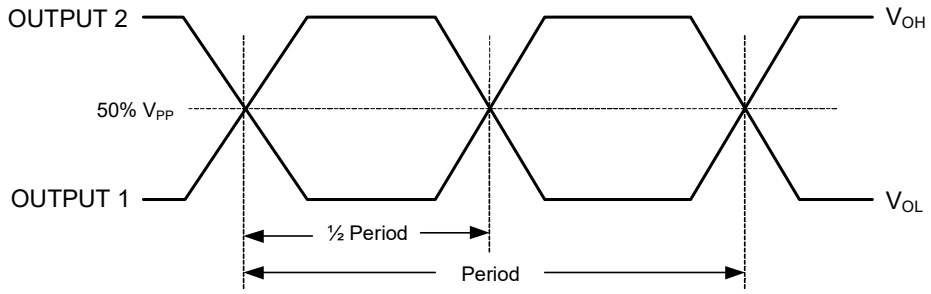


Output Waveforms – LVPECL

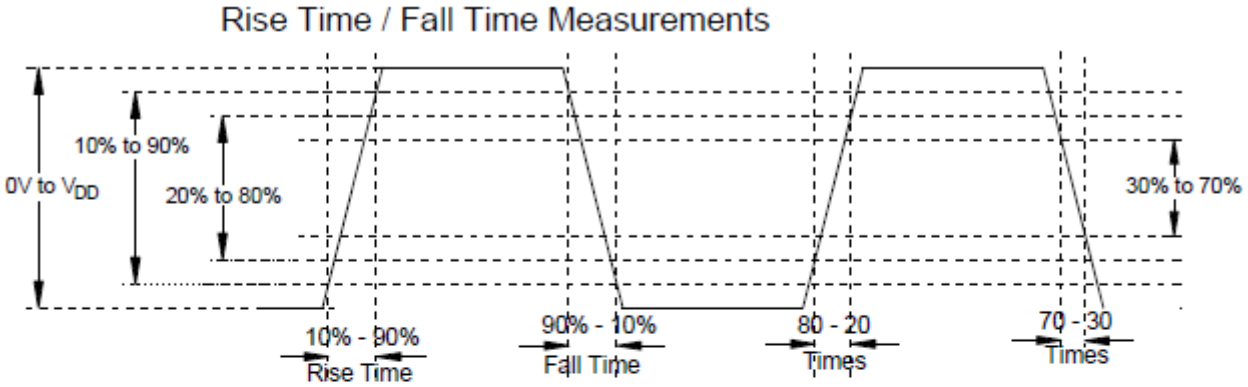
Rise Time/Fall Time Measurements

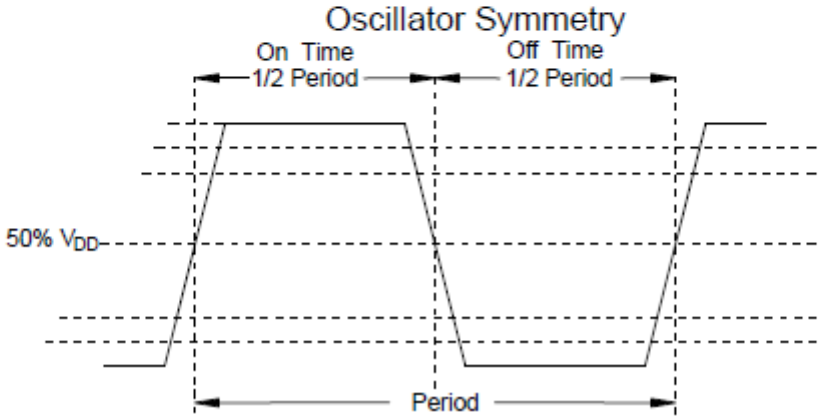


Oscillator Symmetry



Output Waveforms – LVCMOS



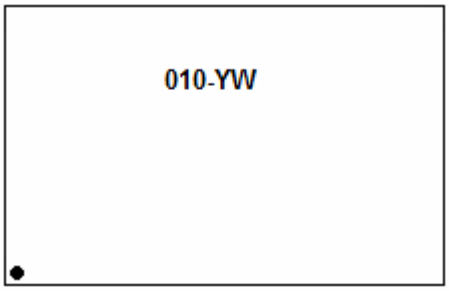


Package Outline Drawings

The package outline drawings (JS6, JX6, JU6) are appended at the end of this document. The package information is the most current data available.

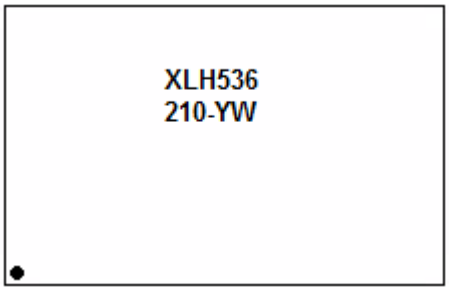
Marking Diagrams

JX6 3.2 × 2.5 mm Package Option (example based on XLH320010.000000I)



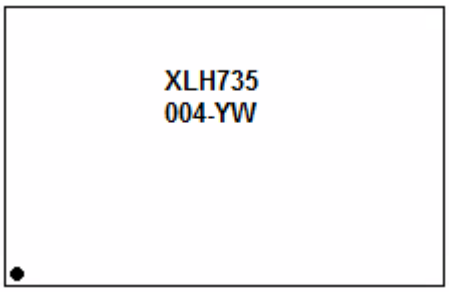
- Line 1:
  - “010” denotes last three digits to the left of the decimal point as shown in the above example. This number will vary depending upon the frequency value selected in the orderable part number.
  - “YW” denotes the last digit of the year and work week the part was assembled.

JS6 5.0 × 3.2 mm Package Option (example based on XLH536210.380000I)



- Line 1:
  - “XL” = family; “H” = output type; “5” = package size; “3” = voltage; “6” = precision level. This number will vary depending upon the output type, voltage, and precision values selected in the orderable part number.
- Line 2:
  - “210” denotes last three digits to the left of the decimal point as shown in the above example. This number will vary depending upon the frequency value selected in the orderable part number.
  - “YW” denotes the last digit of the year and work week the part was assembled.

JU6 7.0 × 5.0 mm Package Option (example based on XLH735004.915200X)

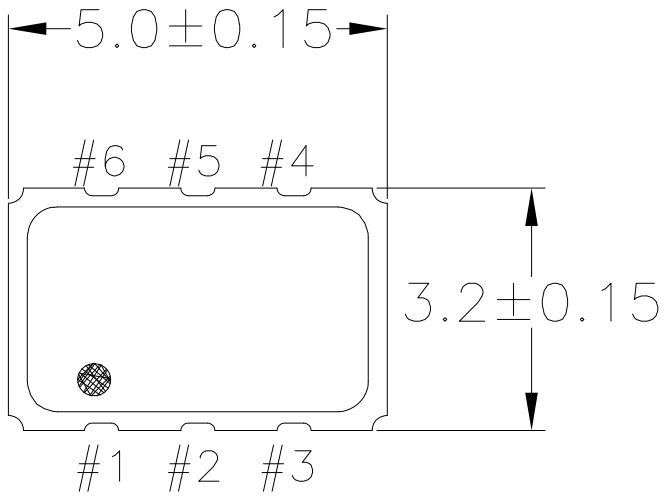


- Line 1:
  - “XL” = family; “H” = output type; “7” = package size; “3” = voltage; “5” = precision level. This number will vary depending upon the output type, voltage, and precision values selected in the orderable part number.
- Line 2:
  - “004” denotes last three digits to the left of the decimal point as shown in the above example. This number will vary depending upon the frequency value selected in the orderable part number.
  - “YW” denotes the last digit of the year and work week the part was assembled.

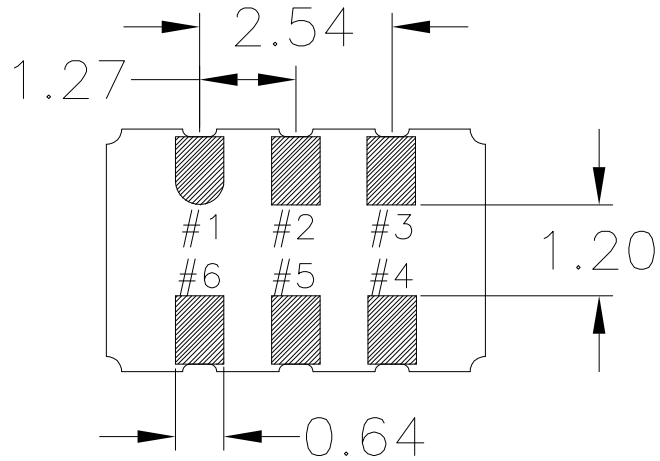
Revision History

Revision Date	Description of Change
March 2, 2022	Changed Output Duty Cycle minimum and maximum values in Table 12 and Table 13 from 45% to 47% and 55% to 53% respectively.
January 11, 2022	▪ Removed Aging parameters in Table 12 and Table 13. ▪ Added footnote 2 after Table 13.
December 1, 2021	Updated Frequency Stability values in Table 12 and Table 13.
November 23, 2021	Added Frequency Stability and Operating Temperature Decoder table after Ordering Information.
August 18, 2021	Moved XO and VCXO ordering information tables to be just after Pin Descriptions.
January 19, 2021	▪ Removed 4-pin package description table, figure, and package drawing references. ▪ Added footnote for pin 5 in Table 1. ▪ Added footnote under “Output Type” in XO Ordering Information.
January 12, 2021	Added Marking Diagrams section and updated Package Outline Drawings links.
October 27, 2020	Added pin counts to Output Type in XO ordering table.
September 21, 2020	Added typical IDD to tables. Added more frequency ranges to IDD tables. Updated H to be LVCMOS in order code.
April 27, 2020	Updated ODC parameter. 2nd LVCMOS row to be changed from <= to > 62.5 MHz.
September 7, 2018	Updated frequency stability options value from ±20ppm to ±25ppm for -40°C to +85°C XO only.
June 25, 2018	▪ Updated Package Outline Drawings section.
May 4, 2018	▪ Added XO and VCXO options. ▪ Updated description and Features sections. ▪ Updated Package Outline Drawings section. ▪ Added VCXO Ordering Information decoder diagram.
January 12, 2018	Initial release.

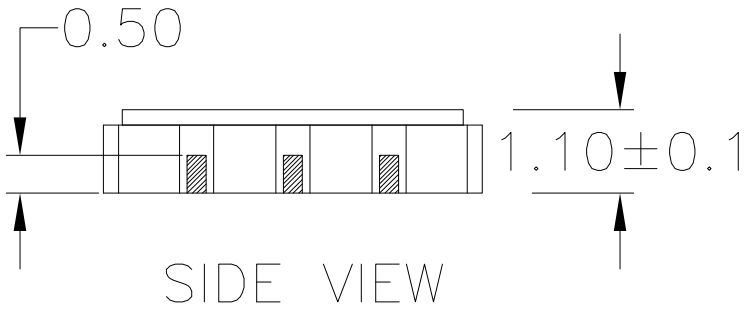
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	04/2/12	DP
01	ADDED LID IN TOP VIEW	07/12/12	KS
02	UPDATED LID TOLERANCES	12/03/12	KS
03	UPDATE PACKAGE DRAWING	8/8/14	J.HUA



TOP VIEW



BOTTOM VIEW



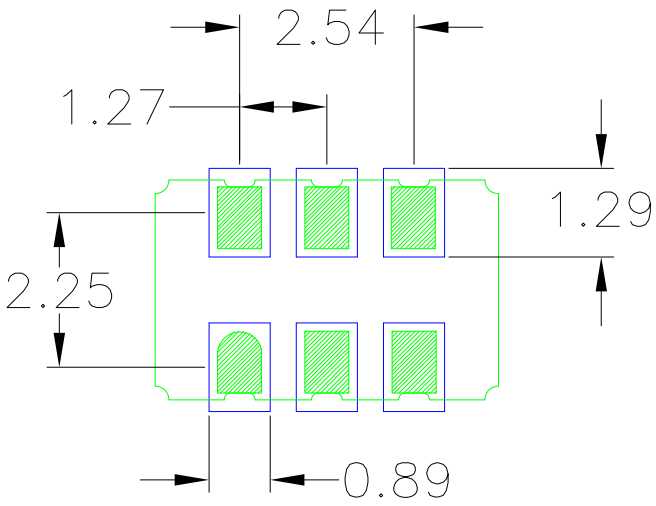
SIDE VIEW

NOTES:

1. ALL DIMENSIONS IN MM.

TOLERANCES UNLESS SPECIFIED DECIMAL XX± XXX± XXXX± ANGULAR ±		IDT™ www.IDT.com	6024 Silver Creek Valley Rd San Jose, CA 95138 PHONE: (408) 727-6116 FAX: (408) 492-8674
APPROVALS	DATE	TITLE JS6 PACKAGE OUTLINE 5.0 x 3.2 mm BODY 1.1 mm Thick	
DRAWN RAC	04/2/12		
CHECKED			
		SIZE C	DRAWING No. PSC-4411	REV 03
		DO NOT SCALE DRAWING	SHEET 1 OF 2

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	04/2/12	DP
01	ADDED LID IN TOP VIEW	07/12/12	KS
02	UPDATED LID TOLERANCES	12/03/12	KS
03	UPDATE PACKAGE DRAWING	8/8/14	J.HUA



RECOMMENDED LAND PATTERN

NOTES:

1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. COMPONENT OUTLINE SHOW FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

TOLERANCES UNLESS SPECIFIED
DECIMAL XX± XXX± XXXX±
ANGULAR ±

IDT™
www.IDT.com
6024 Silver Creek Valley Rd
San Jose, CA 95138
PHONE: (408) 727-6116
FAX: (408) 492-8674

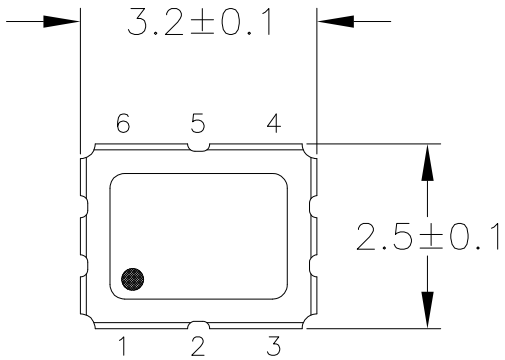
APPROVALS	DATE
DRAWN PEAC	04/2/12
CHECKED	

TITLE JS6 PACKAGE OUTLINE
5.0 x 3.2 mm BODY
1.1 mm Thick

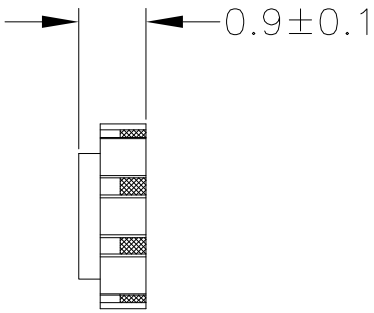
SIZE C | DRAWING No. PSC-4411 | REV 03

DO NOT SCALE DRAWING | SHEET 2 OF 2

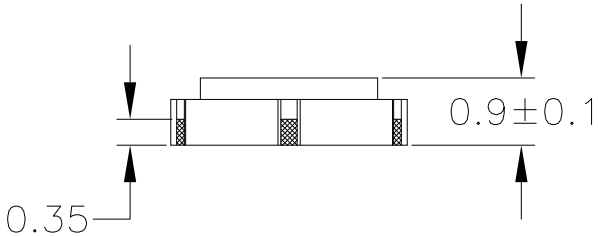
REVISIONS			
REV	DESCRIPTION	DATE CREATED	AUTHOR
00	INITIAL RELEASE	8/11/14	J.HUA
01	ADD PITCH	11/17/16	J.HUA
REFER TO DCP FOR OFFICIAL RELEASE DATE			



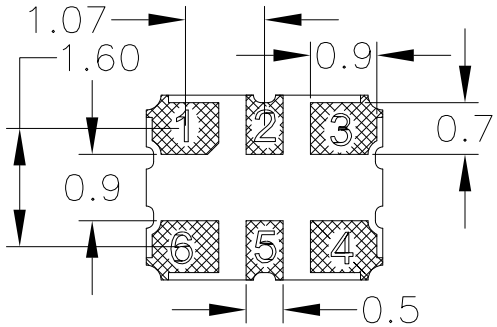
TOP VIEW



END VIEW



SIDE VIEW



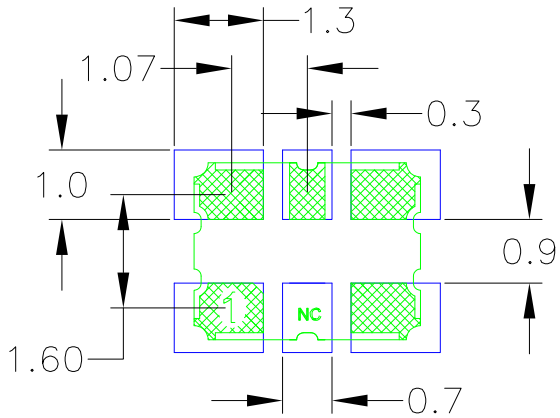
BOTTOM VIEW

NOTES:

1. ALL DIMENSIONS IN MM.

TOLERANCES UNLESS SPECIFIED		IDT™ www.IDT.com	6024 Silver Creek Valley Rd San Jose, CA 95138 PHONE: (408) 727-6116 FAX: (408) 492-8674	
DECIMAL XX± XXX± XXXX±	ANGULAR ±	TITLE	JX6 PACKAGE OUTLINE 3.2 x 2.5 mm BODY 0.9 mm Thick	
		SIZE C	DRAWING No. PSC-4412	REV 01
		DO NOT SCALE DRAWING		SHEET 1 OF 2

REVISIONS			
REV	DESCRIPTION	DATE CREATED	AUTHOR
00	INITIAL RELEASE	8/11/14	J.HUA
01	ADD PITCH	11/17/16	J.HUA
REFER TO DCP FOR OFFICIAL RELEASE DATE			



RECOMMENDED LAND PATTERN DIMENSION

NOTES:

1. ALL DIMENSIONS ARE IN MM. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. COMPONENT OUTLINE SHOWS FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

TOLERANCES UNLESS SPECIFIED

DECIMAL	ANGULAR
XX±	±
XXX±	
XXXX±	

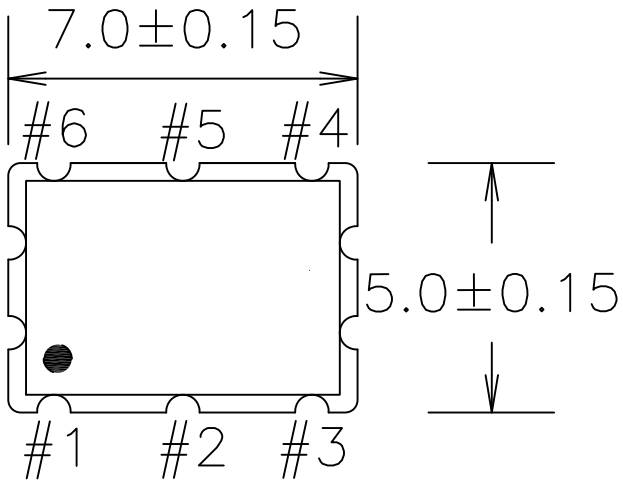
IDT™
www.IDT.com
6024 Silver Creek Valley Rd
San Jose, CA 95138
PHONE: (408) 727-6116
FAX: (408) 492-8674

TITLE JX6 PACKAGE OUTLINE
3.2 x 2.5 mm BODY
0.9 mm Thick

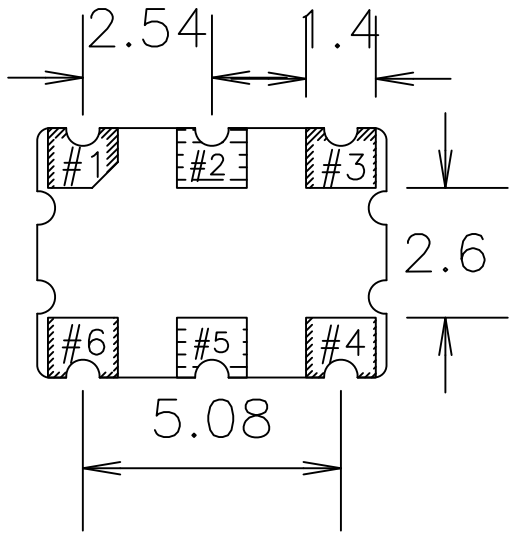
SIZE	DRAWING No.	REV
C	PSC-4412	01

DO NOT SCALE DRAWING

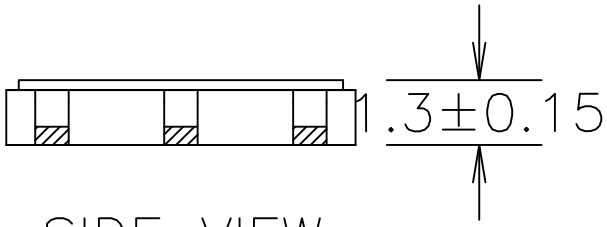
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	10/5/12	KS
01	UPDATE PACKAGE DRWING	8/12/14	J.HUA



TOP VIEW



BOTTOM VIEW



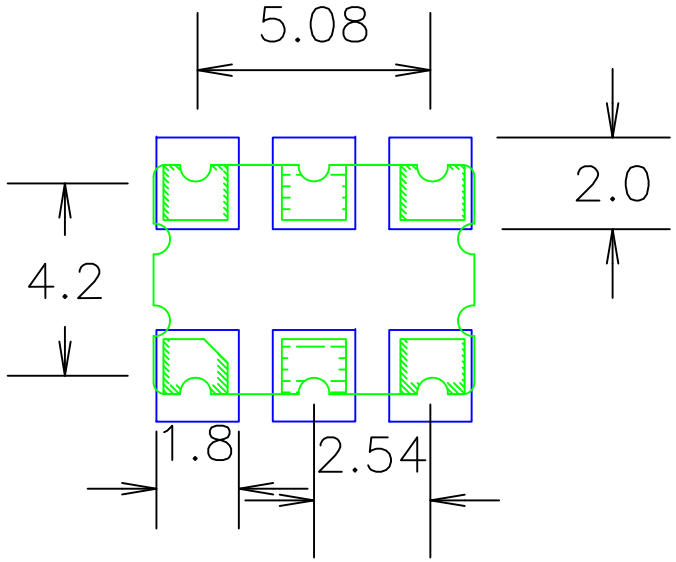
SIDE VIEW

NOTES:

1. ALL DIMENSIONS IN MM.

TOLERANCES UNLESS SPECIFIED DECIMAL XX± XXX± XXXX± ANGULAR ±		IDT™ www.IDT.com	6024 Silver Creek Valley Rd San Jose, CA 95138 PHONE: (408) 727-6116 FAX: (408) 492-8674
APPROVALS	DATE	TITLE JU6 PACKAGE OUTLINE 7.0 x 5.0 mm BODY 1.3 mm Thick	
DRAWN KB	10/03/12		
CHECKED			
		SIZE C	DRAWING No. PSC-4430	REV 01
		DO NOT SCALE DRAWING	SHEET 1 OF 2

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	10/5/12	KS
01	UPDATE PACKAGE DRWING	8/12/14	J.HUA



RECOMMENDED LAND PATTERN

NOTES:

1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. COMPONENT OUTLINE SHOW FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

TOLERANCES UNLESS SPECIFIED
DECIMAL XX± XXX± XXXX±
ANGULAR ±

APPROVALS	DATE
DRAWN JCB	10/03/12
CHECKED	

IDT™
www.IDT.com
6024 Silver Creek Valley Rd
San Jose, CA 95138
PHONE: (408) 727-6116
FAX: (408) 492-8674

TITLE JU6 PACKAGE OUTLINE
7.0 x 5.0 mm BODY
1.3 mm Thick

SIZE	DRAWING No.	REV
C	PSC-4430	01

DO NOT SCALE DRAWING

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use o any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

© 2023 Renesas Electronics Corporation. All rights reserved.